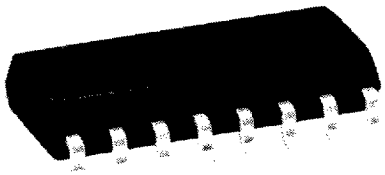
LOGIC/DELAY PROCESSOR

LAS-4820



FEATURES

- Programmable delay functions for noise immunity
- Undervoltage lockout
- SMD, & Plastic DIP packages
- Uncommitted operational amplifier with analog and digital output
- Two external inputs
- 5 status outputs for Power On Clear, Power Down Imminent, Overvoltage, Undervoltage and Power Good Status
- Guaranteed specifications over temperature

DESCRIPTION

The LAS-4820 is a high performance monolithic integrated circuit–logic/delay processor, designed for accepting logic signals from the LAS-4810 Primary Input Comparator I.C. and logic signals from an output voltage monitoring I.C. such as a UN8130LW or a UC3544. Included in the device are independent delay programming for the POC, PDI, OV and UV signals for noise immunity, and 2 external inputs for additional signal monitoring, an uncommitted operational amplifier with an analog output, and an inverted digital output. The device also incorporates a POWER GOOD status output, providing the user an overall "system status" output.

The LAS-4820 is available in 3 packages — surface mount, plastic DIP and hermetic CERDIP.

ABSOLUTE MAXIMUM RATINGS

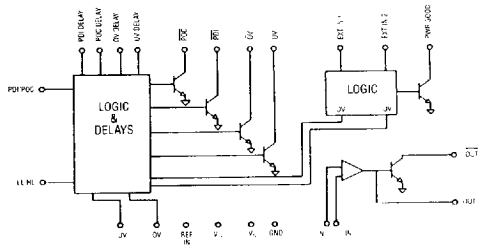
PARAMETER	SYMBOL	VALUE	UNITS
Input Voltage	V_S	32	Volts
Input Voltage	V_{CC}	36	Volts
Output Sink Current $\overline{POC}$, PDI, $\overline{UV}$, $\overline{OV}$, POWER GOOD, OUT, $\overline{OUT}$	I_{SK}	10	mA
Output Collector Voltage	V_C	32	Volts
Input Voltage PDI/POC, HL/LL, OV, UV	V_{IN}	5	Volts
Ext Inputs 1, 2, +IN, −IN	E_{IN}	32	Volts
Reference Input Voltage		6	Volts
Ambient Operating Temperature Range SMD Plastic DIP CERDIP		 0–70 0–70 −55–125	 °C °C °C
Thermal Resistance Junction to Ambient θ_{JA} SMD Plastic DIP CERDIP		 75 65 65	 °C/W °C/W °C/W
Storage Temperature Range All Packages		 −65–150	 °C
Lead Temperature (Soldering, 10 seconds)		260	°C

DEVICE SELECTION GUIDE

DEVICE	PACKAGE
LAS-4820S	Surface mounted device
LAS-4820P	Plastic DIP
LAS-4820L	CERDIP

19

BLOCK DIAGRAM (simplified)



ELECTRICAL CHARACTERISTICS

Test conditions: [1]V_{SS} = 15V, V_{CC} = 5V, V_{REF} = 2.5, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min.	Typ	Max.	Units
INPUT CHARACTERISTICS						
Hysteresis (All Inputs)				10		mV
POC/PDI Logic	Low High		 3.0		1.0	Volts Volts
Clamp Source Current	V_{CL}		4.7 65			Volts uA
HL/LL Logic	Low High		 3.0		1.0	Volts Volts
Clamp Source Current	V_{CL}		4.7 65			Volts uA
UV/OV Logic	Low High		 3.0		1.0	Volts Volts
V_S Range			11.7		32	Volts
V_{CC} Range			2		36	Volts
Undervoltage Lockout Trip Voltage Reset Voltage	 V_T V_R		 11.7		 10.3	 Volts Volts
EXTERNAL INPUTS						
Input High	$V_{EXT-IN\ HI}$				2.0	Volts
Input Low	$V_{EXT-IN\ LOW}$		0.4			Volts
DELAYS						
Source Current	IS		100		300	uA
Logic Delay	LD	C = 1 uFD		15		mSec
Quiescent Current	VCC IQ	VCC = 2 to 36V		3.0	5	mA
VREF IQ Input	VR IQ VS IQ VS IQ	V = 2.5 VS below UV lockout VS above UV lockout		2.7	4 2 10	mA mA mA
STATUS OUTPUTS $\overline{PDI}$, $\overline{POC}$, $\overline{UV}$, $\overline{OV}$, Power Good, OUT, $\overline{OUT}$						
Saturation Voltage	VS	I = 10mA		0.5	0.7	Volts
OPERATIONAL AMPLIFIER						
Input offset voltage Input bias current				5 100	15 360	mV uA
Open loop gain CMRR PSRR Unity gain frequency Slew rate		V C.M. = 0 to +VS −2.0V TA = 25°C		60 60 60 1.2 1		dB dB dB MHz V/uSec
Short circuit current Output voltage swing Positive Negative			 14	50	 100	mA Volts mV
Inverted output Saturated Voltage		I = 10ma		200	500	mV

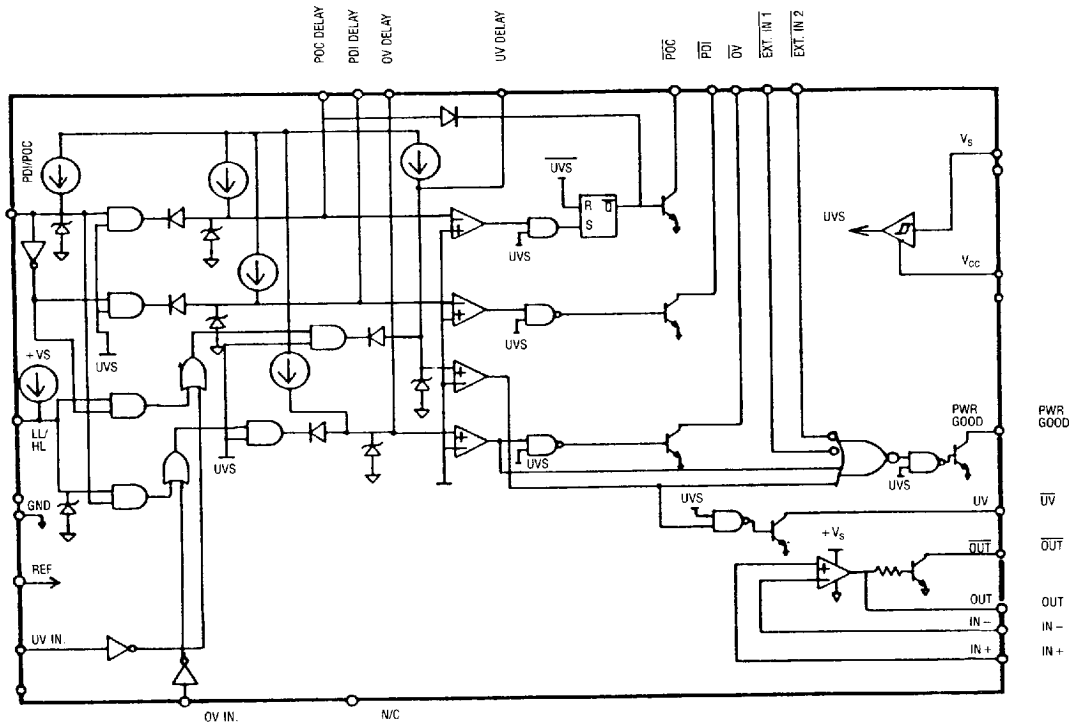
[1] T_A = 0°C–70°C (LAS-4820S, P); T_A = −55°C to 125°C (LAS-4820L)

19

LOGIC/DELAY PROCESSOR

LAS-4820

BLOCK DIAGRAM



LAS-4820 Inputs versus Status Output Functions

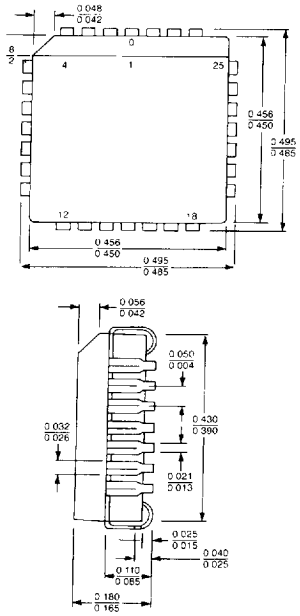
PDI/POC:	Input logic high for POC and a high line input fault. Input logic low for PDI and a low line input fault.
LL/HL:	Input logic high for either low line or a high line input fault.
U.V.:	Input logic low for a U.V. output fault.
O.V.:	Input logic low for a O.V. output fault.
EXT 1, 2:	Input logic low for other faults.

19

LOGIC/DELAY PROCESSOR

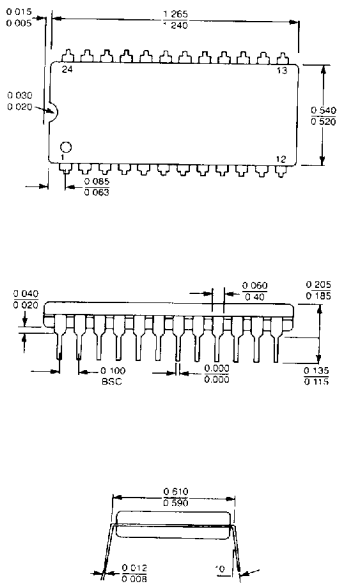
DEVICE OUTLINE

LAS-4820S



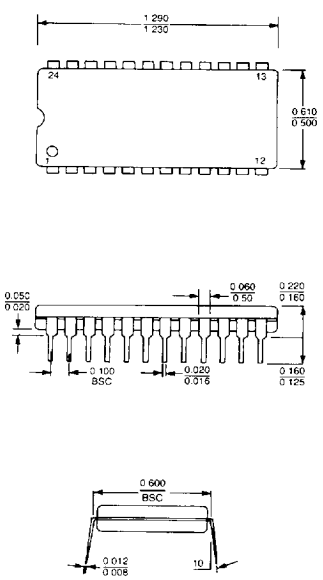
1—PDI Delay
2—VCC
3—NC
4—$\overline{UV}$
5—VREF-IN
6—$\overline{PDI}$
7—$\overline{POC}$
8—$\overline{OV}$
9—POWER GOOD
10—EXT 1
11—EXT 2
12—VS
13—+IN
14—−IN
15—$\overline{OUT}$
16—$\overline{OUT}$
17—GND
18—NC
19—OV Delay
20—LL/HL
21—PDI/POC
22—NC
23—NC
24—OV IN
25—UV IN
26—NC
27—UV Delay
28—POC Delay

LAS-4820P



1—$\overline{UV}$
2—VREF IN
3—$\overline{PDI}$
4—$\overline{POC}$
5—$\overline{OV}$
6—POWER GOOD
7—EXT 1
8—EXT 2
9—VS
10—+IN
11—−IN
12—$\overline{OUT}$
13—$\overline{OUT}$
14—Gnd
15—OV Delay
16—NC
17—LL/HL
18—PDI/POC
19—OV IN
20—UV IN
21—UV Delay
22—POC Delay
23—PDI Relay
24—VCC

LAS-4820L



1—$\overline{UV}$
2—VREF IN
3—$\overline{PDI}$
4—$\overline{POC}$
5—$\overline{OV}$
6—POWER GOOD
7—EXT 1
8—EXT 2
9—VS
10—+IN
11—−IN
12—$\overline{OUT}$
13—$\overline{OUT}$
14—GND
15—OV Delay
16—NC
17—LL/HL
18—PDI/POC
19—OV IN
20—UV IN
21—UV Delay
22—POC Delay
23—PDI Relay
24—VCC

NOTE: All dimensions are in inches.