HARRIS SEMICONDUCTOR

HCTS7266MS

Radiation Hardened Quad 2-Input Exclusive NOR Gate

December 1992

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K or 1 Mega-RAD(Si)
- Dose Rate Upset >10^{10} RAD(Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10^{-9} Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = 2.0V Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

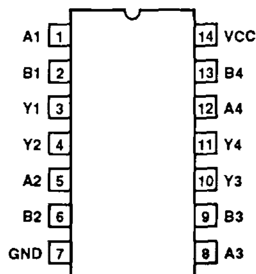
The Harris HCTS7266MS is a Radiation Hardened quad 2-Input exclusive NOR Gate. A logic level high on either one of the inputs (A or B) will force the output (y) low. A high on both inputs, or a low on both inputs will force the output to a logic high.

The HCTS7266MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family with TTL input compatibility.

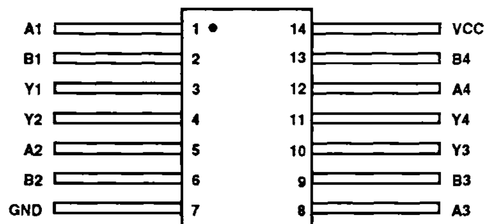
The HCTS7266MS is supplied in a 14 lead Ceramic flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE
MIL-STD-1835 CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLAT PACK
MIL-STD-1835 CDFP3-F14, LEAD FINISH C
TOP VIEW

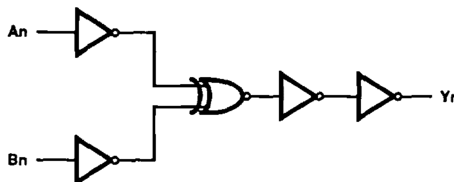


Truth Table

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number 3384

Absolute Maximum Ratings

Supply Voltage . . . . -0.5V to +7.0V
Input Voltage Range, All Inputs . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input. . . . . ±10mA
DC Drain Current, Any One Output. . . . . ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) . . . . -65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . +265°C
Junction Temperature . . . . +175°C
ESD Classification . . . . Class 1

Reliability Information

Thermal Impedance	θ_{ja}	θ_{jc}
Weld Seal DIC	75°C/W	16°C/W
Weld Seal Flat Pack	64°C/W	12°C/W

Power Dissipation per Package (PD)
For T_A = -55°C to +100°C 1W
For T_A = +100°C to +125°C . . . . Derate Linearly at 13mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . 500ns Max
Operating Temperature Range (T_A) . . . . -55°C to +125°C
Input Low Voltage (VIL). . . . . 0.0V to 0.8V
Input High Voltage (VIH) . . . . VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	10	µA
			2, 3	+125°C, -55°C	-	200	µA
Delta ICC	ΔICC	VCC = 5.5V, VIN = VCC or GND 1 Input = 2.4V	1	+25°C	-	1.6	mA
			2, 3	+125°C, -55°C	-	3.2	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V (Note 2)	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V (Note 2)	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.80V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.80V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.80V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. Force/Measure functions may be interchanged.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Input to Output	TPHL	VCC = 4.5V, VIH = 3.0V VIL = 0V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	22	ns
	TPLH	VCC = 4.5V, VIH = 3.0V VIL = 0V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	29	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, F = 1MHz	1	+25°C	Typical 20		pF
			1	+125°C	Typical 30		pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, F = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	1	+25°C	1	15	ns
			1	+125°C, -55°C	1	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.2	-	1.0	mA
Delta ICC	ΔICC	VCC = 5.5V, VIN = VCC or GND 1 Input = 2.4V	+25°C	-	3.2	-	3.2	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	+25°C	4.0	-	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC-0.4V, VIL = 0V	+25°C	-4.0	-	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOL = 50μA	+25°C	-	0.1	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V at 200K RAD, VIL = 0.3V at 1M RAD, IOH = -50μA	+25°C	VCC -0.1	-	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	-	±5	μA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETERS	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMP-ERATURE	200K RAD LIMITS		1M RAD LIMITS		UNITS
				MIN	MAX	MIN	MAX	
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.80V @ 200K RAD, VIL = 0.30V @ 1M RAD (Note 3)	+25°C	-	-	-	-	-
Propagation Delay Input to Outputt	TPHL	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	22	2	28	ns
Propagation Delay Input to Output	TPLH	VCC = 4.5V, VIH = 3.0V, VIL = 0V	+25°C	2	29	2	37	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	+3	µA
IOL/IOH	-15	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	

NOTE:

1. Alternate Group A in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONDITIONS (Note 1)					
3, 4, 10, 11	1, 2, 5, 6, 7, 8, 9, 12, 13	-	14	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
3, 4, 10, 11	7	-	1, 2, 4, 5, 8, 9, 12, 13, 14	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	7	3, 4, 10, 11	14	1, 5, 8, 12	2, 6, 9, 13

NOTES:

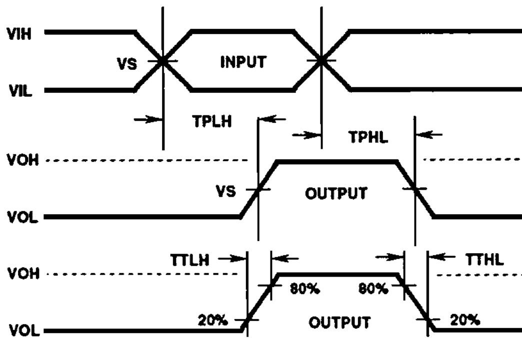
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
3, 4, 10, 11	7	1, 2, 5, 6, 8, 9, 12, 13, 14

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

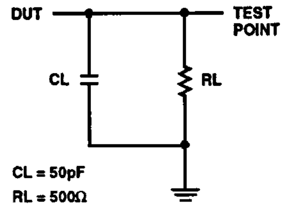
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
84 x 84 mils
2.20 x 2.24mm

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

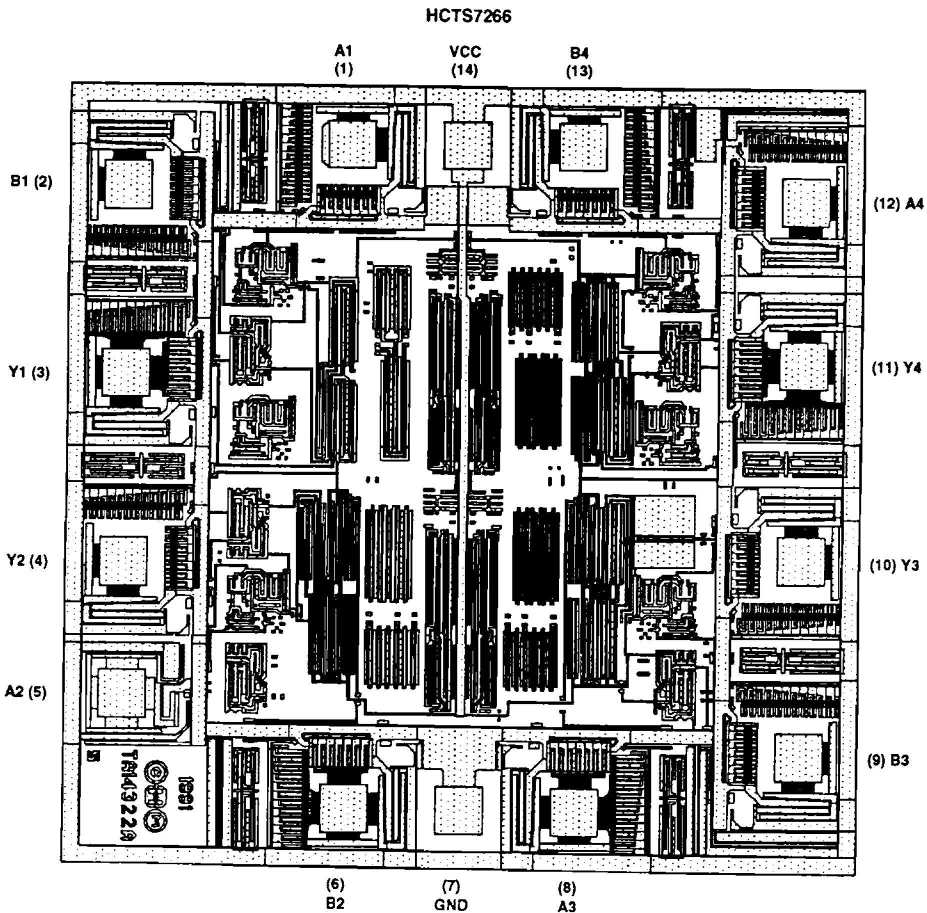
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

DIE ATTACH:
Material: Silver Epoxy

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100μm x 100μm
4 x 4mm

Metallization Mask Layout



CD4000 MS Screening

Wafer Lot Acceptance	(All Lots)	Method 5007 (Includes SEM)
Radiation Verification	(EachWafer)	Method 1019, 4 Samples/Wafer, 0 Rejects
Nondestructive Bond Pull	100%	Method 2023
Internal Visual Inspection	100%	Method 2010
Temperature Cycling	100%	Method 1010 Condition C (-65°C to +150°C)
Constant Acceleration	100%	
PIND Testing	100%	
External Visual Inspection	100%	
Serialization	100%	
Initial Electrical Test	100%	
Static Burn-In I	100%	Method 1015, 24 Hours, +125°C Minimum
Interim Electrical Test I	100%	(Note 1)
Static Burn-In II	100%	Method 1015, 24 Hours, +125°C Minimum
Interim Electrical Test II	100%	(Note 1)
Dynamic Burn-In	100%	Method 1015, 240 Hours, +125°C or Equivalent
Interim Electrical Test III	100%	(Note 1)
Final Electrical Test	100%	
Fine and Gross Seal	100%	Method 1014
Radiographics	100%	Method 2012 (2 Views)
External Visual	100%	Method 2009
Group A (All Tests)		Method 5005 (Class S)
Group B (Optional)		Method 5005 (Class S) (Note 2)
Group D (Optional)		Method 5005 (Class S) (Note 2)
CSI and/or GSI (Optional)		(Note 2)
Data Package Generation		(Note 3)

NOTES:

1. Failure from interim electrical tests I and II are combined for determining PDA (PDA = 5% for subgroups 1, 7 and delta failures combined, PDA = 3% for subgroup 7 failures). Interim electrical tests III PDA (PDA = 5% for subgroups 1, 7 and delta failures combined, PDA = 3% for subgroup 7 failures.
2. These steps are optional, and should be listed on the purchase order if required.
3. Data Package Contents:
   Cover Sheet (P.O. #, Customer #, Lot Data Code, Harris #, Lot #, Quantity.
   Certificate of Conformance (as found on shipper).
   Lot Serial Number Sheet (Good Unit(s), Serial # and Lot #).
   Variables Data (All Read, Record and Delata Operations).
   Group A Attributes Data Summary.
   Wafer Lot Acceptance Report (Method 5007) to include SEM photos. NOTE: SEM photos to include % of step coverage.
   X-Ray Report and file(s), including parameter measurements.
   GAMMA Radiation Report with initial shipment of devices from the same wafer lot; Containing a cover page, Disposition, Rad Dose, Lot #, Test Package, Spec #(s), Test Equipment, etc.
   Irradiation Read and Record data will be on file at Harris.