

CD54/74HC4024

CD54/74HCT4024

T-45-23-17

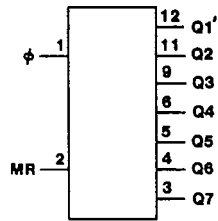
High-Speed CMOS Logic

HARRIS SEMICONDUCTOR

27E D



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92CS-38450R1
CD54/74HC4024, HCT4024
FUNCTIONAL DIAGRAM

7-Stage Binary Ripple Counter

Type Features:

- Fully static operation:
- Buffered inputs:
- Common reset
- Typical $f_{MAX} = 50 \text{ MHz}$ @ $V_{CC} = 5 \text{ V}$, $C_L = 15 \text{ pF}$, $T_A = 25^\circ \text{C}$

The RCA-CD54/74HC4024 and CD54/74HCT4024 are 7-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each input pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

The CD54HC4024 and CD54HCT4024 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4024 and CD74HCT4024 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (over temperature range):
Standard outputs - 10 LSTTL loads
Bus driver outputs - 15 LSTTL loads
- Wide operating temperature range:
CD74HC/HCT: -40 to $+85^\circ \text{C}$
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- Alternate source is Philips/Signetics
- CD54HC/CD74HC types:
2 to 6 V operation
High noise immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}
@ $V_{CC} = 5 \text{ V}$
- CD54HCT/CD74HCT types:
4.5 to 5.5 V operation
Direct LSTTL input logic compatibility
 $V_{IL} = 0.8 \text{ V max.}$, $V_{IH} = 2 \text{ V min.}$
CMOS input compatibility
 $I_i \leq 1 \mu\text{A}$ @ V_{OL} , V_{OH}

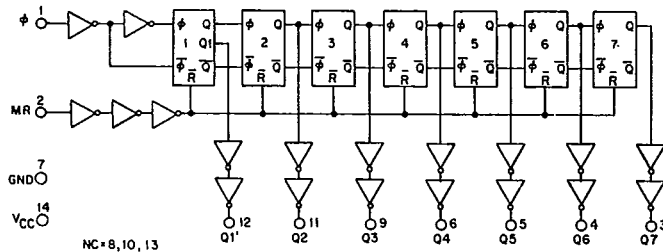


Fig. 1 - Logic diagram for the CD54/74HC/HCT4024.

TRUTH TABLE

ϕ	MR	OUTPUT STATE
	L	No Change
	L	Advance to Next State
X	H	All Outputs are Low

H = high level (steady state)
L = low level (steady state)
X = don't care

CD54/74HC4024

CD54/74HCT4024

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$
Unit Inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A =Full Package Temperature Range) V_{CC}^*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage, V_i, V_o	0	V_{CC}	V
Operating Temperature, T_A :			$^\circ\text{C}$
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f :			ns
at 2 V	0	1000	
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

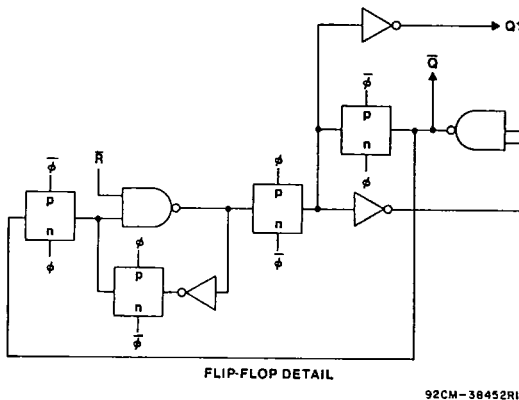


Fig. 2 - Flip-Flop No. 1 detail.

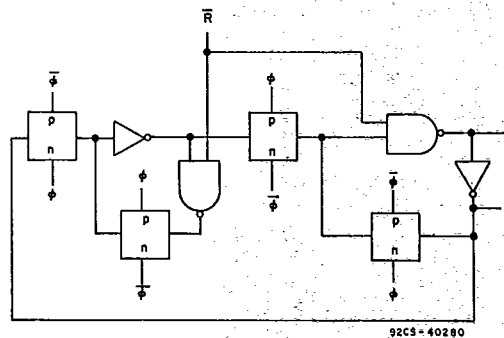


Fig. 3 - Detail for flip-flops 2 through 7.

CD54/74HC4024 CD54/74HCT4024

STATIC ELECTRICAL CHARACTERISTICS

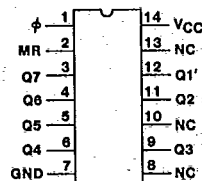
CHARACTERISTICS	CD74HC4024/CD54HC4024										CD74HCT4024/CD54HCT4024										UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE			
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V _I V	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5	2	—	—	2	—	2	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	to	—	—	0.8	—	0.8	—	0.8	V	
			6	4.2	—	—	4.2	—	4.2	—	—	5.5	—	—	—	—	—	—	—	V	
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5	—	—	0.8	—	0.8	—	0.8	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	—	—	—	—	—	V	
			6	—	—	1.8	—	1.8	—	1.8	—	5.5	—	—	—	—	—	—	—	V	
High-Level Output Voltage V _{OH}	V _L	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL}	4.5	4.4	—	—	4.4	—	4.4	—	V	
or			4.5	4.4	—	—	4.4	—	4.4	—	or			—	—	—	—	—	—	—	V
CMOS Loads	V _{IH}		6	5.9	—	—	5.9	—	5.9	—	V _{IH}			—	—	—	—	—	—	—	V
TTL Loads	V _{IL}										V _{IL}	4.5	3.98	—	—	3.84	—	3.7	—	V	
or	-4	4.5	3.98	—	—	3.84	—	3.7	—	or			—	—	—	—	—	—	—	V	
V _{IH}	-5.2	6	5.48	—	—	5.34	—	5.2	—	V _{IH}			—	—	—	—	—	—	—	V	
Low-Level Output Voltage V _{OL}	V _L	0.02	2	—	—	0.1	—	0.1	—	0.1	V _L	4.5	—	—	0.1	—	0.1	—	0.1	V	
or			4.5	—	—	0.1	—	0.1	—	0.1	or			—	—	—	—	—	—	—	V
CMOS Loads	V _{IH}		6	—	—	0.1	—	0.1	—	0.1	V _{IH}			—	—	—	—	—	—	—	V
TTL Loads	V _{IL}										V _{IL}	4.5	—	—	0.26	—	0.33	—	0.4	V	
or	4	4.5	—	—	0.26	—	0.33	—	0.4	or			—	—	—	—	—	—	—	V	
V _{IH}	5.2	6	—	—	0.26	—	0.33	—	0.4	V _{IH}			—	—	—	—	—	—	—	V	
Input Leakage Current I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA	
Quiescent Device Current I _{CC}	V _{CC} or Gnd	0	6	—	—	8	—	80	—	160	V _{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA	
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI _{CC} *											V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA	

*For dual-supply system: theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
φ, MR	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @25°C.



TOP VIEW

92CS-38453RI

TERMINAL ASSIGNMENT

CD54/74HC4024 CD54/74HCT4024

 SWITCHING CHARACTERISTICS ($V_{CC}=5\text{ V}$, $T_A=25^\circ\text{C}$, Input $t_i, t_r=6\text{ ns}$)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay ϕ to Q1'	t_{PHL} t_{PLH}	15	11	17	ns
Qn to Qn+1	t_{PHL} t_{PLH}	15	6	6	
MR to Qn	t_{PHL} t_{PLH}	15	14	17	
Power Dissipation Capacitance*	C_{PD}	—	30	30	pF

 * C_{PD} is used to determine the dynamic power consumption, per package.

 $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_i / M)$ where:

 $M=2^1, 2^2, 2^3, 2^4, 2^5, 2^6, 2^7$
 C_L =output load capacitance

 f_i =input frequency

Prerequisite for Switching Function

CHARACTERISTIC	SYMBOL	V _{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Maximum Input Pulse Frequency	f _{MAX}	2 4.5 6	6 30 35	— — —	— 25 —	— — —	5 24 29	— — —	— 20 —	— — —	4 20 24	— — —	— 16 —	— — —	MHz
Input Pulse Width	t _w	2 4.5 6	80 16 14	— — —	— 20 —	— — —	100 20 17	— — —	— 25 —	— — —	120 24 20	— — —	— 30 —	— — —	ns
Reset Removal Time	t _{REM}	2 4.5 6	50 10 9	— — —	— 10 —	— — —	65 13 11	— — —	— 13 —	— — —	75 15 13	— — —	— 15 —	— — —	
Reset Pulse Width	t _w	2 4.5 6	80 16 14	— — —	— 20 —	— — —	100 20 17	— — —	— 25 —	— — —	120 24 20	— — —	— 30 —	— — —	

 SWITCHING CHARACTERISTICS ($C_L=50\text{ pF}$, Input $t_i, t_r=6\text{ ns}$)

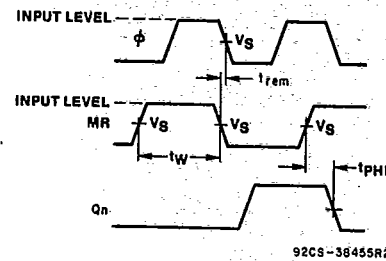
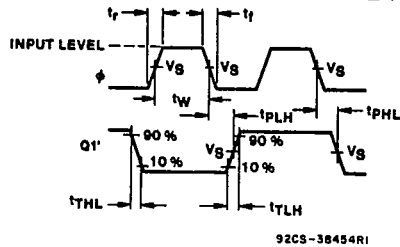
CHARACTERISTIC	SYMBOL	V _{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, ϕ to Q1' Output	t _{PLH}	2	—	140	—	—	—	175	—	—	—	210	—	—	ns
	t _{PHL}	4.5	—	28	—	40	—	35	—	50	—	42	—	60	
		6	—	24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay Q _n to Q _{n+1}	t _{PLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t _{PHL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	13	—	—	—	19	—	—	
Propagation Delay MR to Q _n	t _{PHL}	2	—	170	—	—	—	215	—	—	—	255	—	—	ns
		4.5	—	34	—	40	—	43	—	50	—	51	—	60	
		6	—	29	—	—	—	27	—	—	—	43	—	—	
Output Transition Time	t _{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
	t _{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C _I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC4024
CD54/74HCT4024

HARRIS SEMICONDUCTOR

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	54/74HC	54/74HCT
Input Level	V _{CC}	3 V
Switching Voltage, V _S	50% V _{CC}	1.3 V

Fig. 4 - Input Pulse pre-requisite times, propagation delays and output transition times.

Fig. 5 - Master Reset pre-requisite and propagation delays.