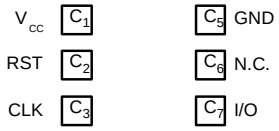
BL7431A 256-Bit EEPROM Logical Encrypted Chip

Description

BL7431A is the memory card chip developed by Shanghai Belling Co.,Ltd.. The chip uses Shanghai Belling's 1.2um CMOS & EEPROM process. It has 256 bits EEPROM(A type) or 512 bits EEPROM(B type) with logical encryption function, its contact configuration is in accordance to ISO standard 7816-3(Synchronous Transmission). It can be used widely in intelligent public telephone area.

Pin Diagram



Features

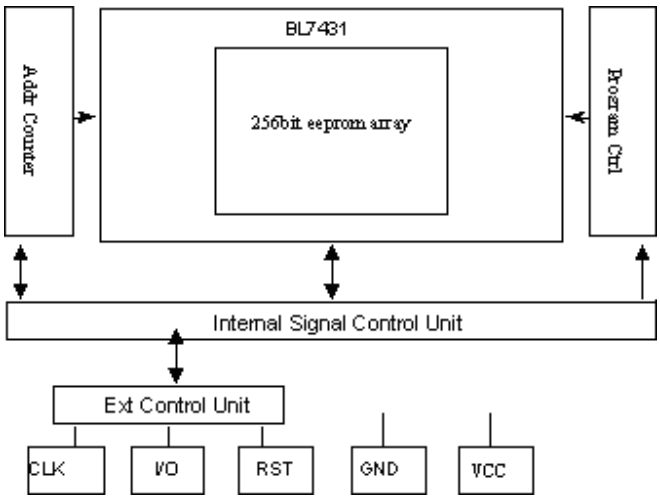
- 256X 1bit E^2PROM(A Type)；512 X 1bit E^2PROM(B Type)
- Read and write by bit, erase by byte
- Logical encryption ensure the security of data and password
- Typical EEPROM program time is 5ms
- Operation Voltage：5V
- Operation Current：<1mA
- Minimal Erase/Write Cycle：10^5
- Data Retention: no less than 10 year
- In accordance to ISO standard 7816-3(Synchronous Transmission)

Pin Description

Pin No.	Parameter	Symbol	Test Condition
1	C1	V_{CC}	Supply Voltage
2	C2	RST	Control input (reset signal)
3	C3	CLK	Clock input
4	C5	GND	Ground
5	C6	N.C.	Not connected
6	C7	I/O	Bidirectional data line (open drain)

Function Description

- **Block Diagram**



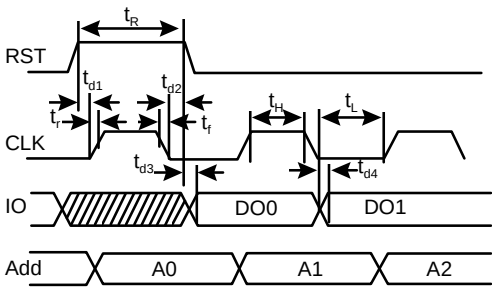
- **Partition of EEPROM**

Address		Memory Function Type					Function
		Before personalize（transmission password not verified）	Before personalize（Transmission password verified）	After personalize			
				Second password not verified	Second password verified	FG=1	
Area1	0~15	ROM	ROM	ROM			Chip Manufacture Code
Area2	16~23	ROM	PROM	ROM			Card Manufacture Code
Area3	24~63	ROM	PROM	ROM			Issue Code
Area4	64	ROM	PROM	ROM			Personalized Flag
	65~71	ROM	PROM	ROM			
	72~79	PROM	EEPROM	ROM			Used as error counter before personalization
	80~103	ROM(can not be read)	EEPROM	ROM			Store the transmission password before personalization After personalization, used as common memory
Area5	104~143	ROM	EEPROM	EEPROM			Issue Extend Code
Area6	144	ROM	EEPROM	ROM	EEPROM		FG Flag
	145~151	ROM	EEPROM	ROM	EEPROM		
Area7	152~159	ROM	EEPROM	PROM	EEPROM		Second Error Counter
Area8	160~183	ROM	EEPROM	ROM（can not be read）	EEPROM		Password of User Data
Area9	184~255	ROM	EEPROM	ROM（can not be read）	EEPROM		User Data
Area10	256~511	ROM	EEPROM	EEPROM			User Data(only in BL7431B)

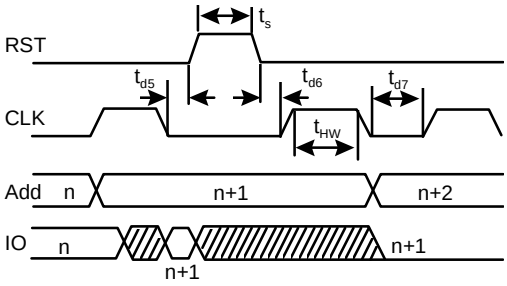
- **Read/Write Operation**

Reading Operation

The address counter inside the chip use bit as counter-unit, at every clock's rising edge, it increases 1. At the falling edge of every clock, data in current address will be sent to I/O port. When CLK is high and RST also is high, the address counter will be cleared to zero.



Address reset and data output



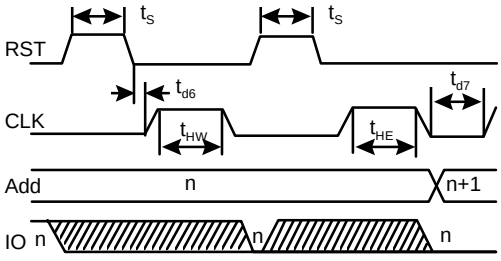
writing operation timing diagram

Writing Operation

When RST is high and CLK is low, "R" flag inside the chip will be set. Under such condition, when next CLK arrived, the chip will enter writing process with address counter no increasing. During writing operation, CLK keep high. When writing operation is finished, at the falling edge of CLK, address counter will be effective again, at the same time, "R" flag will be reset. To chip manufacture area, "R" flag has no use.

Erasing Operation

When writing operation is finished, if again comes a "RST pulse" and CLK keep low, "R" flag will be set again and the chip enter erasing status. Such operation to any bit of same byte has same effect. To PROM area, erase is invalid.



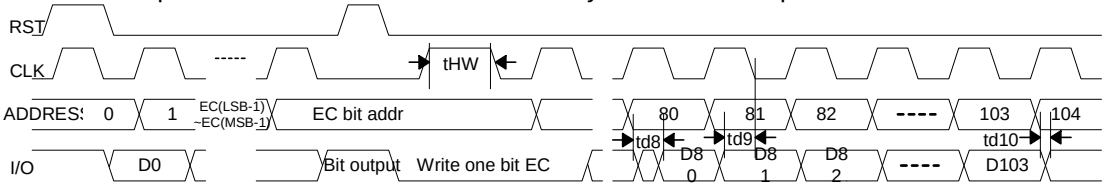
Erasing operation timing diagram

Power on reset

Address is reset after power on. At this time, RST must keep high than one CLK period. When RST goes low, data in address zero will be sent to I/O port.

About Comparison of Transmission Password

Password comparison must be executed immediately after write "0" operation



Comparison of Transmission Password timing diagram

Electrical Parameter

- **Absolute Maximum Parameter**

Parameter	Symbol	Limited Value			Unit
		Min	Typ	Max	
Power Voltage	V_{CC}	-0.3	-	6.0	V
Input Voltage	V_I	-0.3	-	6.0	V
Storage Temperature	T_S	-40	-	125	℃
ESD Protection	Vs		4000		V
Power dissipation	P_{tot}	-	-	50	mW

- **DC Characteristic**

Parameter	Symbol	Limited Value			Unit
		Min	Typ	Max	
H Input Voltage (I/O,CLK,RST)	V_H	3.5	-	V_{CC}	V
L Input Voltage (I/O,CLK,RST)	V_L	-	-	0.8	V
RST,CLK H Input Current	I_H	-	-	1	μA
RST,CLK L Input Current	$-I_L$	-	-	1	μA
L Output Current	I_L	-	-	0.5	mA
H Output Current	I_H	-	-	10	μA
Input Capacitance	C_I	-	-	10	pF
Power Voltage	V_{CC}	4.75	5	5.5	V
Power Current	I_{CC}	-	1	-	mA

- **AC Characteristic**

Parameter	Symbol	Limited Value			Unit
		Min	Typ	Max	
Clock Frequency	CLK			50	KHz
Clock H Level	t_H	10			μs
Clock L Level	t_L	10			μs
Rise Time	t_r			1	μs
Fall Time	t_f			1	μs
Reset Hold Time	t_R	50			μs
	t_S	10			μs
Writing Time	t_{HW}	5			ms
Erasing Time	t_{HE}	5			ms