AP8804
LOW VOLTAGE PULSED LED DRIVER

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Description

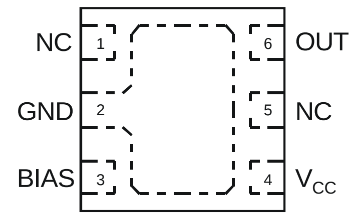
The AP8804 is a low voltage linear LED driver capable of operating from supplies as low as 1.8V.

The AP8804 has an output current tolerance of 10% at 25°C at 250mA and 15% at the full rated current of 350mA.

The maximum output saturation voltage at the full rated current is 200mV.

Pin Assignments

TDFN2020-6

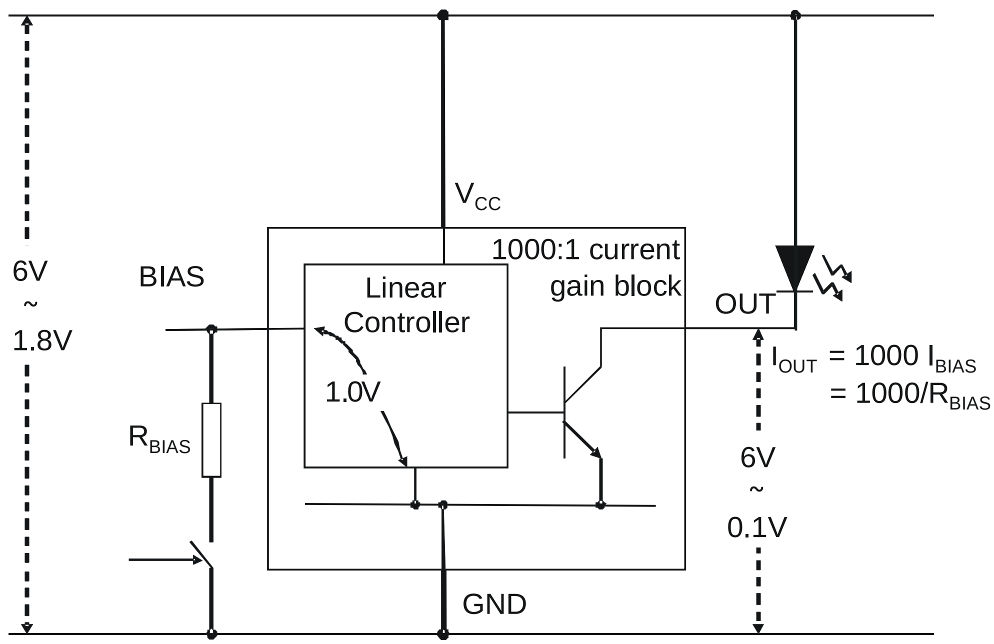


Top View

Features

- 100mV Maximum output saturation voltage
- TDFN small outline package
- 10% Output current tolerance
- 0 to 70°C Junction temperature range
- Available in "Green" Molding Compound (No Br, Sb) with lead free Finish/RoHS Compliant (Note1)

Typical Application Circuit



Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied, see *EU Directive 2002/95/EC Annex Notes*.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	-0.3 to +8 (Relative to GND)	V
V_{OUT}	Output Voltage		
V_{BIAS}	Bias Input Voltage	-0.3 to +0.3 (Relative to GND)	V
T_J	Junction Temperature	150	°C
T_{ST}	Storage Temperature	-65 to +150	°C

Note: These are stress ratings only. Operation outside the absolute maximum ratings may cause device failure. Operation at the absolute maximum rating for extended periods may reduce device reliability.
Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	1.8	6	V
I_{BIAS}	BIAS Input Current	-0.33	0	mA
I_O	Output Current	50	350	mA
T_A	Operating Ambient Temperature Range	0	70	°C

Package Thermal Data

Thermal Resistance	Package		Unit
Junction-to-Ambient, θ_{JA}	TDFN2020-6	80	°C/W
Junction-to-Case, θ_{JC}	TDFN2020-6	20	

Electrical Characteristics (Under Operating Conditions)

V_{OUT} = 0.2V, T_A = 25°C (unless otherwise stated). All typical are at 25°C (FT = 0 to 70°C)

Parameter	Conditions	T_A	Min	Typ.	Max	Unit
DC parameters						
Bias voltage	V_{CC} = 1.8V, R_{BIAS} = 3.05kΩ[2]	25	900	1040	1200	mV
		FT	860		1240	
Output current accuracy[3]	V_{CC} = 2.0V to 6V, V_{OUT} = V_{CC} – 1.8V, R_{BIAS} = 4.1kΩ	25	225	250	275	mA
Saturated output current tolerance[5]	V_{CC} = 2.0V, V_{OUT} = 0.2V R_{BIAS} = 3.05kΩ, I_{OUT} = 350mA	25			15	%
		FT			20	
	V_{CC} = 2.0V, V_{OUT} = 0.5V R_{BIAS} = 3.05kΩ I_{OUT} = 350mA	25			10	%
		FT			15	
	V_{CC} = 2.0V, V_{OUT} = 0.15V R_{BIAS} = 4.1kΩ, I_{OUT} = 250mA	25			15	%
		FT			20	
Current Gain (I_{OUT}/I_{BIAS})[3, 4]	V_{CC} = 2V, V_{OUT} = 0.2V, 50µA < I_{BIAS} < 350µA	25		1000		
Quiescent current	V_{CC} = 6V, R_{BIAS} = Open Circuit	FT		100	150	µA
Supply current (Active)	V_{CC} = 2V, R_{BIAS} = 3.05kΩ, V_{OUT} = 0.5V	FT		5.5	9	mA
Output Leakage (Off)	Vcc = 6V, R_{BIAS} >= 2MΩ, V_{OUT} = 6V	25		<1	10	uA
Output Leakage (Disabled)	Vcc = 0V, V_{OUT} = 6V	25		<1	100	nA
AC parameters						
Rise time (10% to 90%)[5]	V_{CC} = 2.0V, V_{OUT} = 0.5V, R_{BIAS} = O/C to 3.05kΩ			0.2		µs
Fall time (90% to 10%)[5]	V_{CC} = 2.0V, V_{OUT} = 0.5V, R_{BIAS} = 3.05kΩ to O/C			0.2		µs
Propagation delay(low to high)[5]	V_{CC} = 2.0V, V_{OUT} = 0.5V, R_{BIAS} = O/C to 3.05kΩ			0.4		µs
Propagation delay(high to low)[5]	V_{CC} = 2.0V, V_{OUT} = 0.5V, R_{BIAS} = 3.05kΩ to O/C			0.2		µs

Notes:
2. R_{BIAS} connected to GND see Figure 1
3. All active output current measurements are pulsed tests of 8us duration, 10% duty cycle
4. See Typical Characteristics for a graph of Output current vs. R_{BIAS} value
5. See Figure 2

Figure 1: Application Circuit

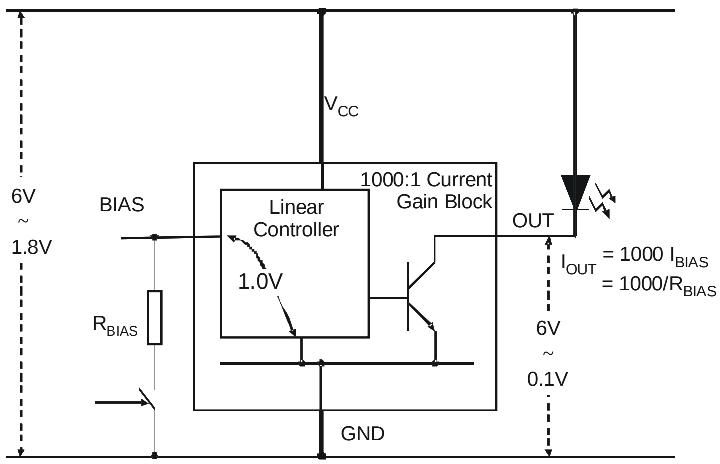
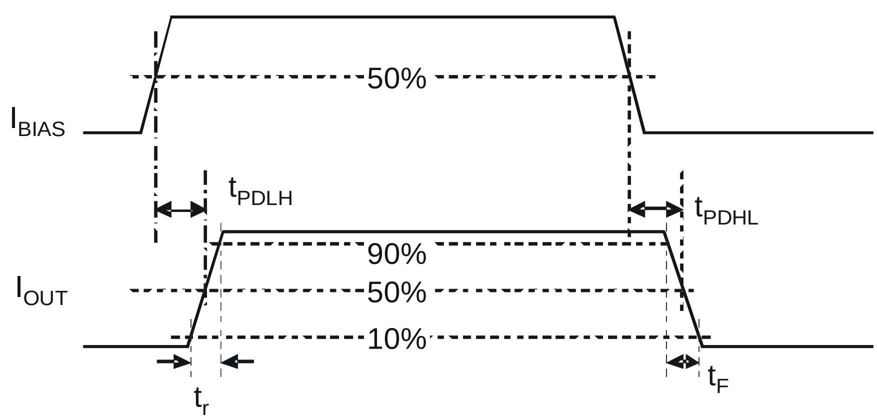


Figure 2: Timing Waveforms



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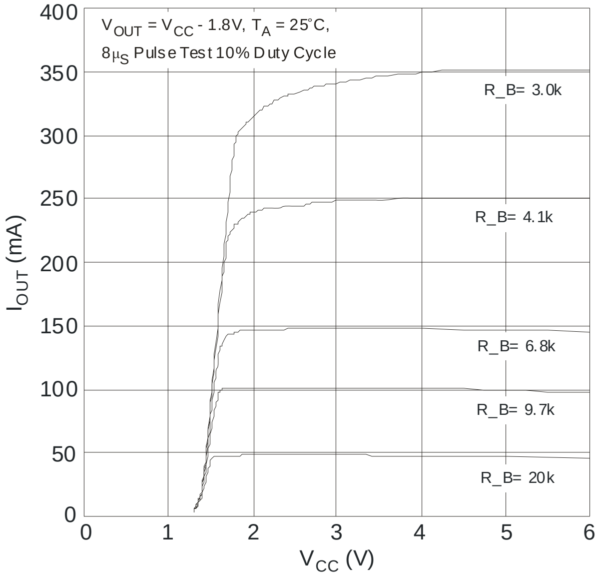
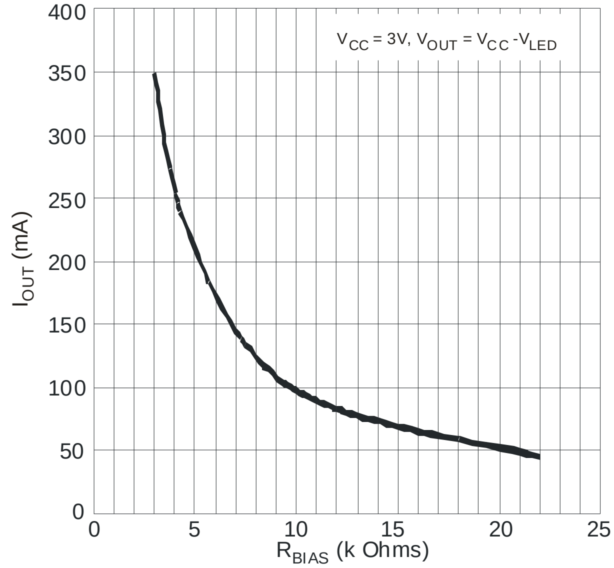
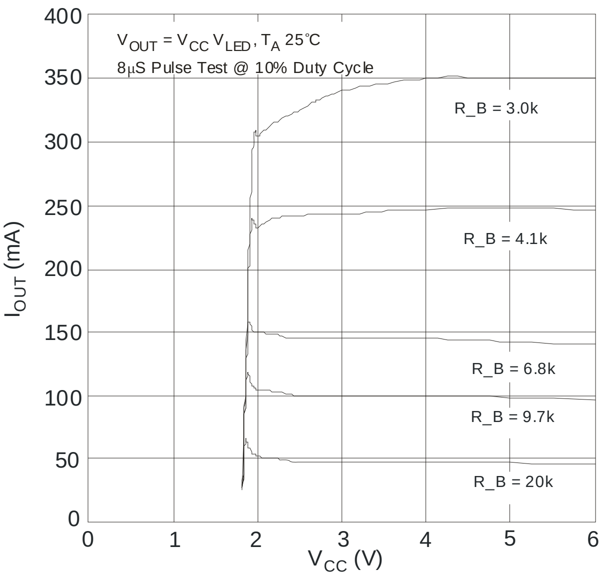
Typical Characteristics



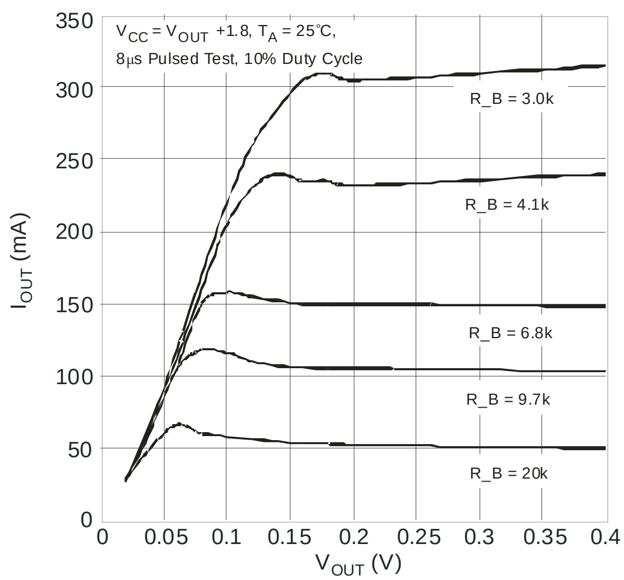
I_{OUT} vs. V_{CC}



I_{OUT} vs. R_{BIAS}

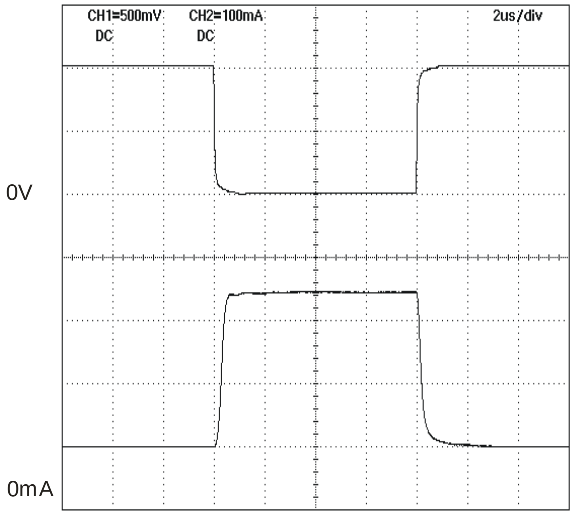


I_{OUT} vs. V_{CC}

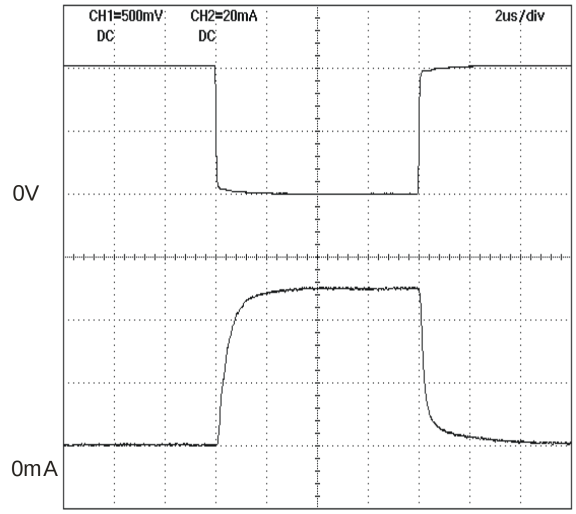


I_{OUT} vs. V_{CC}

Typical Characteristics (Cont.)



Channel 1 (Upper): V_Bias @ 0.5V/div Timebase: 2us/div
Channel 2 (Lower): I_Out @ 100mA/div
Pulse Response R_Bias 4.1k



Channel 1 (Upper): V_Bias @ 0.5V/div Timebase: 2us/div
Channel 2 (Lower): I_Out @ 20mA/div
Pulse Response R_Bias 21.0k

PIN Descriptions

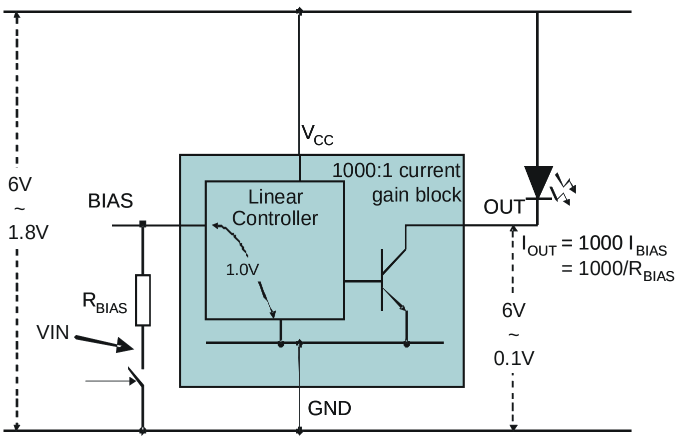
NAME	I/O	Pin #	FUNCTION
NC	-	1	No connection. May be grounded or left floating.
GND	Power	2	GND or the most negative terminal of the LED Driver. Also carries the LED return current.
BIAS	I	3	The output of an internal voltage reference (1.0V approx.). Connect a resistor R_{BIAS} from this pin to the external control input. The LED Driver amplifies the R_{BIAS} resistor current by a factor of nominally1000. Open circuiting this pin or driving this pin to >1.25V will turn off the output of the AP8804. Avoid unnecessary stray capacitance at this pin, and connect R_{BIAS} as close as possible to it.
V_{CC}	Power	4	The supply input pin of the LED Driver. This pin supplies the internal circuitry of the IC which is typically 80uA + 2.5% of the LED output current. It is advisable to decouple this pin with a 100nF capacitor to GND.
NC	-	5	No connection. May be grounded or left floating.
OUT	O	6	The output of the LED Driver, normally connected to the cathode of the LED. The normal working range of this pin is 0.1V (0.1V above GND pin potential) to 6V. It is permissible for the voltage on this pin to be higher than V_{CC}.

Applications Information

Setting the Output Current

The AP8804 is controlled by an input current at the BIAS pin. When an LED or load resistance is connected between a positive supply and OUT, the load current I_{OUT} is proportional to the input current at the BIAS input of the AP8804. The current gain, A_I is nominally -1000. The voltage at the BIAS pin is controlled to nominally +1.0V. The resistor R_{BIAS} sets the input current according to the input voltage, V_{IN}, as in Figure 3.

Figure 3



Therefore the input voltage, V_{IN} , determines the output current according to this equation:

$$I_{OUT} = A_I * (V_{IN} - V_{BIAS}) / R_{BIAS} \quad \text{if } V_{IN} \le V_{BIAS}$$

$$\text{and } I_{OUT} = 0 \quad \text{if } V_{IN} \ge V_{BIAS}$$

Note that these equations are approximate and a more accurate value of current can be found using the graph of I_{OUT} vs R_{BIAS}. Select R_{BIAS} to give the required I_{OUT}.

For example, if R_{BIAS} = 3k, an input of 0V will give an output current of nominally 350mA, while an input of about +1.1V or greater will give an output current equal to the leakage value which is typically less than1µA.

Driving the AP8804

The input current is approximately 1/R_{BIAS} when the driven end of R_{BIAS} is pulled to 0V or roughly output current divided by 1000. For a typical output current of up to about 300 mA, the input current will be 300µA or less. Hence a low level CMOS or open-drain logic drive level is convenient to turn the LED on (logic LOW, 0V) and off (logic HIGH, 1V or greater).

By connecting a switch to ground in series with R_{BIAS} (see figure 3) the device can be turned on and off. Typical applications for this include LED dimming as well as data interface applications.

An alternate way of turning the output of the AP8804 off is to drive the bias pin to greater than 1.1V. However direct drive to this pin is not recommended. Stray capacitance at the BIAS pin must be avoided for stability and the resistor R_{BIAS} should be placed close to the BIAS pin. The best method is to drive the input through the series resistor R_{BIAS} as shown from a CMOS or open drain logic signal.

Vcc pin quiescent current is typically 100uA and OUT pin leakage is typically less than 1uA when the device is turned off using the BIAS pin. BIAS pin controlled output switching times are less than 1us.

A further means of disabling the device is to turn off the supply to the Vcc pin. In this state, assuming the LED anode is still connected to the supply, the Vcc pin current is of course zero and the OUT pin leakage is typically less than 1nA. This method has the advantage of reducing the quiescent current from about 100µA to less than 1nA. When using this switching method, the time to settle to the desired current level may be several microseconds.

PCB Layout and Supply Conditioning

For a satisfactory pulse shape and AC stability, attention should be given to power supply decoupling. Connect a 0.1µF to 1µF X7R ceramic capacitor from Vcc to the common ground plane close to the Vcc pin. Position the capacitor close to the V_{CC} pin and use local vias to ground the capacitor. Additional ground vias should be placed as close as possible to the central paddle connection for the sake of both the pulse performance and thermal heat-sinking. The ground plane is also required to minimize undesired common-impedance coupling between input and output.

Excessive stray capacitance at the BIAS pin affects stability. It is sufficient to place the input bias resistor close to the BIAS pin to minimize the PCB trace capacitance to ground.

The AP8804 has been designed to drive the cathode of a low voltage LED which has the anode connected to the same node as V_{CC} pin. Alternatively the anode may be connected to a higher voltage than V_{CC} within the limits given. However best LED current regulation will be obtained when the anode is connected to V_{CC}.

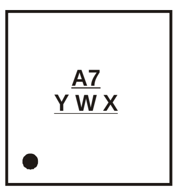
Power Dissipation and Operating Temperature

Although the performance of the AP8804 is not significantly affected by junction temperature, excessive power dissipation does affect the target output current. The typical variation of I_Out with power dissipation is approximately +0.065%/mW. A typical remote control application uses an NEC protocol data-burst with a low impedance 3V supply and 1.6V drop (at 250mA) across the LED load. Under these conditions, the power dissipation related error in I_Out will be approximately 3% average during the burst.

Ordering Information

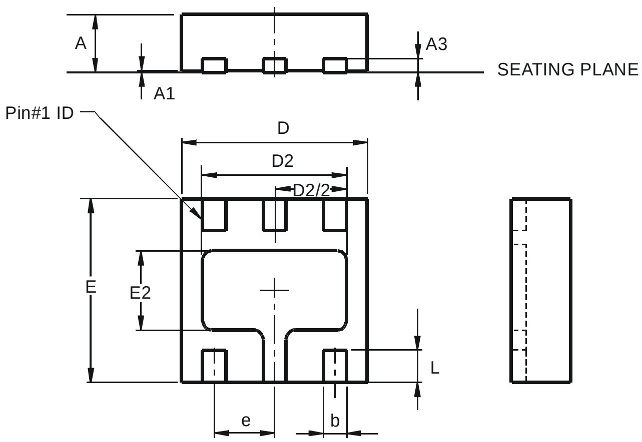
Device	Package Code	Packaging	7"/13" Tape and Reel	
			Quantity	Part Number Suffix
AP8804SNG-7	SN	DFN2020-6	3000/ Tape & Reel	-7

Marking Information



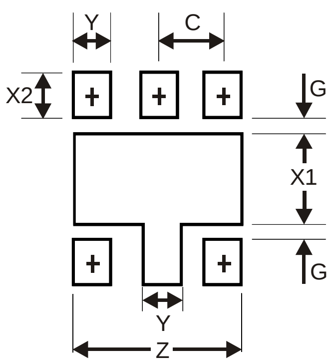
A7 = Product Type Marking Code
Y = Year 0 ~ 9
W = Week: A ~ Z : 1 ~ 26 Week;
a ~ z : 27 ~ 52 week;
z represents 52 and 53 week

Package Outline Dimensions



DFN2020-6			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0	0.05	0.03
A3	—	—	0.15
b	0.20	0.30	0.25
D	1.95	2.075	2.00
D2	1.45	1.65	1.55
e	—	—	0.65
E	1.95	2.075	2.00
E2	0.76	0.96	0.86
L	0.30	0.40	0.35
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
Z	1.67
G	0.15
X1	0.90
X2	0.45
Y	0.37
C	0.65

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