

**-20V, -4A, 42mΩ, 2.0W, DFN3x3, P-MOSFET**

**Descriptions**

This single P-Channel MOSFET is produced using trench process that provides minimum on resistance performance. WPM2009D is enhancement power MOSFET with 2.0W power dissipation mounting 1 in<sup>2</sup> pad in a DFN3x3 package. This device is suited for high power charging circuit of mobile phone application. It also can be used in a high power switching application.

**Features**

- Max Rds(on) 42mΩ @ Vgs=-4.5V
- Max Vds -20V
- Max Current -4.0A
- Typical Vgs(th) -0.65V @ Id=-250uA
- Power Dissipation 2.0W (Note2)
- High performance Trench process
- DFN3x3-8L Package
- Pb-Free

**Applications**

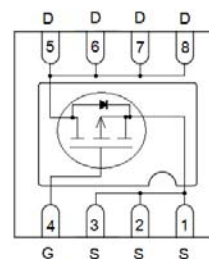
- Battery charging
- Load Switch
- Power Switch
- DC-DC converter

Bottom



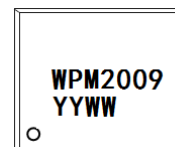
**DFN3x3-8L**

Bottom



**Pin Connection**

Top



WPM2009 = Part Number  
 YY = Year  
 WW = Week

**Marking**

**Order Information**

Device	Package	Shipping
WPM2009D-8/TR	DFN3x3-8L	3000/Tape&Reel

### Maximum Ratings

( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

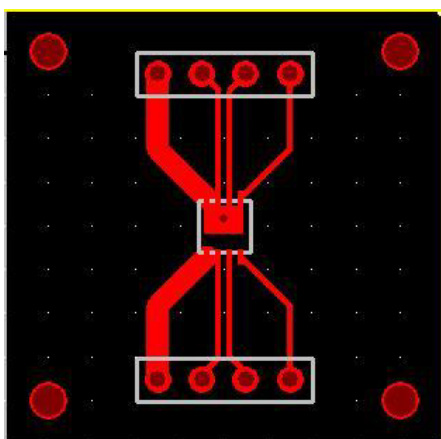
Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain-to-Source Voltage	-20	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 12$	V
$I_D$	Drain Current – Continue <b>Note1</b>	-4.0	A
	Drain Current – Continue (t<5s) <b>Note1</b>	-4.9	A
	Drain Current – Continue <b>Note2</b>	-6.5	A
	Drain Current – Pulsed (t<300us, Duty<2%) <b>Note2</b>	-24	A
$P_D$	Power Dissipation – <b>Note1</b>	1.0	W
	Power Dissipation – (t<5s) <b>Note1</b>	1.5	W
	Power Dissipation – <b>Note2</b>	2.0	W
$T_J$	Operation junction temperature range	150	$^{\circ}\text{C}$
$T_{SG}$	Storage temperature range	-55~150	$^{\circ}\text{C}$

### Thermal Resistance Ratings

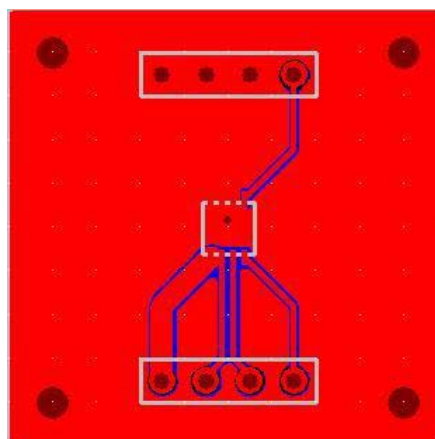
Symbol	Parameter	Max.	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient – <b>Note1</b>	125	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient – <b>Note2</b>	62	$^{\circ}\text{C}/\text{W}$

**Note1:** Surface mounted on a 2 oz copper, recommend minimum pad, FR-4 board.

**Note2:** Surface mounted on a 2 oz copper, 1 in<sup>2</sup> pad with dual side, FR-4 board.



Note1



Note2

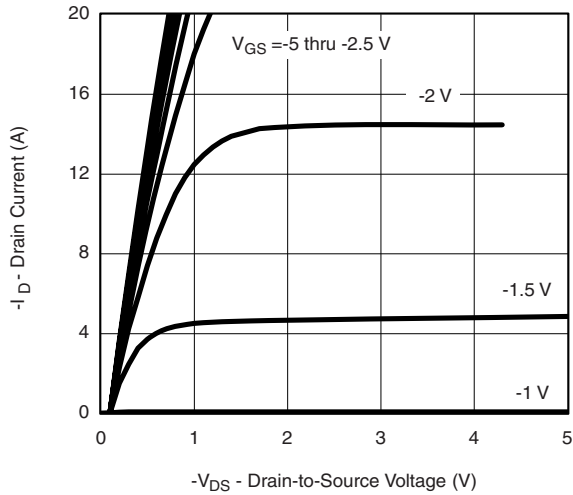
**Electronics Characteristics**

 ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

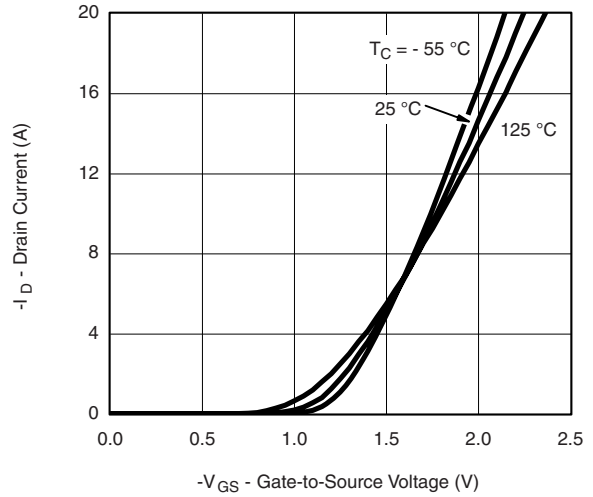
Symbol	Parameter	Test Condition	Min	Typ.	Max	Unit
<b>Off Characteristics</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250A$	-20			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-16V, V_{GS}=0V$			-1.0	$\mu\text{A}$
$I_{GSS}$	Gate –Source leakage current	$V_{GS}=\pm 12V, V_{DS}=0V$			$\pm 100$	nA
<b>ON Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250A$	-0.35	-0.65	-1.00	V
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=-4.5V, I_D=-4.0A$		42	59	$\text{m}\Omega$
		$V_{GS}=-2.5V, I_D=-3.5A$		54	74	$\text{m}\Omega$
		$V_{GS}=-1.8V, I_D=-3.0A$		77	93	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=-5V, I_D=-3.3A$		3.0		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=-6V, V_{GS}=0V,$ $F=1.0\text{ MHz}$	700	850	1000	pF
$C_{oss}$	Output Capacitance		100	150	200	pF
$C_{rss}$	Reverse Transfer Capacitance		80	120	150	pF
$Q_{G(TOT)}$	Total Gate Charge	$V_{DS}=-6V, I_D=-3.3A,$ $V_{GS}=-4.5V$	8	12	15	nC
$Q_{G(TH)}$	Threshold gate charge		0.4	0.6	0.8	nC
$Q_{GS}$	Gate-Source Charge		1.2	1.6	2.0	nC
$Q_{GD}$	Gate-Drain Charge		1.8	2.2	2.6	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{GS}=-4.5V, V_{DS}=-6V,$ $I_D = -1.0A, R_G=6.0\Omega$	15	19	25	ns
$t_r$	Turn-On Rise Time		5	8	15	ns
$t_{d(off)}$	Turn-Off Delay Time		80	100	120	ns
$t_f$	Turn-Off Fall Time		15	25	35	ns
<b>Drain-to-Source Diode Characteristics</b>						
$V_{SD}$	Forward Diode Voltage	$V_{GS}=0V, I_S=-1.6A$		-0.7		V

**Typical Performance Graph**

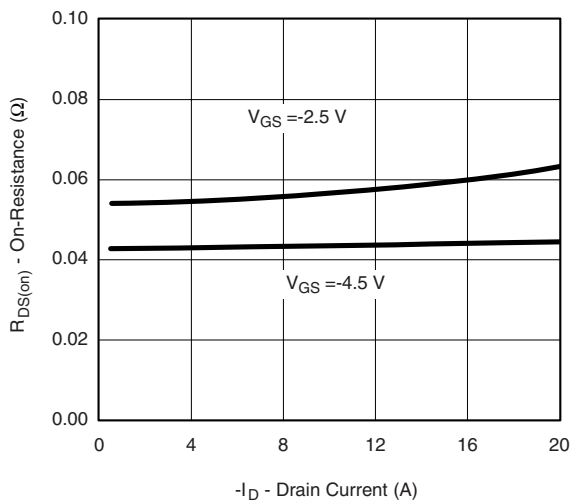
( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



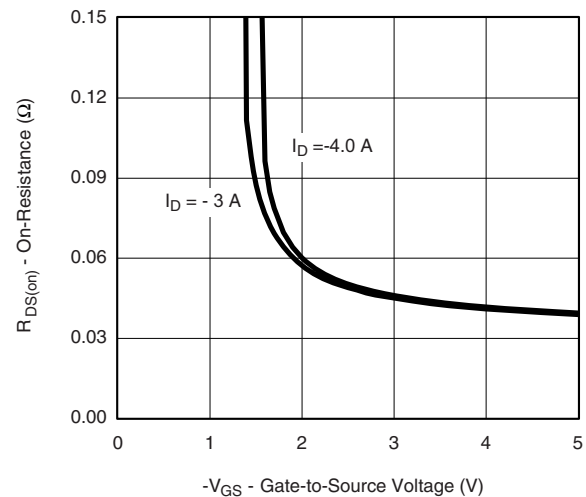
**Output Characteristics**



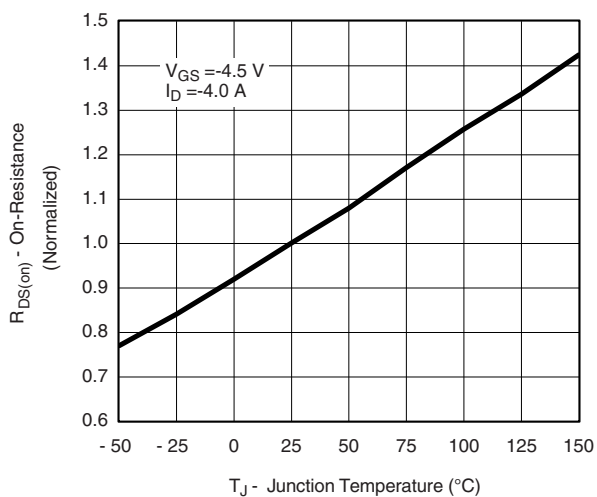
**Transfer Characteristics**



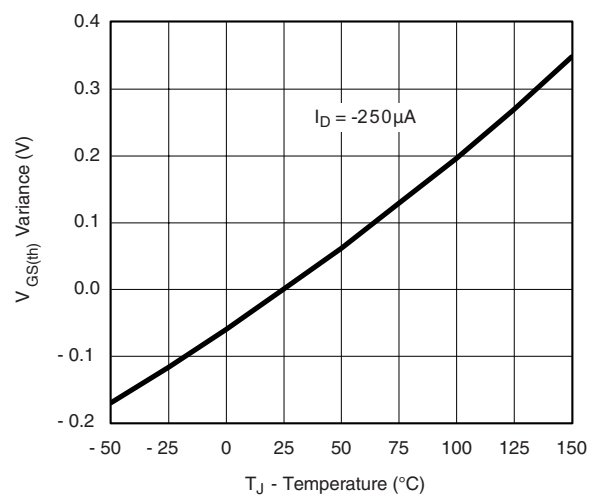
**On-Resistance vs. Drain Current**



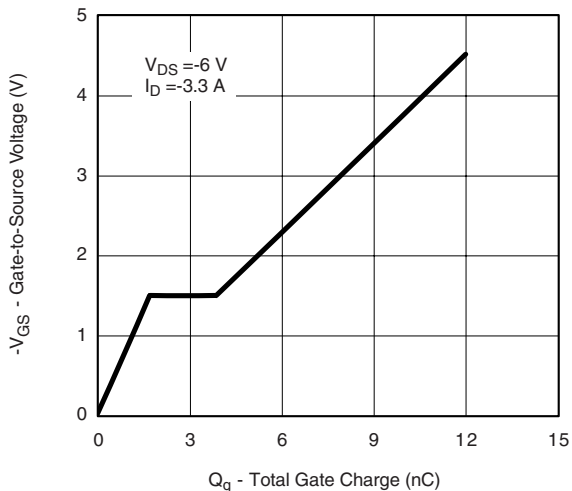
**On-Resistance vs. Gate-to-Source Voltage**



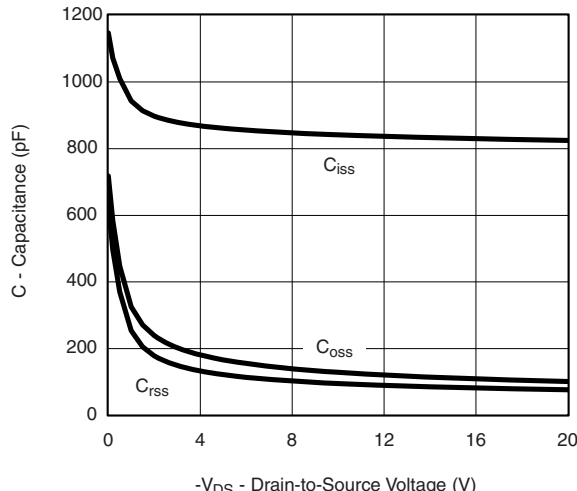
**On-Resistance vs. Junction Temperature**



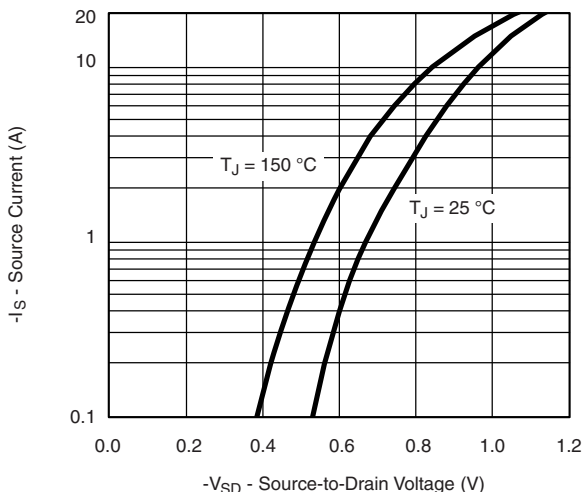
**Threshold Voltage**



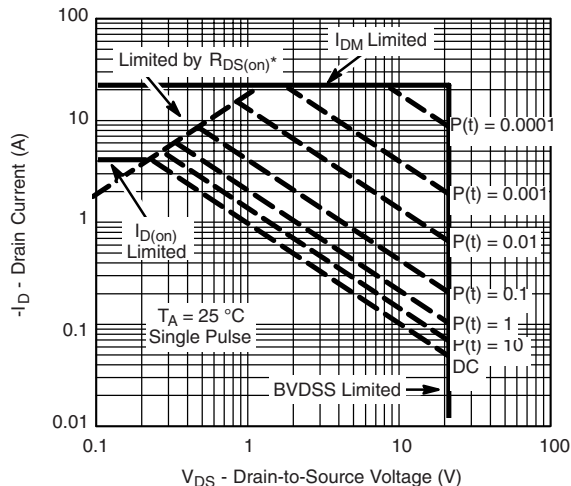
Gate Charge



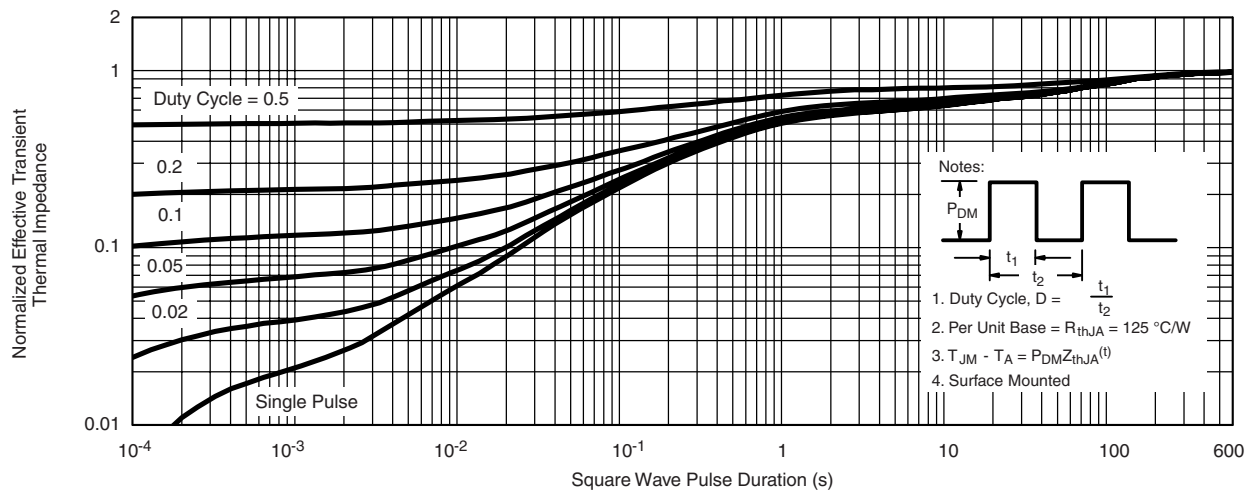
Capacitance

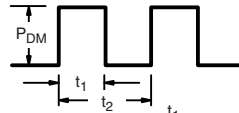


Source-Drain Diode Forward Voltage



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified  
Safe Operating Area

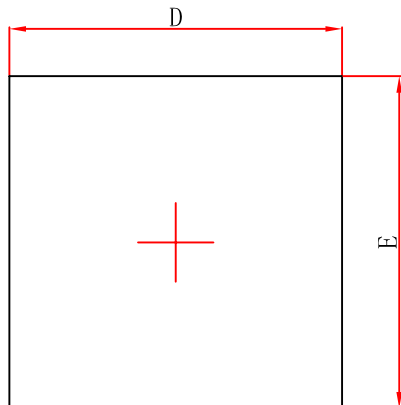


- Notes:
- 
- Duty Cycle,  $D = \frac{t_1}{t_2}$
  - Per Unit Base =  $R_{thJA} = 125\text{ }^\circ\text{C/W}$
  - $T_{JM} - T_A = P_{DM} Z_{thJA}(t)$
  - Surface Mounted

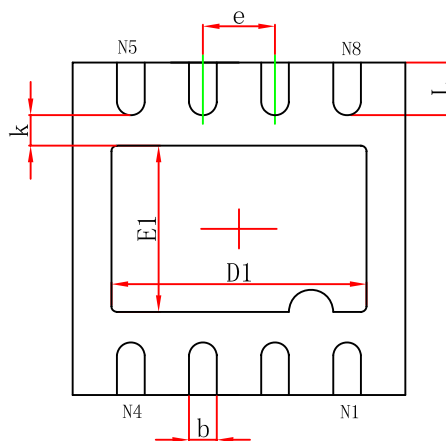
Normalized Thermal Transient Impedance, Junction-to-Ambient

Package Outline Dimension

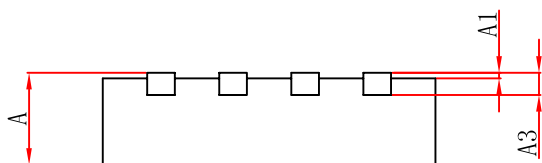
DFN3x3-8L



Top View



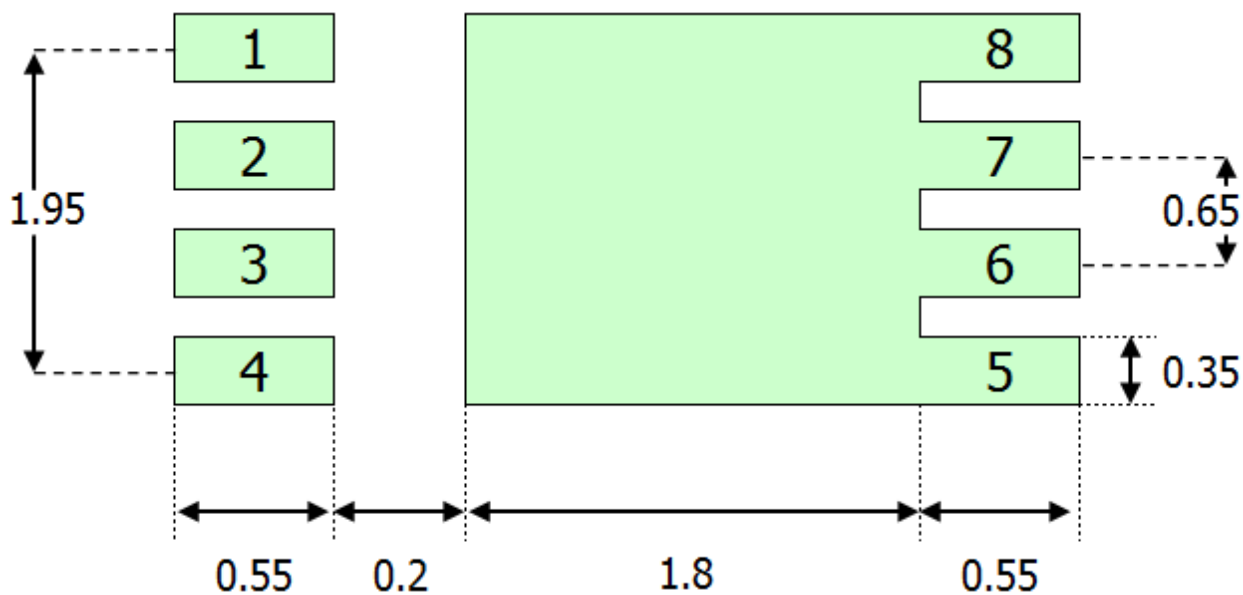
Bottom View



Side View

Symbol	Dimensions in millimeters	
	Min.	Max.
A	0.7	0.8
A1	0.00	0.05
A3	0.203 Ref.	
D	2.9	3.1
E	2.9	3.1
D1	2.2	2.4
E1	1.4	1.6
k	0.200 Min.	
b	0.18	0.3
e	0.650 Typ.	
L	0.375	0.575

PCB Layout Guide



Recommend Minimum Pad Guide  
Unit: mm