VTC Inc.
Value the Customer™

VM311R

8-CHANNEL, FERRITE HEAD READ/WRITE PREAMPLIFIER

July, 1992

FEATURES

- Enhanced System Write to Read Recovery Time
- Power-Up/Power-Down Write Protection
- Operates on +5V and +12V Power Supplies
- Write-Unsafe Detection Circuitry
- Programmable Write-Current Source
- Low Input Noise of 1.4nV/ $\sqrt{Hz}$ maximum
- For Use With Center-Tapped Ferrite or MIG Heads
- Internal Head Damping Resistors
- Available in 4, 6, or 8 Channels

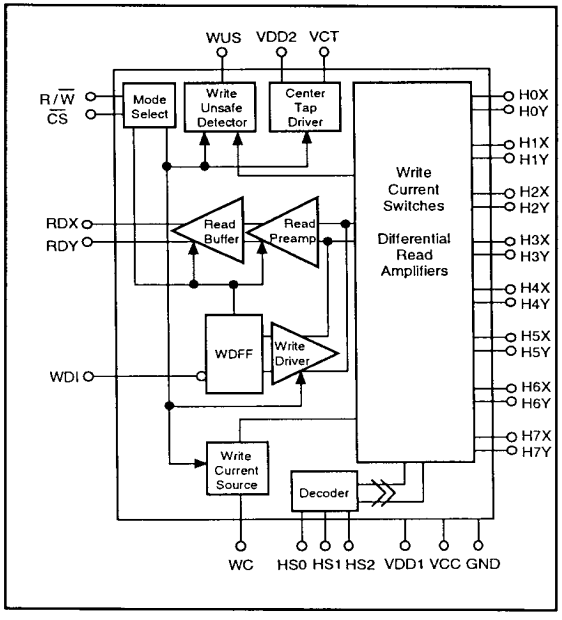
DESCRIPTION

The VM311R is a bipolar, monolithic read/write preamp circuit, designed for use with center-tapped ferrite or MIG recording heads. The circuit provides a low-noise read data path for signals from the disk in the read mode and provides write-current control for data written on the disk in the write mode.

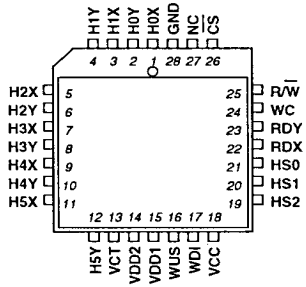
The write-to-read recovery should be enhanced when doing a DC erase. Layout of the chip minimizes thermal effects on the read amp for improved write-to-read recovery. Also, the write unsafe circuit has a much larger inductance range and is not dependent on the magnitude of Iw. This part will serve a wider range of head loads and write current values.

The VM311R is available in a variety of package styles, please consult factory for availability.

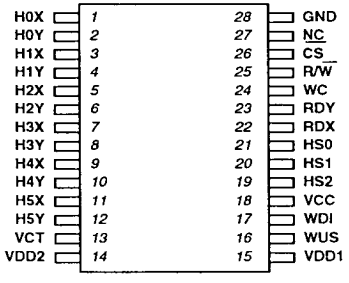
BLOCK DIAGRAM



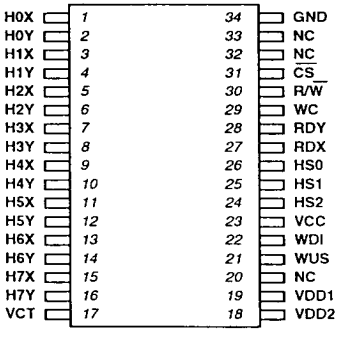
CONNECTION DIAGRAMS



6-Channel
28-lead PLCC
VM311R6PLJ



6-Channel
28-lead SOIC
VM311R6POJ



8-Channel
34-lead SOIC
VM311R8PO34J

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD1} ..... -0.3V to 14V
- V_{DD2} ..... -0.3V to 14V
- V_{CC} ..... -0.3V to 6V

Pin Voltages:
- Head Select (HS) ..... -0.3V to V_{CC} + 0.3V
- Write Unsafe (WUS) ..... -0.3V to V_{CC} + 0.3V
- Write Data Input (WDI) ..... -0.3V to V_{CC} + 0.3V
- Read/Write Select (R/W) ..... -0.3V to V_{CC} + 0.3V

Output Current:
- Write Current (I_W) 60mA
- Read Data (RDX, RDY) 10mA
- Center Tap Current (I_{CT}) 60mA
- Write Unsafe (WUS) 12mA

Operating Temperature Range ..... 0° to 70°C
Storage Temperature Range ..... -65° to 150°C
Lead Temperature (Soldering 60 Sec.) ..... 300°C
Junction Temperature ..... 150°C
Thermal Characteristics:
- 28-lead SOIC ..... 70°C/W
- 28-lead PLCC ..... 65°C/W
- 34-lead SOIC ..... 60°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD1} ..... 12V ± 10%
- V_{DD2} ..... 7.0V to VDD1
- V_{CC} ..... 5V ± 10%

Head Inductance (L_H) ..... 2.5 - 15µH
Damping Resistance (R_D on chip ..... 750Ω ± 20%
R_{CT} Resistor (Note 2) .....120Ω ± 5%
RDX,RDY Output Current (Read Mode) ..... 0 to 2mA
Write Current ..... 10 to 50mA
Junction Temperature ..... 25° to +125°C

Note 1: Resistor (R_{CT}) used to limit power dissipation.

CIRCUIT OPERATION

The VM311R addresses up to eight center-tapped ferrite heads and operates as a write-current switch in the write mode and as a low-noise differential amplifier in the read mode. Head selection is controlled by HS0, HS1 and HS2 lines and mode select is controlled by the $\overline{CS}$ and R/$\overline{W}$ select lines as shown in Tables 1 and 2. Both $\overline{CS}$ and R/$\overline{W}$ have internal pull-up resistors to prevent accidental write condition. Unsafe conditions are indicated by the WUS line.

Write Mode

In the write mode, the VM311R operates as a write-current switch. Write current is supplied by an internal current source. The magnitude of the write current is determined by an external resistor connected between WC and ground. The head current is switched between the X and Y side of a selected head by falling transitions on WDI (write data input). When switching to the write mode from the read mode, the write data flip-flop is initialized to pass head current through the X side of the head.

The write unsafe (WUS), open collector output, will give a high level for any of the following unsafe conditions:

- Open Head
- No Write Current
- Read Mode
- Idle Mode
- Write Data Frequency Too Low
- Head Center-Tap Open

After the fault condition is corrected, it takes two negative transitions on WDI to clear the WUS line. To further protect accidental writing to the disk, a voltage fault detection circuit ensures no write current during power loss or power sequencing. An enhanced write to read recovery time is achieved by maintaining a constant common mode level on the RDX, RDY outputs between write and read modes.

Write mode power dissipation may be minimized by connecting a resistor (R_{CT}) between V_{DD2} and V_{DD1}. The optimum value for R_{CT} is 120x40/Iw (Iw in mA). At write currents below 15mA, the read mode dissipation is higher than write mode and need not be used. In this case V_{DD2} is connected to V_{DD1}.

Read Mode

In the read mode the circuit operates as a low-noise differential amplifier. The write-current source is turned off and the write-data flip-flop is set. The selected head provides a differential input. The RDX and RDY pins provide differential emitter follower outputs which are in phase with the X and Y inputs and should be AC coupled to the load. Write current is deactivated for both the read and idle mode so that external gating is not required.

Idle Mode

In the idle mode ($\overline{CS}$ = high level) both the read amp and write driver are disabled and the device's power dissipation is minimal. The internal write current reference is disabled and the RDX, RDY outputs are in a high impedance state. For multiply chip usage, the RDX, RDY outputs may be wire OR'ed, and a common write current resistor (R_{WC}) may be used to set the write current.

Table 1: Head Select

HS0	HS1	HS2	HEAD
L	L	L	0
H	L	L	1
L	H	L	2
H	H	L	3
L	L	H	4
H	L	H	5
L	H	H	6
H	H	H	7

Table 2: Mode Select

$\overline{CS}$	$R/\overline{W}$	MODE
L	L	Write
L	H	Read
H	X	Idle

Table 3: External Resistor vs. Write Current

External resistor vs. DC write current I_W into the selected head terminal X or Y with V_{CT} shorted only to the respective X or Y terminal.	
External Resistor R_{WC} (Ω)	Write Current I_W (mA)
249	10
124	20
82.5	30
61.9	40

Note: Effective current I_{FLUX} generated in the magnetic head is related to I_W by the expression:

$$I_{FLUX} = I_W\left(\frac{R_D}{R_H + R_D}\right)$$

Where R_H equals the full coil resistance of a center-tapped ferrite head and R_D is the damping resistor connected internally or externally between the X and Y terminals. Nominal internal resistance on VM311R is 750Ω.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select Inputs
$\overline{CS}$	I	Chip Select: a low level enables device
$R/\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative edge toggles the head current
H0X-H7X H0Y-H7Y	I/O	X,Y head connections
RDX, RDY	O*	X,Y Read Data: diff. read signal outputs
WC		Write Current: used to set the magnitude of the write current
VCT		Voltage Center Tap: voltage source for head center tap
VCC		+5 V
VDD1		+12 V
VDD2		Positive power supply for the center tap voltage source
GND		Ground

** For multiple chip usage, these signals can be wire OR'ed*

DC CHARACTERISTICS Unless otherwise specified, V_{DD1} = 12V ±10%, V_{CC1} = V_{CC2} = 5V ±10%, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
POWER SUPPLY						
Positive Supply Current	I_{DD}	Read Mode		19	25	mA
		Write Mode		9 + I_W	12 + I_W	
		Idle Mode		9	12	
	I_{CC}	Read Mode		11	15	mA
		Write Mode		13	18	
		Idle Mode		9	12	
Power Dissipation T_A = 70°C	P_D	Idle Mode			200	mW
		Read Mode			425	
		Write Mode I_W = 40mA, R_{CT} = 120Ω			500	
		Write Mode I_W = 40mA, R_{CT} = 0Ω			675	
DIGITAL TTL INPUTS: $\overline{CS}$, R/$\overline{W}$, HS, WDI						
Input High Voltage	V_{IH}		2		V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		-0.3		0.8	V
Input High Current	I_{IH}	V_{IH} = 2.0V, V_{CC} = 5.5V	-400		100	µA
Input Low Current	I_{IL}	V_{IL} = 0.4V, V_{CC} = 5.5V	-0.4			mA
WUS OUTPUT						
Low Voltage	V_{OL}	I_{OL} = 8 mA (Safe)			0.5	V
High Current	I_{OH}	V_{OH} = 5V (Unsafe)			100	µA

READ CHARACTERISTICS Unless otherwise specified, I_W = 40mA, L_H = 2.5µH, R_D = 750Ω, f_{DATA} = 5MHz, C_L (RDX, RDY) ≤ 20pF, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, f = 500KHz R_L (RDX,RDY) = 1kΩ	85		115	V/V
Dynamic Range	DR	DC input voltage where AC gain falls 10%, $V_{IN} = V_{DC}$ + 0.5mVp-p f = 500KHz	-3	1.0	3	mV
Bandwidth (- 3dB)	BW	V_{IN} =1 mVp-p, Z_S < 5Ω	30			MHz
Input Noise Voltage	e_{in}	L_H = 0, R_H = 0, BW = 15MHz			1.4	nV/√Hz
Differential Input Capacitance	C_{IN}	f = 5MHz			20	pF
Differential Input Resistance	R_{IN}	VM311R, f = 5MHz	460		860	Ω
Input Current (per side)	I_{IN}				80	µA
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{CT}$ + 100mVp-p, f = 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	V_{DD} or V_{CC} = 100mVp-p, f = 5MHz	45			dB
Channel Separation	CS	V_{IN} = 100mVp-p, f = 5MHz Three channels driven, selected channel measured	45			dB
Output Offset Voltage	V_{OS}		-200		200	mV
Common Mode Output Voltage	V_{OCM}		4.5		6.5	V
Head Center Tap Voltage	V_{CT}	Read Mode		4.2		V
Single-Ended Output Resistance	R_{SEO}				30	Ω
Output Current	I_{OUT}	AC coupled load, RDX, RDY	2.1			mA
Channel Separation	CS	Read or Idle Mode 0V ≤ V_{CC} ≤ 5.5V 0 ≤ V_{DD1} ≤ 13.2V	-200		200	µA

WRITE CHARACTERISTICS Unless otherwise specified, I_W = 40mA, L_H = 2.5µH, R_D = 750Ω, f_{DATA} = 5MHz, C_L (RDX, RDY) ≤ 20pF, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write Current Range	I_W	(See table 3)	10		40	mA
Write Current Tolerance	ΔI_W	Over I_W range	-5		+5	%
Differential Head Voltage	V_{DH}		7			Vp-p
Current Gain	A_I			.99		mA/mA
Unselected Head Current	I_{UH}				2	mA p-p
Head Current Propagation Delay	t_{PD}	L_H = 0µH, R_H = 0, 50% WDI to 50% I_W			30	ns
Rise/Fall Time	$t_r - t_f$	L_H = 0µH, R_H = 0, 10% to 90%	5		20	ns
Symmetry	S	$[(t_r - t_f)/2]$			2	ns
Differential Output Resistance	R_{OUT}	VM311R	600		960	Ω
Differential Output Capacitance	C_{OUT}	f = 5MHz			15	pF
WDI Transition Frequency	f_{min}	WUS = low	250			KHz
Center Tap Voltage	V_{CT}	Write Mode		6.6		V
Head Current (per side)	I_H	Write Mode; $0 \le V_{CC} \le 3.7V$; $0 \le V_{DD1} \le 8.7V$	-200		200	µA
RDX,RDY Output Offset Voltage	V_{OS}	Write or Idle Mode	-20		20	mV
RDX, RDY Common Mode Output Voltage	V_{CM}	Write or Idle Mode		5.3		V
RDX, RDY Leakage	I_L	RDX, RDY = 6V, Write or Idle Mode	-100		100	µA
Unselected Leakage Current	I_{UH}				85	µA

SWITCHING CHARACTERISTICS Unless otherwise specified, I_W = 40mA, L_H = 2.5µH, R_D = 750Ω, f_{DATA} = 5MHz, C_L (RDX, RDY) ≤ 20pF, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Read-to-Write Switching Delay	t_{RW}	50% of R/$\overline{W}$ to 90% of write output envelope			1	µs
Write-to-Read Switching Delay	t_{WR}	50% of R/$\overline{W}$ to 90% of 100mVp-p RDX, RDY envelope			1	µs
Idle-to-Write Switching Delay	t_{IW}	50% of $\overline{CS}$ to 90% of write output envelope			1	µs
Idle-to-Read Switching Delay	t_{IR}	50% of $\overline{CS}$ to 90% of 100mVp-p RDX, RDY envelope			1	µs
Write-to-Idle Switching Delay	t_{WI}	50% of $\overline{CS}$ to 10% of write output envelope			1	µs
Read-to-Idle Switching Delay	t_{RI}	50% of $\overline{CS}$ to 10% of RDX, RDY envelope			1	µs
Head Select Switching Delay	t_{HS}	50% of HS transition to 90% of 100mVp-p RDX, RDY envelope from selected head			1	µs
Write Unsafe Delay Safe to Unsafe	t_{D1}	Gate WDI. Measure from 50% of last data pulse to 50% WUS. I_W = 10 to 40mA	1.6		8	µs
Write Unsafe Delay Unsafe to Safe	t_{D2}	Gate WDI. Measure from 50% of falling edge of first data pulse to 50% WUS, I_W =10mA			1	µs

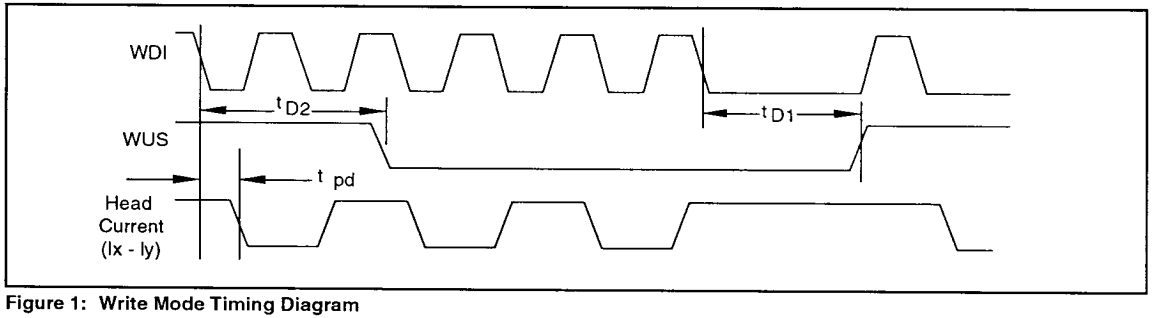


Figure 1: Write Mode Timing Diagram