TSM 2301A

SOT-23

Pin Definition:
1. Gate
2. Source
3. Drain

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
-20	130 @ V_{GS} =-4.5V	-2.8
	190 @ V_{GS} =-2.5V	-2.0

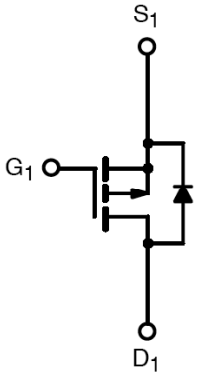
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Battery Management
- High Speed Switch

Block Diagram



P-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM2301ACX RFG	SOT-23	3Kpcs / 7" Reel

Note: "G" denotes Halogen Free Product.

Absolute Maximum Rating (T_A=25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current		I_D	-2.8	A
Pulsed Drain Current		I_{DM}	-10	A
Continuous Source Current (Diode Conduction)[a,b]		I_S	-1	A
Maximum Power Dissipation	T_A=25°C	P_D	0.7	W
	T_A=70°C		0.45	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	175	°C/W

Notes:

a. Pulse width limited by the Maximum junction temperature

b. Surface Mounted on a 1 in^2 pad of 2oz Cu, t ≤ 10 sec.

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Electrical Specifications (Ta = 25°C unless otherwise noted)

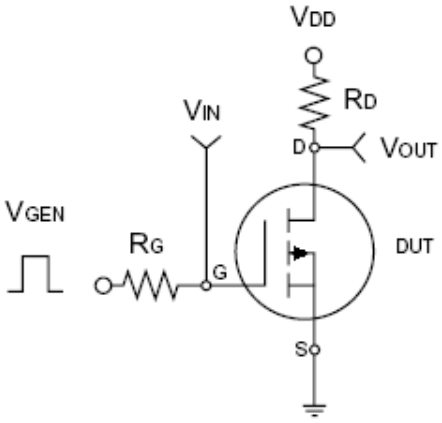
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	-20	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	$V_{GS(TH)}$	-0.6	-0.7	-1	V
Gate Body Leakage	V_{GS} = ±12V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = -20V, V_{GS} = 0V	I_{DSS}	--	--	1.0	μA
Drain-Source On-State Resistance	V_{GS} = -4.5V, I_D = -2.8A	$R_{DS(ON)}$	--	90	130	mΩ
	V_{GS} = -2.5V, I_D = -2.0A		--	120	190	
Diode Forward Voltage	I_S = -1A, V_{GS} = 0V	V_{SD}	--	-0.7	-1.3	V
Dynamic[b]						
Gate Resistance	V_{GS} = V_{DS} =0V, f=1MHz	R_g	--	7.5	--	Ω
Total Gate Charge	V_{DS} = -6V, I_D = -2.8A, V_{GS} = -4.5V	Q_g	--	7.2	--	nC
Gate-Source Charge		Q_{gs}	--	2.2	--	
Gate-Drain Charge		Q_{gd}	--	1.2	--	
Input Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	480	--	pF
Output Capacitance		C_{oss}	--	460	--	
Reverse Transfer Capacitance		C_{rss}	--	10	--	
Switching[b,c]						
Turn-On Delay Time	V_{DD} = -6V, R_L = 6Ω, V_{GEN} = -4.5V, R_G = 6Ω	$t_{d(on)}$	--	38	--	nS
Turn-On Rise Time		t_r	--	25	--	
Turn-Off Delay Time		$t_{d(off)}$	--	43	--	
Turn-Off Fall Time		t_f	--	5	--	

Notes:

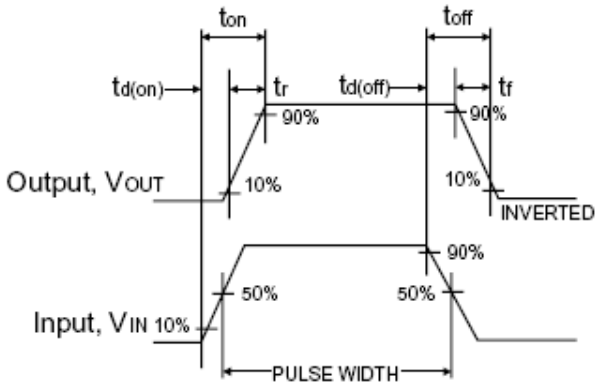
a. pulse test: PW ≤300μS, duty cycle ≤2%

b. For DESIGN AID ONLY, not subject to production testing.

c. Switching time is essentially independent of operating temperature.



Switching Test Circuit



Switchin Waveforms