



# PHC21025

## Complementary intermediate level FET

Rev. 04 — 17 March 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Intermediate level N-channel and P-channel complementary pair enhancement mode Field-Effect Transistor (FET) in a plastic package using vertical D-MOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

### 1.3 Applications

- Motor and actuator drivers
- Synchronized rectification
- Power management

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C};$ N-channel	-	-	30	V
		$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C};$ P-channel	-	-	-30	V
$I_D$	drain current	$T_{sp} \leq 80\text{ °C};$ P-channel	-	-	-2.3	A
		$T_{sp} \leq 80\text{ °C};$ N-channel	-	-	3.5	A
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[1]	-	1	W

#### Static characteristics

$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -1\text{ A};$ $T_j = 25\text{ °C};$ P-channel; see <a href="#">Figure 16</a> ; see <a href="#">Figure 19</a>	-	0.22	0.25	$\Omega$
		$V_{GS} = 10\text{ V}; I_D = 2.2\text{ A};$ $T_j = 25\text{ °C};$ N-channel; see <a href="#">Figure 15</a> ; see <a href="#">Figure 18</a>	-	0.08	0.1	$\Omega$



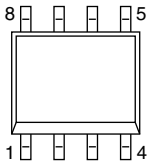
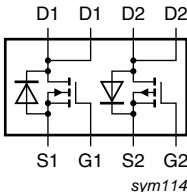
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = -10 V; I <sub>D</sub> = -2.3 A; V <sub>DS</sub> = -15 V; T <sub>j</sub> = 25 °C; P-channel; see <a href="#">Figure 12</a>	-	3	-	nC
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 2.3 A; V <sub>DS</sub> = 15 V; T <sub>j</sub> = 25 °C; N-channel; see <a href="#">Figure 11</a>	-	2.5	-	nC

[1] Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with a thermal resistance from ambient to solder point of 90 K/W.

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>SOT96-1 (SO8)</p>	 <p>sym114</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHC21025	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 150 °C; N-channel	-	30	V	
		T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 150 °C; P-channel	-	-30	V	
V <sub>GS</sub>	gate-source voltage		-	-	V	
V <sub>GSO</sub>	gate-source voltage	open drain	-20	20	V	
I <sub>D</sub>	drain current	T <sub>sp</sub> ≤ 80 °C; P-channel	-	-2.3	A	
		T <sub>sp</sub> ≤ 80 °C; N-channel	-	3.5	A	
I <sub>DM</sub>	peak drain current	T <sub>sp</sub> = 25 °C; pulsed; N-channel; see <a href="#">Figure 2</a>	[1]	-	14	A
		T <sub>sp</sub> = 25 °C; pulsed; P-channel; see <a href="#">Figure 3</a>	[1]	-	-10	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	1	W
		T <sub>sp</sub> = 80 °C; see <a href="#">Figure 1</a>	[3]	-	2	W
		T <sub>amb</sub> = 25 °C	[4]	-	1.3	W
			[5]	-	2	W
T <sub>stg</sub>	storage temperature		-65	150	°C	
T <sub>j</sub>	junction temperature		-	150	°C	
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>sp</sub> ≤ 80 °C; P-channel	-	-1.25	A	
		T <sub>sp</sub> ≤ 80 °C; N-channel	-	1.5	A	
I <sub>SM</sub>	peak source current	T <sub>sp</sub> = 25 °C; pulsed; P-channel	[6]	-	-5	A
		T <sub>sp</sub> = 25 °C; pulsed; N-channel	[6]	-	6	A

[1] Pulse width and duty cycle limited by maximum junction temperature.

[2] Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with a thermal resistance from ambient to solder point of 90 K/W.

[3] Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.

[4] Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with thermal resistance from ambient to solder point of 90 K/W.

[5] Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with a Thermal resistance from ambient to solder point of 27.5 K/W.

[6] Pulse width and duty cycle limited by maximum junction temperature.

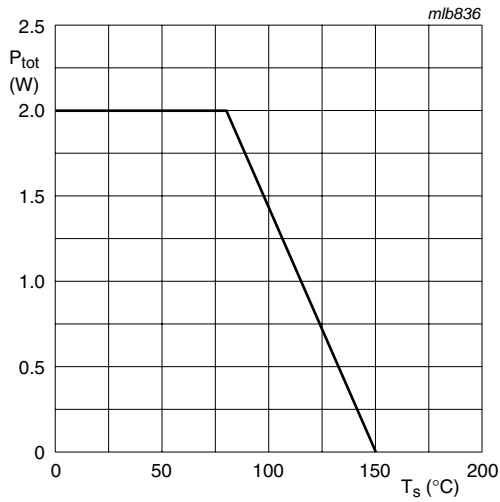
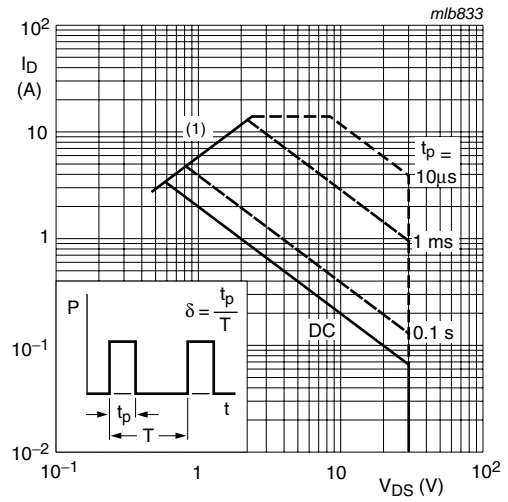
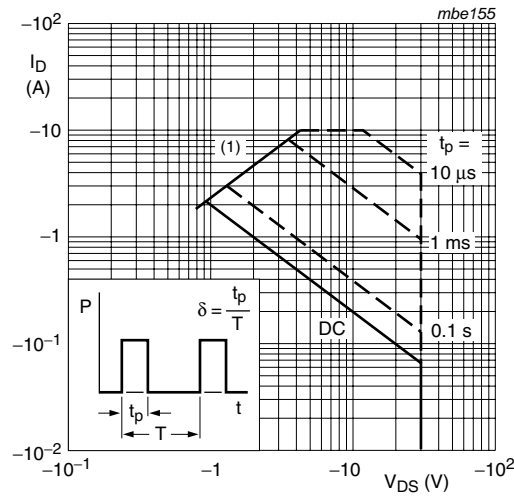


Fig 1. Power derating curve



$\delta = 0.01$ .  
 $T_s = 80\text{ }^\circ\text{C}$ .  
 (1)  $R_{DSon}$  limitation.

Fig 2. SOAR; N-channel



$\delta = 0.01$   
 $T_s = 80\text{ }^\circ\text{C}$ .  
 (1)  $R_{DSon}$  limitation.

Fig 3. SOAR; P-channel

### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	35	K/W

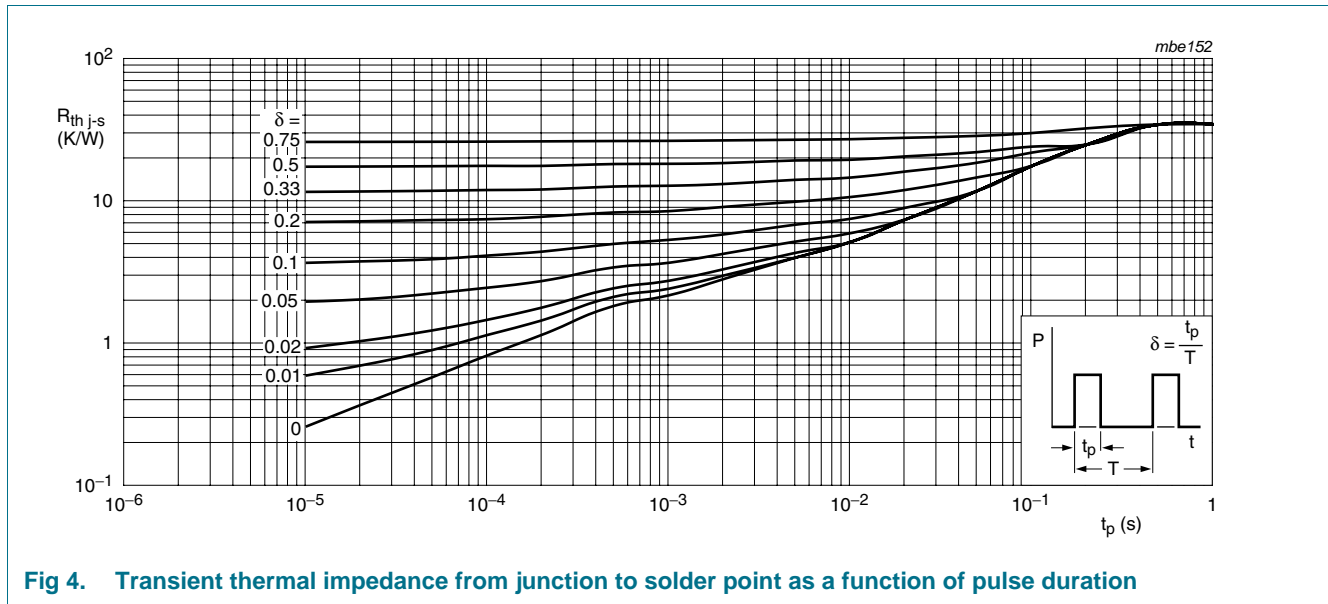


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

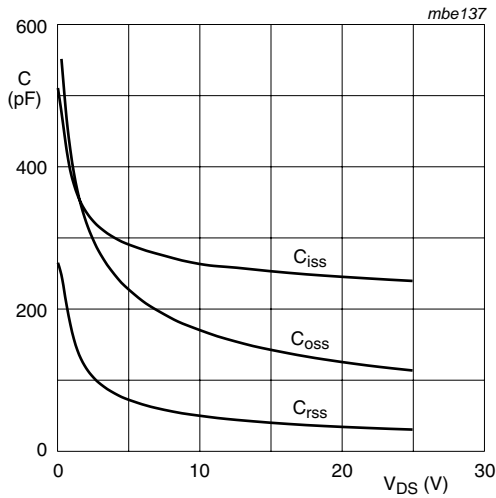
## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -10 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ P-channel	-30	-	-	V
		$I_D = 10 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ N-channel	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = -1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ P-channel; see <a href="#">Figure 17</a>	-1	-	-2.8	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ N-channel; see <a href="#">Figure 17</a>	1	-	2.8	V
$I_{DSS}$	drain leakage current	$V_{DS} = -24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ P-channel	-	-	-100	nA
		$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ N-channel	-	-	100	nA
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ N-channel	-	-	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ P-channel	-	-	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ P-channel	-	-	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ N-channel	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10 \text{ V}; I_D = -1 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ P-channel; see <a href="#">Figure 16</a> ; see <a href="#">Figure 19</a>	-	0.22	0.25	$\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 2.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ N-channel; see <a href="#">Figure 15</a> ; see <a href="#">Figure 18</a>	-	0.08	0.1	$\Omega$
		$V_{GS} = -4.5 \text{ V}; I_D = -0.5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ P-channel; see <a href="#">Figure 16</a> ; see <a href="#">Figure 19</a>	-	0.33	0.4	$\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 1 \text{ A};$ N-channel; see <a href="#">Figure 15</a> ; see <a href="#">Figure 18</a>	-	0.11	0.2	$\Omega$
$I_{DS(on)}$	on-state drain current	$V_{DS} = 5 \text{ V}; V_{GS} = 4.5 \text{ V};$ N-channel	2	-	-	A
		$V_{DS} = -5 \text{ V}; V_{GS} = -4.5 \text{ V};$ P-channel	-1	-	-	A
		$V_{DS} = -1 \text{ V}; V_{GS} = -10 \text{ V};$ P-channel	-2.3	-	-	A
		$V_{DS} = 1 \text{ V}; V_{GS} = 10 \text{ V};$ N-channel	3.5	-	-	A
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 2.3 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ N-channel; see <a href="#">Figure 11</a>	-	10	30	nC
		$I_D = -2.3 \text{ A}; V_{DS} = -15 \text{ V};$ $V_{GS} = -10 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ P-channel; see <a href="#">Figure 12</a>	-	10	25	nC

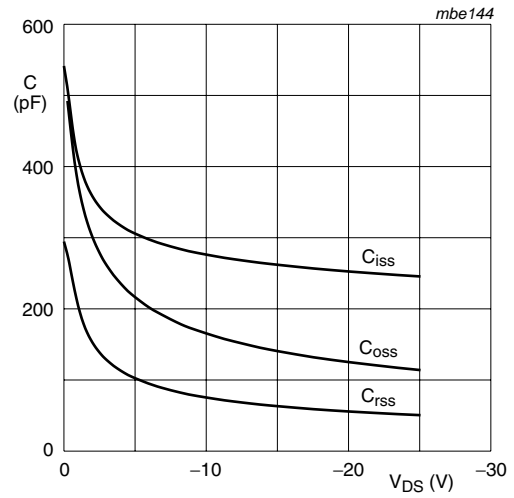
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 2.3 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; N-channel; see <a href="#">Figure 11</a>	-	1	-	nC
		I <sub>D</sub> = -2.3 A; V <sub>DS</sub> = -15 V; V <sub>GS</sub> = -10 V; T <sub>j</sub> = 25 °C; P-channel; see <a href="#">Figure 12</a>	-	1	-	nC
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = -2.3 A; V <sub>DS</sub> = -15 V; V <sub>GS</sub> = -10 V; T <sub>j</sub> = 25 °C; P-channel; see <a href="#">Figure 12</a>	-	3	-	nC
		I <sub>D</sub> = 2.3 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; N-channel; see <a href="#">Figure 11</a>	-	2.5	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; N-channel; see <a href="#">Figure 5</a>	-	250	-	pF
		V <sub>DS</sub> = -20 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; P-channel; see <a href="#">Figure 6</a>	-	250	-	pF
C <sub>oss</sub>	output capacitance	V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; N-channel; see <a href="#">Figure 5</a>	-	140	-	pF
		V <sub>DS</sub> = -20 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; P-channel; see <a href="#">Figure 6</a>	-	140	-	pF
C <sub>rss</sub>	reverse transfer capacitance	V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; N-channel; see <a href="#">Figure 5</a>	-	50	-	pF
		V <sub>DS</sub> = -20 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; P-channel; see <a href="#">Figure 6</a>	-	50	-	pF
g <sub>fs</sub>	transfer conductance	V <sub>DS</sub> = -20 V; I <sub>D</sub> = -1 A; T <sub>j</sub> = 25 °C; P-channel	1	2	-	S
		V <sub>DS</sub> = 20 V; I <sub>D</sub> = 2.2 A; T <sub>j</sub> = 25 °C; N-channel	2	4.5	-	S
t <sub>off</sub>	turn-off time	V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 4.7 Ω; I <sub>D</sub> = 1 A; R <sub>L</sub> = 20 Ω; T <sub>j</sub> = 25 °C; N-channel	-	25	140	ns
t <sub>on</sub>	turn-on time	V <sub>DS</sub> = -20 V; V <sub>GS</sub> = -10 V; R <sub>G(ext)</sub> = 4.7 Ω; I <sub>D</sub> = -1 A; R <sub>L</sub> = 20 Ω; T <sub>j</sub> = 25 °C; P-channel	-	50	140	ns
		V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 4.7 Ω; I <sub>D</sub> = 1 A; R <sub>L</sub> = 20 Ω; T <sub>j</sub> = 25 °C; N-channel	-	20	80	ns
		V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 4.7 Ω; I <sub>D</sub> = 1 A; R <sub>L</sub> = 20 Ω; T <sub>j</sub> = 25 °C; N-channel	-	15	40	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 1.25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; N-channel; see <a href="#">Figure 13</a>	-	-	1.2	V
		I <sub>S</sub> = -1.25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; P-channel; see <a href="#">Figure 14</a>	-	-	-1.6	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = -1.25 A; dI <sub>S</sub> /dt = 100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = -25 V; T <sub>j</sub> = 25 °C; P-channel	-	150	200	ns
		I <sub>S</sub> = 1.25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; T <sub>j</sub> = 25 °C; N-channel	-	35	100	ns



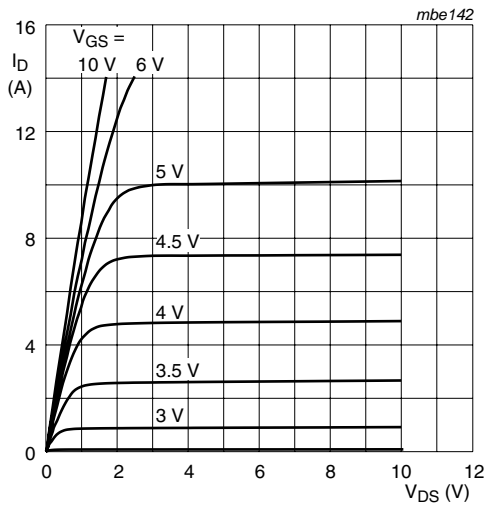
$T_j = 25^\circ\text{C}; V_{GS} = 0\text{V}$

Fig 5. Capacitance as a function of drain-source voltage; N-channel; typical values



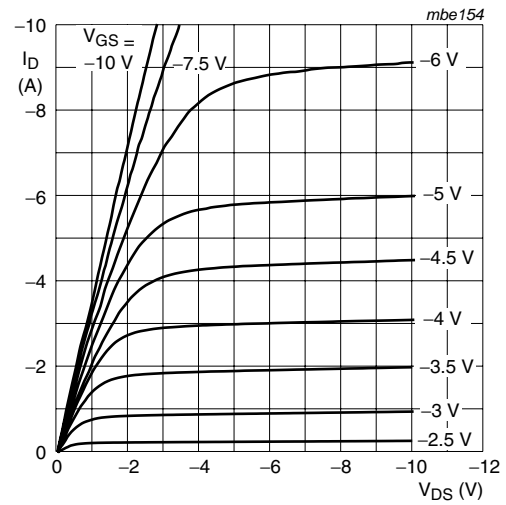
$T_j = 25^\circ\text{C}; V_{GS} = 0\text{V}$

Fig 6. Capacitance as a function of drain-source voltage; P-channel; typical values



$T_j = 25^\circ\text{C}$

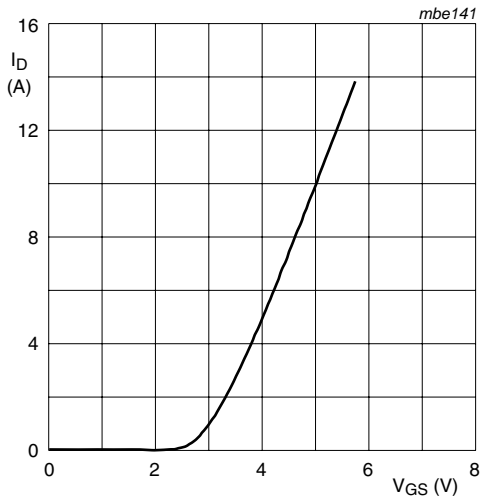
Fig 7. Output characteristics: drain current as a function of drain-source voltage; N-channel; typical values



$T_j = 25^\circ\text{C}$

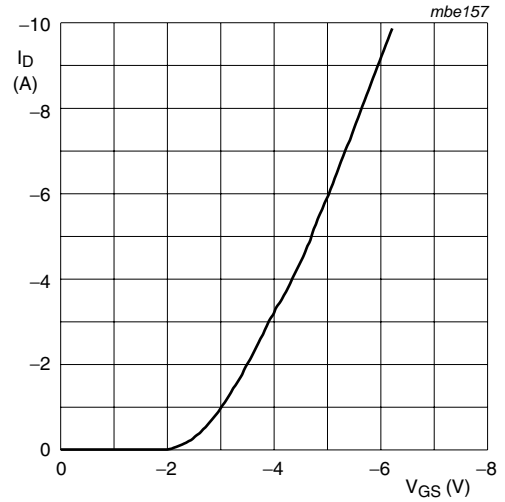
Fig 8. Output characteristics: drain current as a function of drain-source voltage; P-channel; typical values





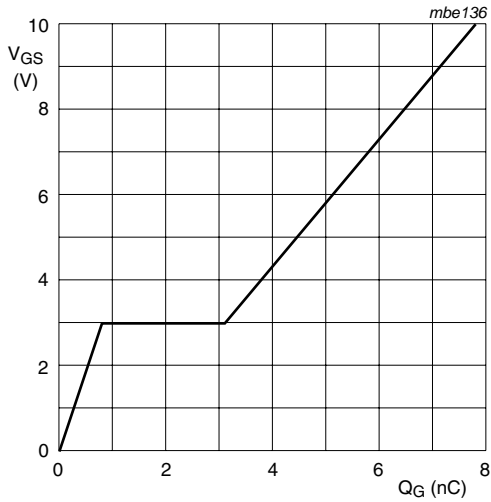
$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$

**Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; N-channel; typical values**



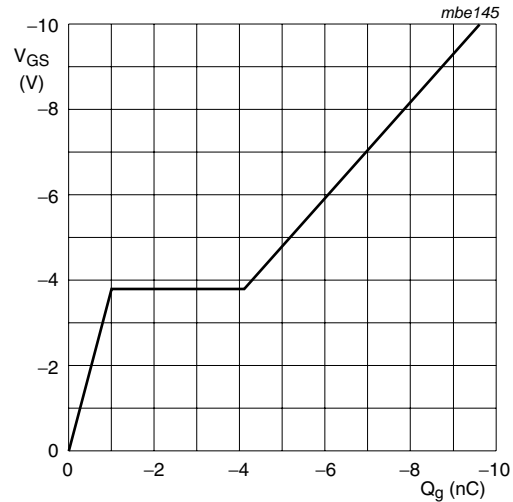
$T_j = 25^\circ\text{C}; V_{DS} = -10\text{V}$

**Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; P-channel; typical values**



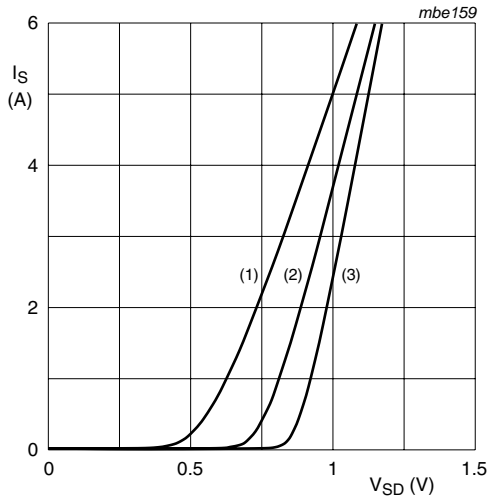
$I_D = 3.5\text{A}; V_{DS} = 15\text{V}$

**Fig 11. Gate-source voltage as a function of gate charge; N-channel; typical values**



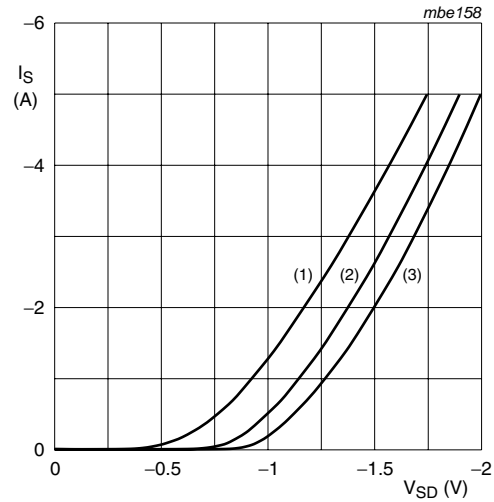
$I_D = -2.3\text{A}; V_{DS} = -15\text{V}$

**Fig 12. Gate-source voltage as a function of gate charge; P-channel; typical values**



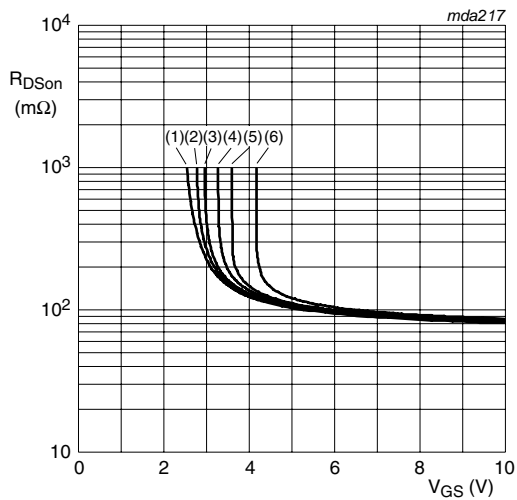
$V_{GD} = 0$ .  
 (1)  $T_j = 150\text{ °C}$ .  
 (2)  $T_j = 25\text{ °C}$ .  
 (3)  $T_j = -55\text{ °C}$ .

**Fig 13. Source current as a function of source-drain voltage; N-channel; typical values**



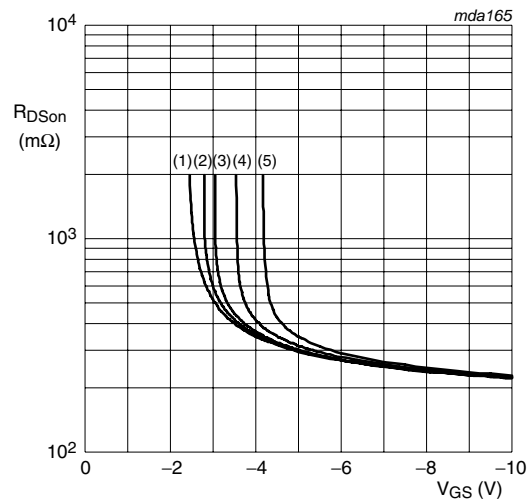
$V_{GD} = 0$ .  
 (1)  $T_j = 150\text{ °C}$ .  
 (2)  $T_j = 25\text{ °C}$ .  
 (3)  $T_j = -55\text{ °C}$ .

**Fig 14. Source current as a function of source-drain voltage; P-channel; typical values**



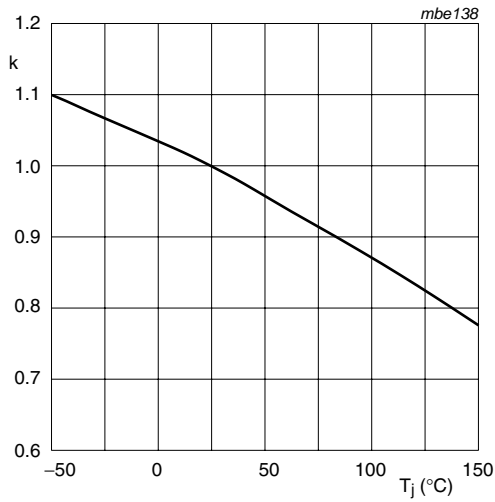
$V_{DS} \geq I_D \times R_{DSon}$ ;  $T_j = 25\text{ °C}$ .  
 (1)  $I_D = 0.1\text{ A}$ .  
 (2)  $I_D = 0.5\text{ A}$ .  
 (3)  $I_D = 1\text{ A}$ .  
 (4)  $I_D = 2.2\text{ A}$ .  
 (5)  $I_D = 3.5\text{ A}$ .  
 (6)  $I_D = 7\text{ A}$ .

**Fig 15. Drain-source on-state resistance as a function of drain current; N-channel; typical values**



$-V_{DS} \geq -I_D \times R_{DSon}$ ;  $T_j = 25\text{ °C}$ .  
 (1)  $I_D = -0.1\text{ A}$ .  
 (2)  $I_D = -0.5\text{ A}$ .  
 (3)  $I_D = -1\text{ A}$ .  
 (4)  $I_D = -2.3\text{ A}$ .  
 (5)  $I_D = -4.5\text{ A}$ .

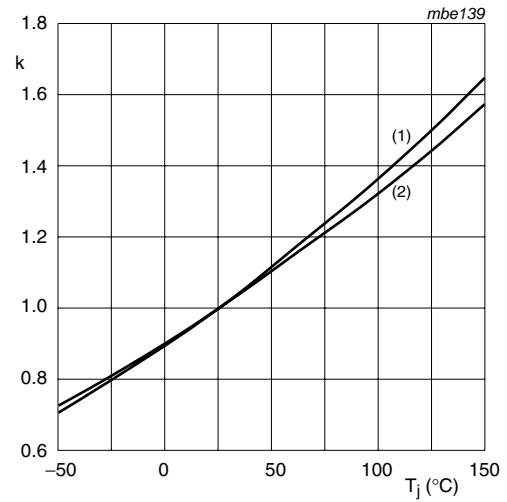
**Fig 16. Drain-source on-state resistance as a function of drain current; typical values**



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25^\circ\text{C}}$$

Typical  $V_{GSth}$  at  $I_D = 1 \text{ mA}$ ;  $V_{DS} = V_{GS} = V_{GSth}$ .

Fig 17. Temperature coefficient of gate-source threshold voltage



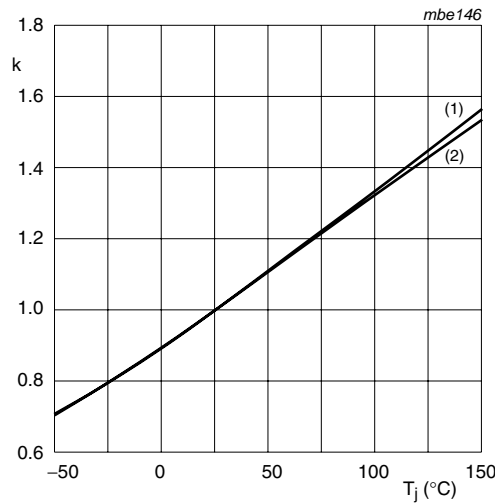
$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25^\circ\text{C}}$$

Typical  $R_{DSon}$  at:

(1)  $I_D = 2.2 \text{ A}$ ;  $V_{GS} = 10 \text{ V}$ .

(2)  $I_D = 1 \text{ A}$ ;  $V_{GS} = 4.5 \text{ V}$ .

Fig 18. Temperature coefficient of drain-source on-state resistance; N-channel



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25^\circ\text{C}}$$

Typical  $R_{DSon}$  at:

(1)  $I_D = -1 \text{ A}$ ;  $V_{GS} = -10 \text{ V}$ .

(2)  $I_D = -0.5 \text{ A}$ ;  $V_{GS} = -4.5 \text{ V}$ .

Fig 19. Temperature coefficient of drain-source on-state resistance; P-channel

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

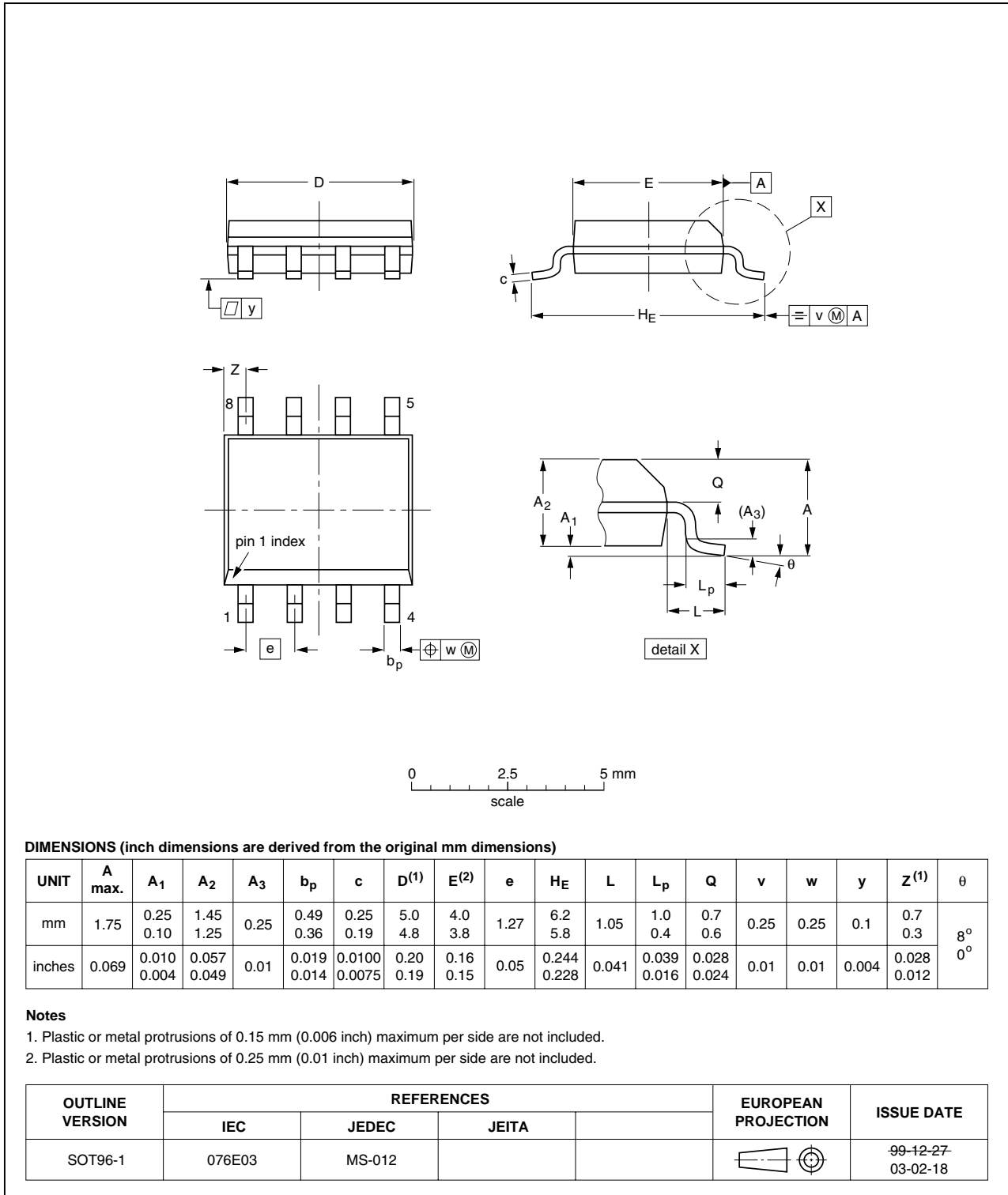


Fig 20. Package outline SOT96-1 (SO8)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHC21025 v.4	20110317	Product data sheet	-	PHC21025 v.3
Modifications:	• Various changes to content.			
PHC21025 v.3	20101217	Product data sheet	-	PHC21025 v.2

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1]</sup> <sup>[2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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