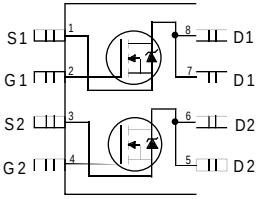
IRF7303

MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Dual N-Channel Mosfet
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching



Top View

V_{DSS} = 30V

$R_{DS(on)}$ = 0.050Ω

SOP-8

Description

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.

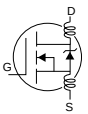
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_A = 25°C	10 Sec. Pulsed Drain Current, V_{GS} @ 10V	5.3	A
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	4.9	
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	3.9	
I_{DM}	Pulsed Drain Current ①	20	
P_D @T_A = 25°C	Power Dissipation	2.0	W
	Linear Derating Factor	0.016	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

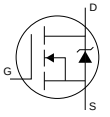
Thermal Resistance Ratings

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient④	——	62.5	°C/W

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.032	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	——	——	0.050	Ω	V_{GS} = 10V, I_D = 2.4A ③
		——	——	0.080		V_{GS} = 4.5V, I_D = 2.0A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	——	——	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	5.2	——	——	S	V_{DS} = 15V, I_D = 2.4A
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	μA	V_{DS} = 24V, V_{GS} = 0V
		——	——	25		V_{DS} = 24V, V_{GS} = 0V, T_J = 125 °C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = - 20V
Q_g	Total Gate Charge	——	——	25	nC	I_D = 2.4A
Q_{gs}	Gate-to-Source Charge	——	——	2.9		V_{DS} = 24V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	7.9		V_{GS} = 10V, See Fig. 6 and 12 ③
$t_{d(on)}$	Turn-On Delay Time	——	6.8	——	ns	V_{DD} = 15V
t_r	Rise Time	——	21	——		I_D = 2.4A
$t_{d(off)}$	Turn-Off Delay Time	——	22	——		R_G = 6.0Ω
t_f	Fall Time	——	7.7	——		R_D = 6.2Ω, See Fig. 10 ③
L_D	Internal Drain Inductance	——	4.0	——	nH	Between lead tip and center of die contact 
L_S	Internal Source Inductance	——	6.0	——		
C_{iss}	Input Capacitance	——	520	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	180	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	72	——		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	2.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	20		
V_{SD}	Diode Forward Voltage	——	——	1.0	V	T_J = 25°C, I_S = 1.8A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	——	47	71	ns	T_J = 25°C, I_F = 2.4A
Q_{rr}	Reverse RecoveryCharge	——	56	84	nC	di/dt = 100A/μs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② I_{SD} ≤ 2.4A, di/dt ≤ 73A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C

③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

④ Surface mounted on FR-4 board, t ≤ 10sec.

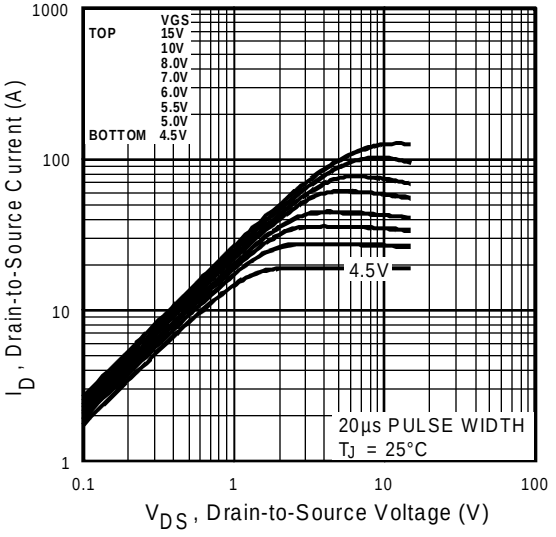


Fig 1. Typical Output Characteristics

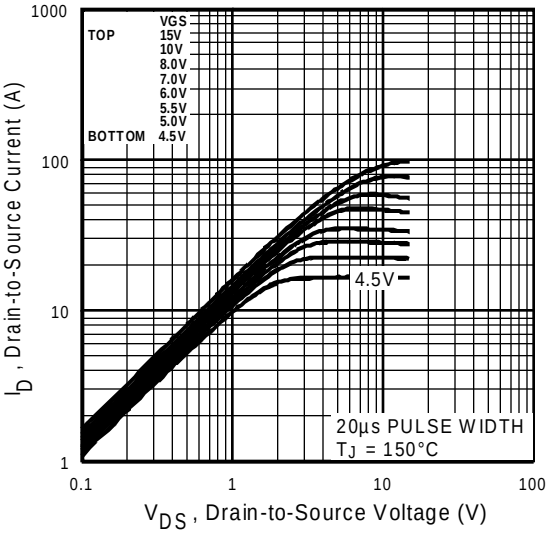


Fig 2. Typical Output Characteristics

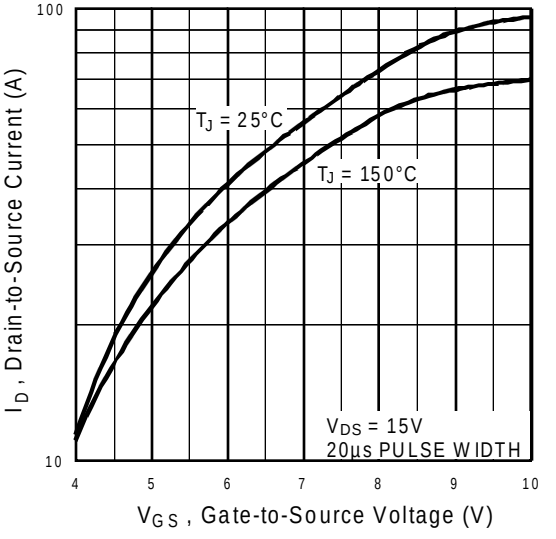


Fig 3. Typical Transfer Characteristics

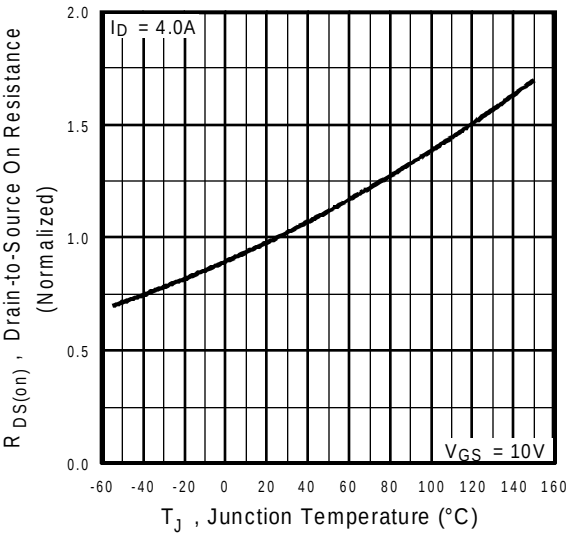


Fig 4. Normalized On-Resistance Vs. Temperature

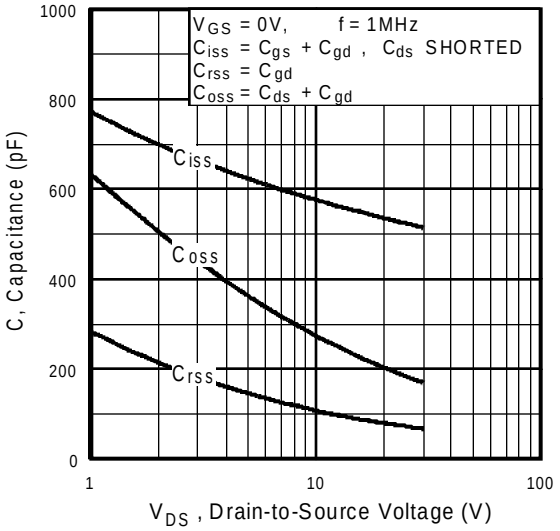


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

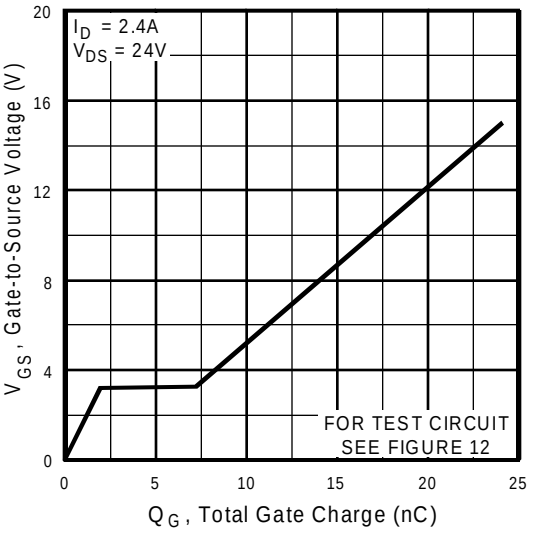


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

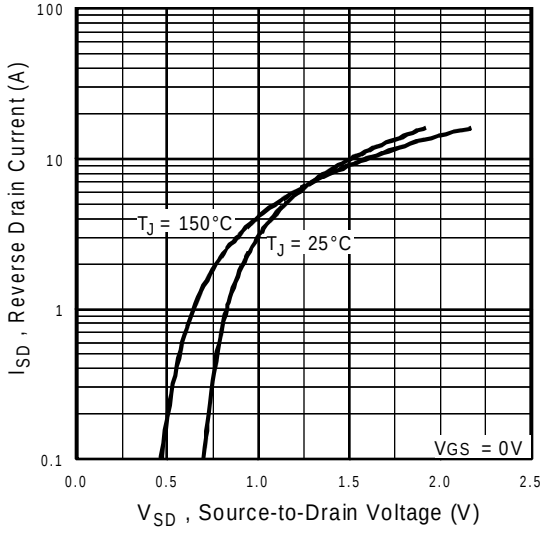


Fig 7. Typical Source-Drain Diode Forward Voltage

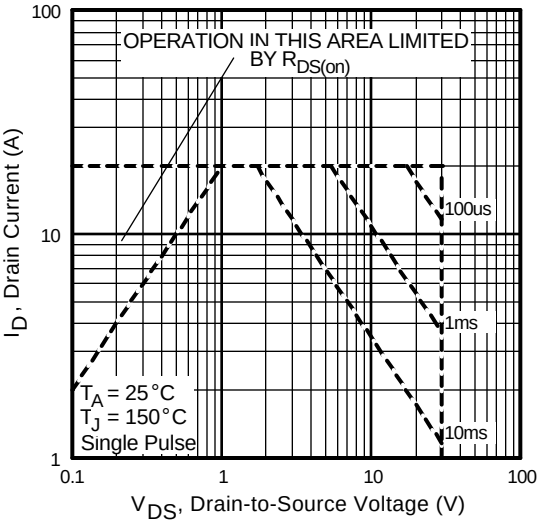


Fig 8. Maximum Safe Operating Area

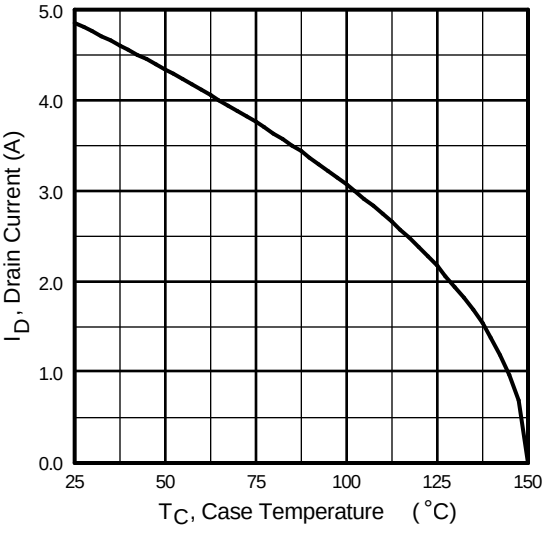


Fig 9. Maximum Drain Current Vs. Ambient Temperature

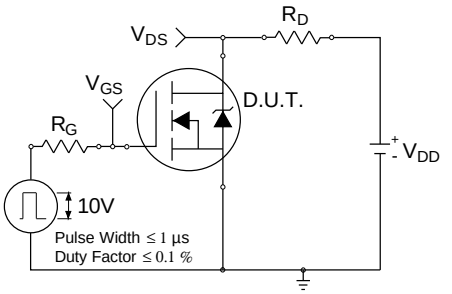


Fig 10a. Switching Time Test Circuit

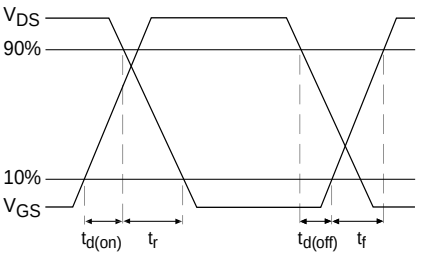


Fig 10b. Switching Time Waveforms

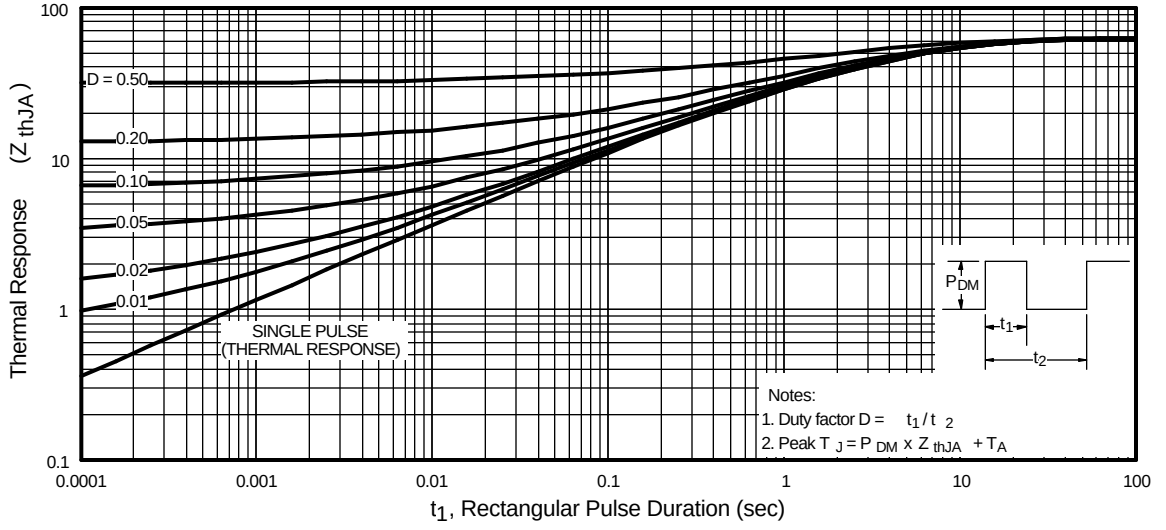


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

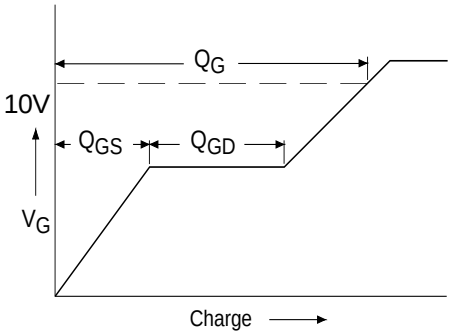


Fig 12a. Basic Gate Charge Waveform

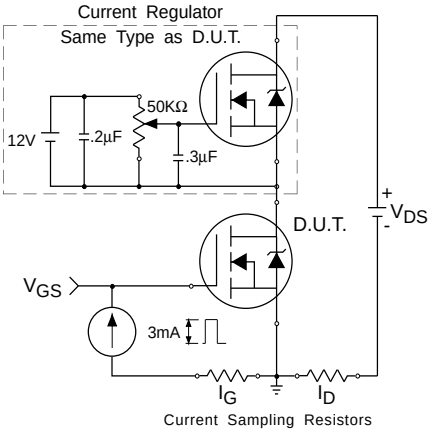
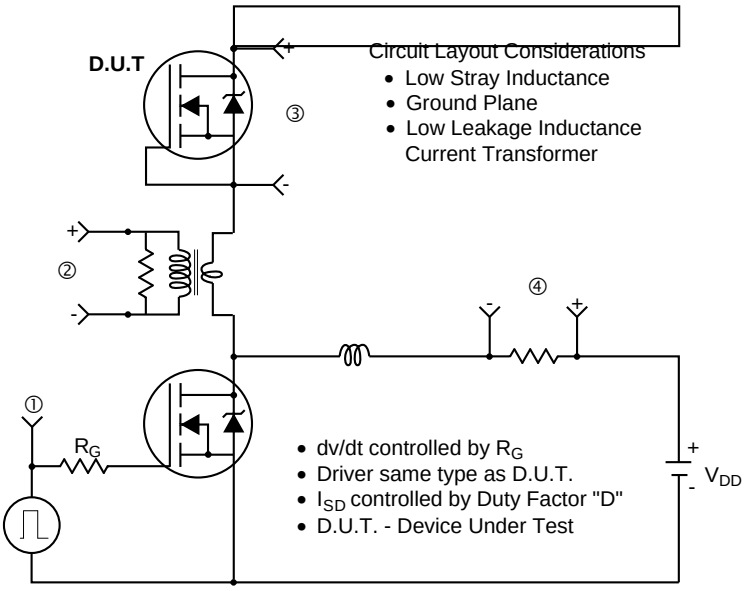
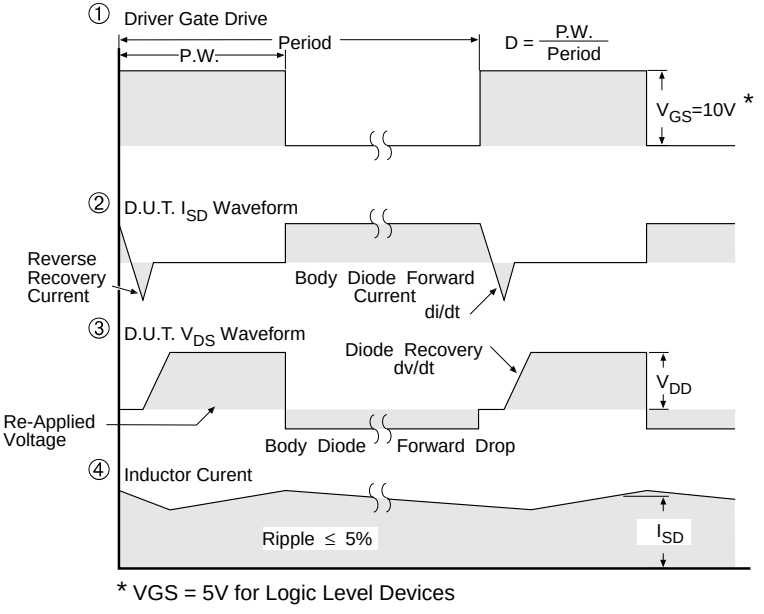


Fig 12b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



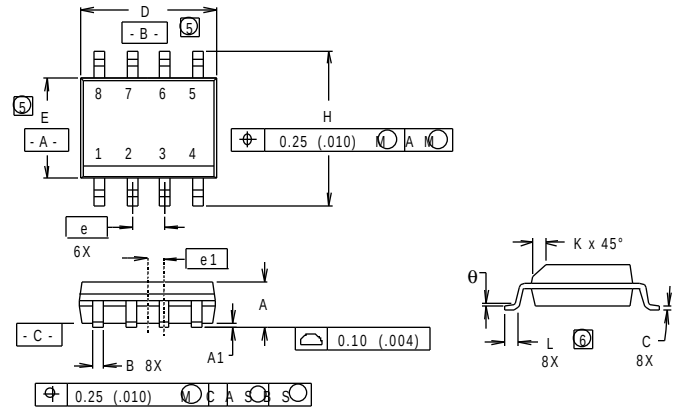


* VGS = 5V for Logic Level Devices

Fig 13. For N-Channel HEXFETS

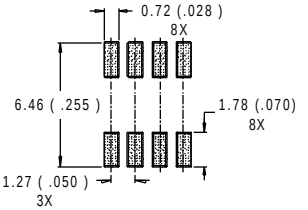
Package Outline

SO8 Outline



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	0.16	.050	0.41	1.27
θ	0°	8°	0°	8°

RECOMMENDED FOOTPRINT



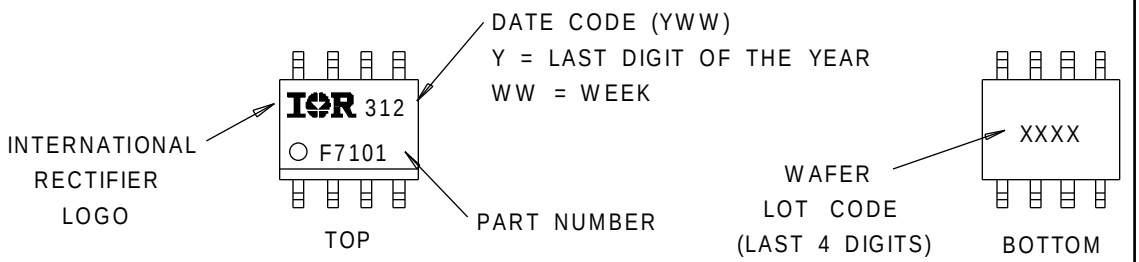
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION : INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS
   MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.006).
6. DIMENSIONS IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE..

Part Marking Information

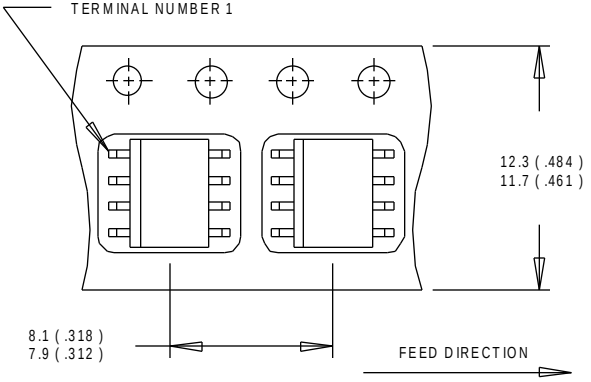
SO8

EXAMPLE : THIS IS AN IRF7101

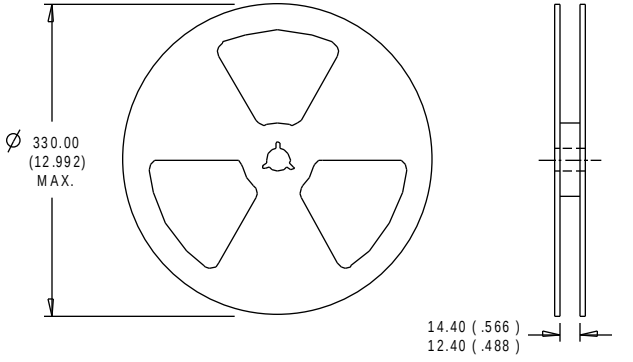


SO8

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.