

TOSHIBA Diode Silicon Epitaxial Planar Type

HN1D01FU

Ultra High Speed Switching Application

- Small package
- Low forward voltage: $V_F(3) = 0.92 \text{ V (typ.)}$
- Fast reverse recovery time: $t_{rr} = 1.6 \text{ ns (typ.)}$
- Small total capacitance: $C_T = 2.2 \text{ pF (typ.)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Maximum (peak) reverse voltage	V_{RM}	85	V
Reverse voltage	V_R	80	V
Maximum (peak) forward current	I_{FM}	300*	mA
Average forward current	I_O	100*	mA
Surge current (10ms)	I_{FSM}	2*	A
Power dissipation	P	200	mW
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	-55 to 125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

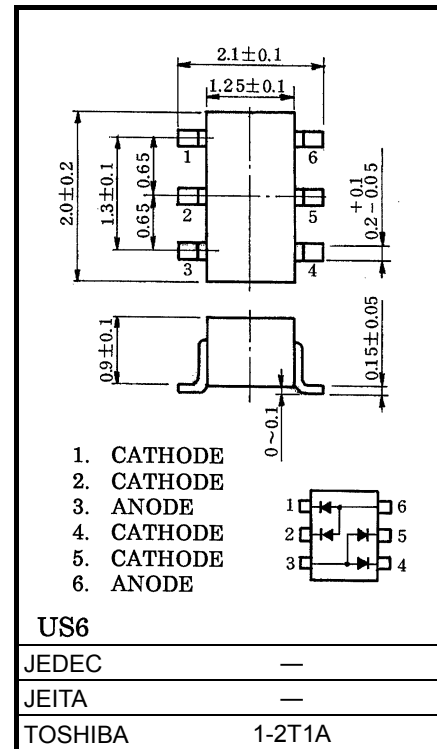
*: This is the Absolute Maximum Ratings of single diode (Q1, Q2, Q3 or Q4).

In the case of using Unit 1 and Unit 2 independently or simultaneously, the Absolute Maximum Ratings per diode is 75% of the single diode one.

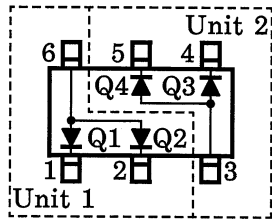
Electrical Characteristics (Q1, Q2, Q3, Q4 Common, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_F(1)$	—	$I_F = 1 \text{ mA}$	—	0.61	—	V
	$V_F(2)$	—	$I_F = 10 \text{ mA}$	—	0.74	—	
	$V_F(3)$	—	$I_F = 100 \text{ mA}$	—	0.92	1.20	
Reverse current	$I_R(1)$	—	$V_R = 30 \text{ V}$	—	—	0.1	μA
	$I_R(2)$	—	$V_R = 80 \text{ V}$	—	—	0.5	
Total capacitance	C_T	—	$V_R = 0, f = 1 \text{ MHz}$	—	2.2	4.0	pF
Reverse recovery time	t_{rr}	—	$I_F = 10 \text{ mA (fig.1)}$	—	1.6	4.0	ns

Unit in mm



Pin Assignment (Top View)



Marking

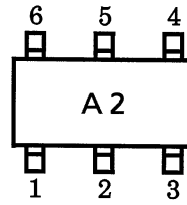
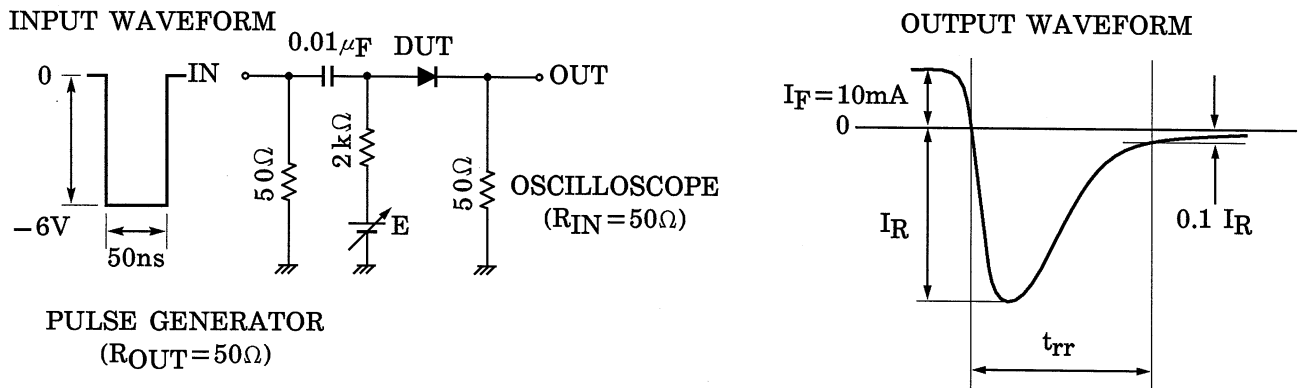
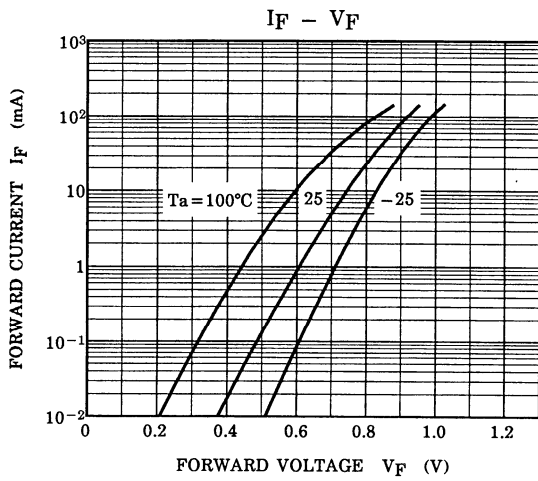


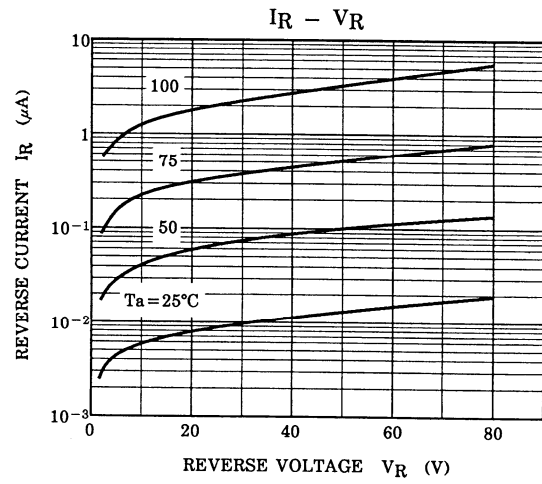
Fig.1 Reverse Recovery Time (t_{rr}) Test Circuit



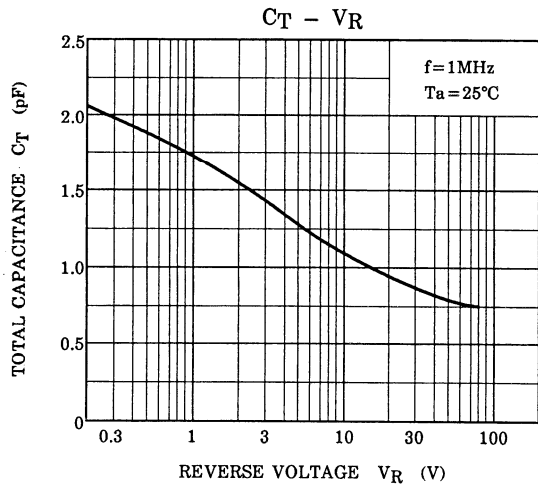
Q1, Q,2, Q3, Q4 Common



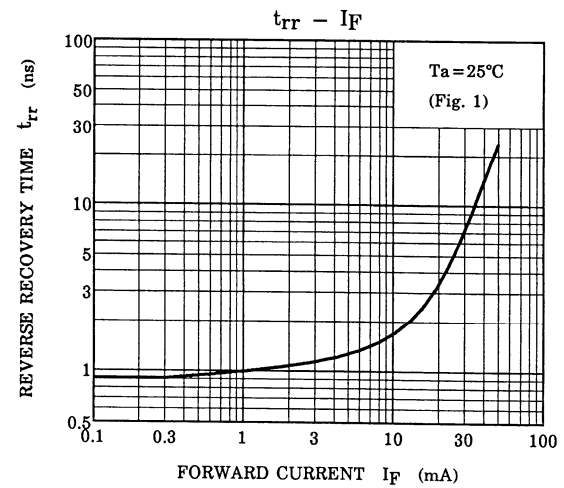
Q1, Q,2, Q3, Q4 Common



Q1, Q,2, Q3, Q4 Common



Q1, Q,2, Q3, Q4 Common



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