TOKO Switching Regulators

FD-Family

No input to output isolation
Single output of 3.3, 5, 12, 15 or 30 V DC/0.5...1.5 W
Double output of ±12 or ±15 V DC/0.5...3 W
Input voltage from 4.5 V up to 17 V DC

- Miniature size
- Surface mounting type
- High power density
- High efficiency
- Excellent line/load regulation
- Parallel operation
- Inhibit function available
- High reliability

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Type Survey

Table 1a: Survey of step-down type FDD

Nominal output voltage $U_{\text{o nom}}$	Nominal output current I_{o}	Input voltage range U_{i}	Nominal input voltage $U_{\text{i nom}}$	Efficiency (typ) η	Type designation (Master or Slave)	Rated output power $P_{\text{o max}}$
3.3 V	120...600 mA	5...12 V	8 V	84%	FDD 1106	2 W
		6...17 V	12 V	82%	FDD 1206	
5 V				87%	FDD 1203	3 W

Table 1b: Survey of flyback type FDB and FDF

Nominal output voltage $U_{\text{o nom}}$	Nominal output current I_{o}	Input voltage range U_{i}	Nominal input voltage $U_{\text{i nom}}$	Efficiency (typ) η	Type designation (Master or Slave)	Rated output power $P_{\text{o max}}$
5 V	100...250 mA	5...12 V	8 V	77%	FDF 1103	1.25 W
12 V	45...115 mA	4.5...5.5 V	5 V	70%	FDB 1001	1.4 W
	70...125 mA	9...17 V	12 V	71%	FDF 1301	1.5 W
15 V	40...90 mA	4.5...5.5 V	5 V	70%	FDB 1002	1.35 W
	70...100 mA	9...17 V	12 V	71%	FDF 1302	1.5 W
30 V	10...30 mA	5...12 V	8 V	79%	FDF 1105	0.9 W
		6...17 V	12V	80%	FDF 1205	
±12 V	±22.5...±57.5 mA	4.5...5.5 V	5 V	72%	FDB 2001	1.4 W
	±35...±62.5 mA	9...17 V	12 V	73%	FDF 2301	1.5 W
±15 V	±20...±45 mA	4.5...5.5 V	5 V	72%	FDB 2002	1.35 W
	±35...±50 mA	9...17 V	12 V	72%	FDF 2302	1.5 W

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Description

The FD-Family features very compact designed switching regulators in a miniature size case for surface mount, hence, these converters have an extremely high power density. With a high efficiency of up to 87 %, very stable output voltages as well as high reliability, the FD-family becomes a perfect choice for the supply of LCD's, non-volatile memories, voltage distribution in 5 V logical circuits and CCD applications. Furthermore, a special master-slave connection allows safe parallel operation of two or more units. For a wide variety of filtering circuits for smooth output voltages, a full range of optional choke coils are available.

Safety and Installation Instructions

Safety for Step Down Types

If the output circuit of a switching regulator is operator-accessible according to the IEC 950 related safety standards, it shall be an SELV circuit (Safety Extra Low Voltage circuit, i.e. a circuit, separated from mains by at least basic insulation, that is so designed and protected that under normal and single fault conditions, the voltage between any two conductors and between any conductor and earth does not exceed DC 60 V).

In the following statement an interpretation is provided of the IEC 950 safety standard with respect to the safety status of the output circuit. However, it is the sole responsibility of the installer or user to assure the compliance with the relevant and applicable safety standards:

If the input circuit of a switching regulator is an SELV circuit, it's output is considered to be an SELV circuit.

Filtering Recommendations

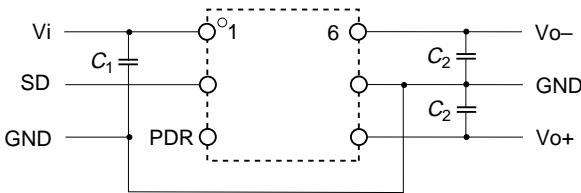Circuit design by means of adding input and output capacitors in order to reduce ripple and noise to a moderate value.

Fig. 1
External circuitry for 2 output units

Safety for Step Up Types

If the output circuit of a switching regulator is operator-accessible according to the IEC 950 related safety standards, it shall be an SELV circuit (Safety Extra Low Voltage circuit, i.e. a circuit, separated from mains by at least basic insulation, that is so designed and protected that under normal and single fault conditions, the voltage between any two conductors and between any conductor and earth does not exceed DC 60 V).

In the following statement an interpretation is provided of the IEC 950 safety standard with respect to the safety status of the output circuit. However, it is the sole responsibility of the installer or user to assure the compliance with the relevant and applicable safety standards:

If the input circuit of a switching regulator is an SELV circuit and the output is protected against overvoltages higher than 60 V by external means, e.g. an overvoltage suppressor diode, the output is considered to be an SELV circuit.
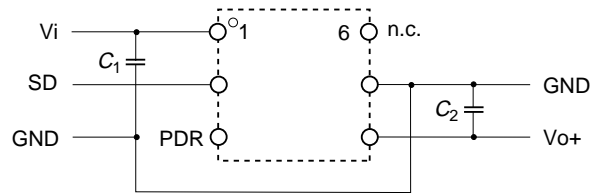

Fig. 2
External circuitry for 1 output step down units

Table 2a: Recommended external capacitors

C_1	$I_{i\ ripple}$ (mA$_{rms}$)	Type	$I_{o\ ripple}$ (mA$_{rms}$)	C_2
OS-CON 10 µF/20 V in parallel Al-Chip 33 µF/25 V	535	FDD 1106	100	SP Cap 22 µF/8 V
	490	FDD 1206	105	
	575	FDD 1203	135	
	450	FDB 1001	245	same as C_1
		FDB 1002	215	
	425	FDB 2001	125	OS CON 3.3 µF/20 V in parallel Al-Chip 33 µF/25 V
	415	FDB 2002	105	

Table 2b: Recommended external capacitors

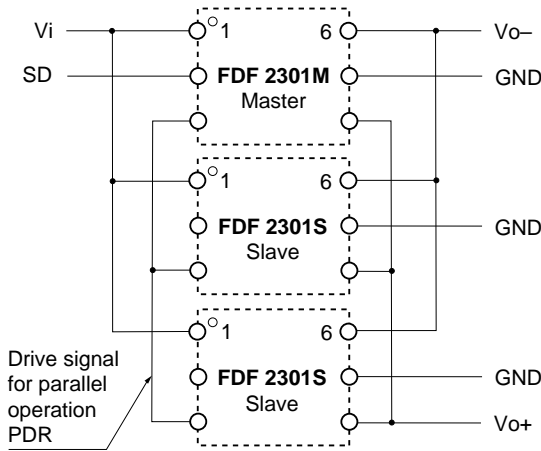| C_1	$I_{i\ ripple}$ (mA$_{rms}$)	Type	$I_{o\ ripple}$ (mA$_{rms}$)	C_2
OS-CON 3.3 µF/20 V in parallel Al-Chip 33 µF/25 V	245	FDF 1301	205	same as C_1
	240	FDF 1302	180	
	260	FDF 2301	135	
	250	FDF 2302	130	
OS-CON 10 µF/20 V in parallel Al-Chip 33 µF/25 V	475	FDF 1103	395	SP Cap 22 µF/8 V in parallel Al-Chip 33 µF/25 V
	295	FDF 1105	55	Al-Chip 10 µF/50 V 2 in parallel
	270	FDF 1205	60	

Remarks:

Smoothing capacitors should be connected within 15 mm from the converter pins.

It is recommended to use low impedance smoothing capacitors with high frequency rating. Refer to the table above for recommended external capacitors.

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Parallel Connection

Fig. 3
Parallel connection

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Notes:

– For parallel operation the master parallel drive signal output is connected to the slave parallel drive signal input.
– Up to 5 units can be operated in parallel.
– The converters should be placed close to each other.

Soldering Directions

Best results can be achieved with a soldering temperature of 215°C for 10 seconds using a reflow soldering system after a pre-heating period of 80 seconds at 135°C. The switching regulator should not be exposed to the heat for more than 30 seconds. Solder temperatures exceeding 240°C may damage the device.

Electrical Input and Output Data

General Condition; $T_A = 25°C$

Table 3a: Input and output data FDD single channel

Characteristics		Conditions	FDD 1106			FDD 1206			FDD 1203			Unit
			min	typ	max	min	typ	max	min	typ	max	
Output												
U_o	Output voltage	$U_{i\,min}…U_{i\,max}$	3.2	3.3	3.4	3.2	3.3	3.4	4.85	5.0	5.15	V
$I_{o\,nom}$	Output current	$U_{i\,min}…U_{i\,max}$	120	360	600	120	360	600	120	360	600	mA
u_o	Output ripple	$U_{i\,min}, I_{o\,max}$		15			15			15		mV_{pp}
$\Delta U_{o\,U}$	Static line regulation	$U_{i\,min}…U_{i\,max}$		±1.5			±1.5			±1.5		%
$\Delta U_{o\,I}$	Static load regulation	$U_{i\,nom}, I_{o\,min}…I_{o\,max}$		±1			±1			±1		
$\Delta U_o/\Delta T$	Thermal coefficient	$U_{i\,nom}, I_{o\,min}…I_{o\,max}$		±0.5			±0.5			±0.5		
Input												
U_i	Input voltage	$I_{o\,min}…I_{o\,max}$	5	8	12	6	12	17	6	12	17	V DC
Efficiency												
η	Efficiency	$U_{i\,nom}, I_{o\,nom}$		84			82			87		%

Table 3b: Input and output data FDB single channel

Characteristics		Conditions	FDB 1001			FDB 1002			Unit
			min	typ	max	min	typ	max	
Output									
U_o	Output voltage	$U_{i\,min}…U_{i\,max}$	11.64	12	12.36	14.55	15	15.45	V
$I_{o\,nom}$	Output current	$U_{i\,min}…U_{i\,max}$	45	80	115	40	65	90	mA
u_o	Output ripple	$U_{i\,min}, I_{o\,max}$		58			49		mV_{pp}
$\Delta U_{o\,U}$	Static line regulation	$U_{i\,min}…U_{i\,max}$		±1.5			±1.5		%
$\Delta U_{o\,I}$	Static load regulation	$U_{i\,nom}, I_{o\,min}…I_{o\,max}$		±1			±1		
$\Delta U_o/\Delta T$	Thermal coefficient	$U_{i\,nom}, I_{o\,min}…I_{o\,max}$		±0.5			±0.5		
Input									
U_i	Input voltage	$I_{o\,min}…I_{o\,max}$	4.5	5	5.5	4.5	5	5.5	V DC
Efficiency									
η	Efficiency	$U_{i\,nom}, I_{o\,nom}$		77			79		%

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General condition: $T_A = 25°C$

Table 3c: Input and output data FDF single channel

Characteristics		Conditions	FDF 1103 min	typ	max	FDF 1105 min	typ	max	FDF 1205 min	typ	max	Unit
Output												
U_o	Output voltage	$U_{i\,min}…U_{i\,max}$	4.85	5	5.15	29.1	30	30.9	29.1	30	30.9	V
$I_{o\,nom}$	Output current	$U_{i\,min}…U_{i\,max}$	100	175	250	10	20	30	10	20	30	mA
u_o	Output ripple	$U_{i\,min}, I_{o\,max}$		34			53			46		mV_{pp}
$\Delta U_{o\,U}$	Static line regulation	$U_{i\,min}…U_{i\,max}$		±1.5			±1.5			±1.5		%
$\Delta U_{o\,I}$	Static load regulation	$U_{i\,nom}, I_{o\,min}…I_{o\,max}$		±1			±1			±1		
$\Delta U_o/\Delta T$	Thermal coefficient	$U_{i\,nom}, I_{o\,min}…I_{o\,max}$		±0.5			±0.5			±0.5		
Input												
U_i	Input voltage	$I_{o\,min}…I_{o\,max}$	5	8	12	5	8	12	6	12	17	V DC
Efficiency												
η	Efficiency	$U_{i\,nom}, I_{o\,nom}$		77			79			80		%

Table 3d: Input and output data FDF single channel

Characteristics		Conditions	FDF 1301 min	typ	max	FDF 1302 min	typ	max	Unit
Output									
U_o	Output voltage	$U_{i\,min}…U_{i\,max}$	11.64	12	12.36	14.55	15	15.45	V
$I_{o\,nom}$	Output current	$U_{i\,min}…U_{i\,max}$	70	100	125	70	85	100	mA
u_o	Output ripple	$U_{i\,min}, I_{o\,max}$		76			72		mV_{pp}
$\Delta U_{o\,U}$	Static line regulation	$U_{i\,min}…U_{i\,max}$		±1.5			±1.5		%
$\Delta U_{o\,I}$	Static load regulation	$U_{i\,nom}, I_{o\,min}…I_{o\,max}$		±1			±1		
$\Delta U_o/\Delta T$	Thermal coefficient	$U_{i\,nom}, I_{o\,min}…I_{o\,max}$		±0.5			±0.5		
Input									
U_i	Input voltage	$I_{o\,min}…I_{o\,max}$	9	12	17	9	12	17	V DC
Efficiency									
η	Efficiency	$U_{i\,nom}, I_{o\,nom}$		71			71		%

Table 3e: Input and output data FDB double channel

Characteristics		Conditions		FDB 2001 min	typ	max	FDB 2002 min	typ	max	Unit
Output										
U_o	Output voltage	$U_{i\,min}…U_{i\,max}$		+11.64 −12.72	+12 −12	+12.36 −11.28	+14.55 −15.90	+15 −15	+15.45 −14.10	V
$I_{o\,nom}$	Output current	$U_{i\,min}…U_{i\,max}$		±22.5	±40	±57.5	±20	±32.5	±45	mA
u_o	Output ripple	$U_{i\,min}, I_{o\,max}$			59			49		mV_{pp}
$\Delta U_{o\,U}$	Static line regulation	$U_{i\,min}…U_{i\,max}$	U_o+		±1.5			±1.5		%
			U_o-		±3.0			±3.0		
$\Delta U_{o\,I}$	Static load regulation	$U_{i\,nom}$	U_o+		±1			±1		
		$I_{o\,min}…I_{o\,max}$	U_o-		±2			±2		
$\Delta U_o/\Delta T$	Thermal coefficient	$U_{i\,nom}, I_{o\,min}…I_{o\,max}$			±0.5			±0.5		
Input										
U_i	Input voltage	$I_{o\,min}…I_{o\,max}$		4.5	5	5.5	4.5	5	5.5	V DC
Efficiency										
η	Efficiency	$U_{i\,nom}, I_{o\,nom}$			72			72		%

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General condition: $T_A = 25°C$

Table 3f: Input and output data FDF double channel

Characteristics		Conditions		FDF 2301			FDF 2302			Unit
				min	typ	max	min	typ	max	
Output										
U_o	Output voltage	$U_{i\,min}...U_{i\,max}$		+11.64	+12	+12.36	+14.55	+15	+15.45	V
				−12.72	−12	−11.28	−15.90	−15	−14.10	
$I_{o\,nom}$	Output current	$U_{i\,min}...U_{i\,max}$		±35	±50	±62.5	±35	±42.5	±50	mA
u_o	Output ripple	$U_{i\,min}, I_{o\,max}$			48			42		mV_{pp}
$\Delta U_{o\,U}$	Static line regulation	$U_{i\,min}...U_{i\,max}$	U_o+		±1.5			±1.5		%
			U_o-		±3.0			±3.0		
$\Delta U_{o\,I}$	Static load regulation	$U_{i\,nom}$	U_o+		±1			±1		
		$I_{o\,min}...I_{o\,max}$	U_o-		±2			±2		
$\Delta U_o/\Delta T$	Thermal coefficient	$U_{i\,nom}, I_{o\,min}...I_{o\,max}$			±0.5			±0.5		
Input										
U_i	Input voltage	$I_{o\,min}...I_{o\,max}$		9	12	17	9	12	17	V DC
Efficiency										
η	Efficiency	$U_{i\,nom}, I_{o\,nom}$			73			73		%

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Immunity to Environmental Conditions

Table 4: Temperature specifications

Temperature			Operating		Storage		
Characteristics		Conditions	min	max	min	max	Unit
T_A	Ambient temperature	$U_{i\,min}...U_{i\,max}$ $I_{o\,min}...I_{o\,max}$	−10	65	−40	85	°C
$r.H.$	Relative humidity			95		95	%

Mechanical Data

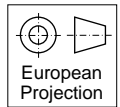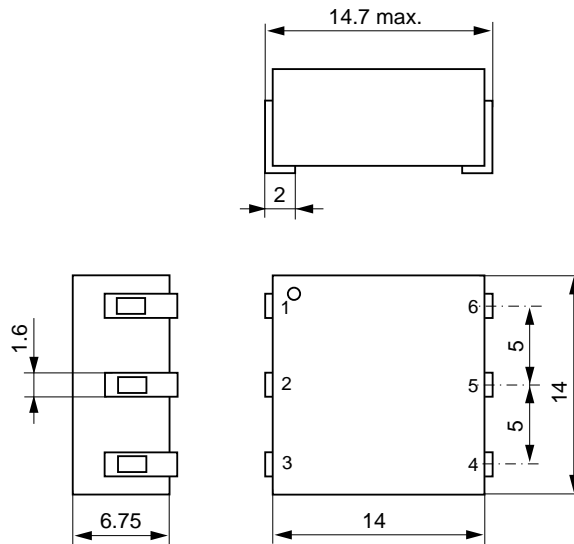Dimensions in mm.

European
Projection

Fig. 4
Mechanical dimensions

Table 5: Pin assignments

Type of regulator		Pin no. 1	Pin no. 2	Pin no. 3	Pin no. 4	Pin no. 5	Pin no. 6
Master	1 output step down	Vi+	SD	PDR	Vo+	GND	n.c.
	2 outputs	Vi+	SD	PDR	Vo+	GND	Vo−
Slave	1 output step down	Vi+	n.c.	PDR	Vo+	GND	n.c.
	2 outputs	Vi+	n.c.	PDR	Vo+	GND	Vo−

n.c. = not connected, SD = Control signal ON/OFF (low = ON, Vi+ or floating = OFF), PDR = Parallel drive signal

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Type Key and Product Marking

Type Key

		FDD 1 1 0 6 M
Family .... FDD, FDB, FDF		
Channel 1, 2		

Nominal input voltage

5 V 0	
9 V 1	
6...17 V 2	
9...15 V 3	

Nominal output voltage

12 V 1	
15 V 2	
5 V 3	
3.3 V 6	

Master/Slave type

Master .... M	
Slave .... S	
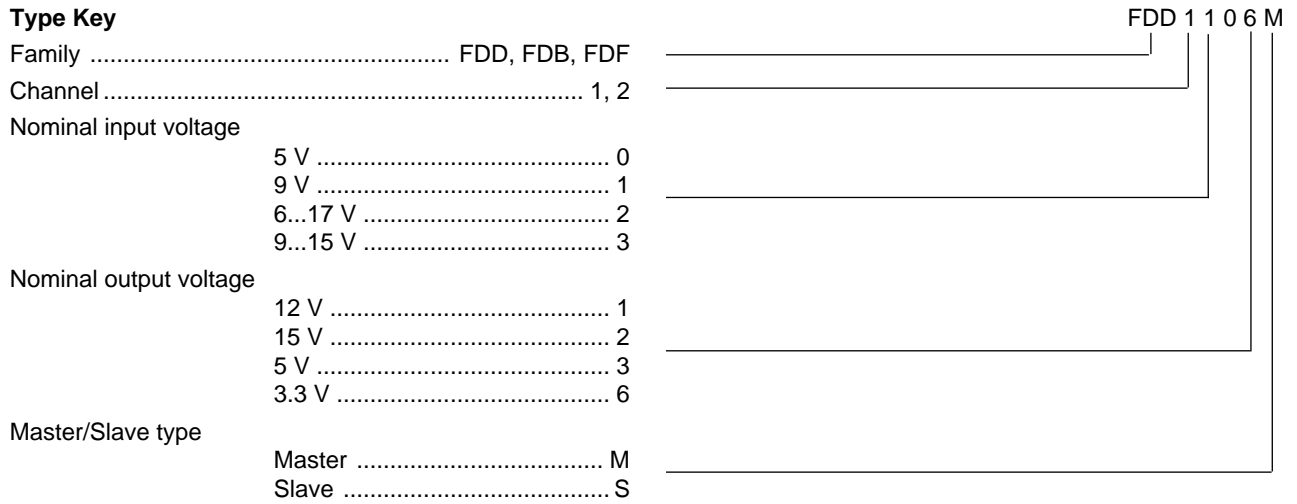
Product Marking

Main face: Part number, output voltage and lot number.

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