

2N5441-2N5446, T6420 Series

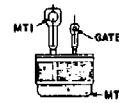
40-A Silicon Triacs

Features:

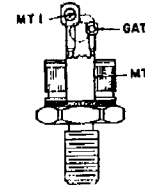
- *di/dt* capability = 100 A/ μ s
- Low switching losses
- Low on-state voltage at high current levels
- Low thermal resistance

Package \ Voltage	200 V Types	400 V Types	600 V Types
Press-Fit	2N5441	2N5442	2N5443
Stud	2N5444	2N5445	2N5446
Isolated-Stud	T6420B	T6420D	T6420M

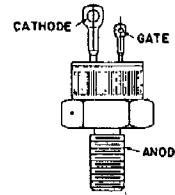
TERMINAL DESIGNATIONS



2N5441-43



T6420 Series



2N5444-46

MAXIMUM RATINGS, Absolute-Maximum Values:

For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with resistive or Inductive Load

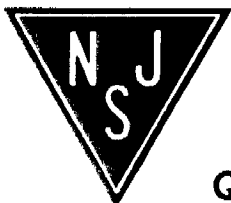
	2N5441 2N5444 T6420B	2N5442 2N5445 T6420D	2N5443 2N5446 T6420M	
• REPETITIVE PEAK OFF-STATE VOLTAGE V_{ORM} Gate Open, $T_j = -65$ to 100°C	200	400	600	V
RMS ON-STATE CURRENT (Conduction angle = 360°C), $I_{\text{TRM(S)}}$ Case temperature				
• $T_c = 70^\circ\text{C}$ (Press-fit types)	40	40	40	A
• $T_c = 65^\circ\text{C}$ (Stud types)	40	40	40	A
• $T_c = 60^\circ\text{C}$ (Isolated-stud types)	40	40	40	A
For other conditions	See Fig. 3			
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT, I_{TRM} For one cycle of applied principal voltage				
• 60 Hz (sinusoidal)	300	300	300	A
• 50 Hz (sinusoidal)	285	285	285	A
For more than one cycle of applied principal voltage	See Fig. 4			
RATE OF CHANGE OF ON-STATE CURRENT, di/dt $V_{\text{DM}} = V_{\text{ORM}}$, $I_{\text{GT}} = 200$ mA, $t_r = 0.1$ μ s (See Fig. 12)	100	100	100	A/ μ s
FUSING CURRENT (for Triac Protection), I^2t $T_j = -65$ to 110°C , $t = 1.25$ to 10 ms	450	450	450	A ² s
• PEAK GATE-TRIGGER CURRENT I_{GT} For 1 μ s max.	12	12	12	A
• GATE POWER DISSIPATION Peak (For 10 μ s max., $I_{\text{GT}} \leq 4$ A, P_{GM}	40	40	40	W
Average, P_{GAV}	0.75	0.75	0.75	W
• TEMPERATURE RANGE Δ Storage, T_{stg}	-65 to 150	-65 to 150	-65 to 150	$^\circ\text{C}$
Operating (Case), T_c	-65 to 110	-65 to 110	-65 to 110	$^\circ\text{C}$
• TERMINAL TEMPERATURE (During Soldering), T_T For 10 s max. (terminals and case)	225	225	225	$^\circ\text{C}$
STUD TORQUE, τ_s Recommended	35	35	35	in-lb
Maximum (DO NOT EXCEED)	50	50	50	in-lb

* In accordance with JEDEC registration data format (JS-14, RDF2) filed for the JEDEC (2N-Series) types.

• For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

Δ For temperature measurement reference point, see Dimensional Outline



NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

2N5441-2N5446, T6420 Series

ELECTRICAL CHARACTERISTICS

At Maximum Ratings Unless Otherwise Specified and at Indicated Case Temperature (T_C)

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		FOR ALL TYPES UNLESS OTHERWISE SPECIFIED			
		MIN.	TYP.	MAX.	
Peak Off-State Current: [♠] Gate open, $T_J = 110^\circ\text{C}$, $V_{DROM} = \text{Max. rated value}$	I_{DROM}	—	0.2	4*	mA
Maximum On-State Voltage: [♠] For $I_T = 100\text{ A (peak)}$, $T_C = 25^\circ\text{C}$	V_{TM}	—	1.7	2	V
For $I_T = 56\text{ A (peak)}$, $T_C = 25^\circ\text{C}$		—	1.5	1.85*	
DC Holding Current: [♠] Gate open, Initial principal current = 500 mA (dc), $v_D = 12\text{V}$: $T_C = 25^\circ\text{C}$	I_{HO}	—	26	60	mA
$T_C = -65^\circ\text{C}$		—	—	100*	
For other case temperatures		See Fig. 6			
Critical Rate of Rise of Commutation Voltage: [♠] For $v_D = V_{DROM}$, $I_T(\text{RMS}) = 40\text{ A}$, commutating $di/dt = 22\text{ A/ms}$, gate unenergized, (See Fig. 13): $T_C = 70^\circ\text{C}$ (Press-fit types)	dv/dt	5*	30	—	V/ μs
$T_C = 85^\circ\text{C}$ (Stud types)		5*	30	—	
$T_C = 60^\circ\text{C}$ (Isolated-stud types)		5	30	—	
Critical Rate of Rise of Off-State Voltage: [♠] For $v_D = V_{DROM}$, exponential voltage rise, gate open, $T_C = 110^\circ\text{C}$: 2N5441, 2N5444, T6420B.	dv/dt	50*	200	—	V/ μs
2N5442, 2N5445, T6420D.		30*	150	—	
2N5443, 2N5446, T6420M.		20*	100	—	
DC Gate-Trigger Current: ^{♠♠} Mode V_{MT2} V_G For $v_D = 12\text{ V (dc)}$ I^+ positive positive $R_L = 30\ \Omega$ III ⁻ negative negative $T_C = 25^\circ\text{C}$ I ⁻ positive negative III ⁺ negative positive	I_{GT}	—	15	50	mA
		—	20	50	
		—	30	80	
		—	40	80	
For $v_D = 12\text{ V (dc)}$ Mode V_{MT2} V_G $R_L = 30\ \Omega$ I ⁺ positive positive $T_C = -65^\circ\text{C}$ III ⁻ negative negative I ⁻ positive negative III ⁺ negative positive		—	—	125*	
For other case temperatures		See Figs. 7 & 8			
DC Gate-Trigger Voltage: ^{♠♠} For $v_D = 12\text{ V (dc)}$, $R_L = 30\ \Omega$, $T_C = 25^\circ\text{C}$	V_{GT}	—	1.35	2.5	V
$T_C = -65^\circ\text{C}$		—	1.8	3.4*	
For other case temperatures		See Fig. 9			
For $v_D = V_{DROM}$, $R_L = 125\ \Omega$, $T_C = 110^\circ\text{C}$		0.2	—	—	
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For $v_D = V_{DROM}$, $I_{GT} = 200\text{ mA}$, $t_r = 0.1\ \mu\text{s}$, $I_T = 60\text{ A (peak)}$, $T_C = 25^\circ\text{C}$ (See Figs. 10 & 14)	t_{gt}	—	1.7	3	μs
Thermal Resistance, Junction-to-Case: Steady-State Press-fit types	$R_{\theta JC}$	—	—	0.8*	$^\circ\text{C/W}$
Stud types		—	—	0.9*	
Isolated-stud types		—	—	1	
Transient (Press-fit & stud types)		See Fig. 11			

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♠♠ For either polarity of gate voltage (V_G) with reference to main terminal 1.