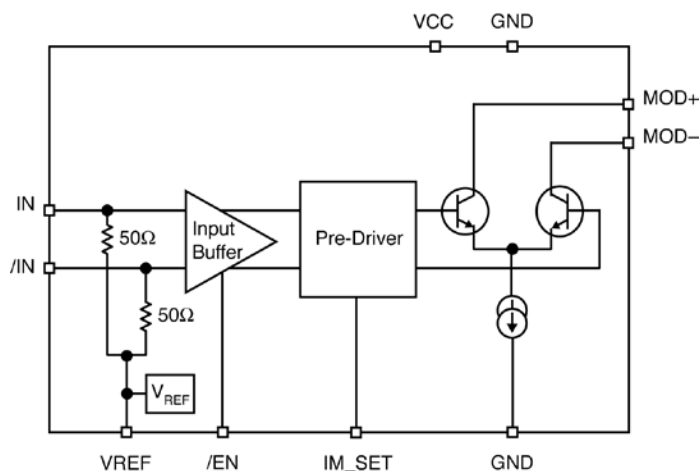


Functional Block Diagram



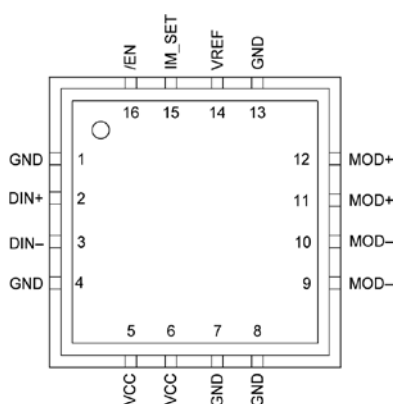
Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88782LMG	QFN-16	Industrial	782L with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY88782LMGTR ⁽²⁾	QFN-16	Industrial	782L with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = +25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.

Pin Configuration



16-Pin QFN

Pin Description

Pin Name	Pin Number	Pin Function
1, 4, 7, 8, 13	GND	Ground. Ground and exposed pad must be connected to the plane of the most negative potential.
2	DIN+	Non-inverting input data. Internally terminated with 50Ω to a reference voltage.
3	DIN–	Inverting input data. Internally terminated with 50Ω to a reference voltage.
5, 6	VCC	Supply Voltage. Bypass with a 0.1μF//0.01μF low-ESR capacitor as close to VCC pin as possible.
9, 10	MOD–	Inverted modulation current output. Outputs modulation current when input data is negative.
11, 12	MOD+	Non-inverted modulation current output. Outputs modulation current when input data is positive.
14	VREF	Reference Voltage. Install a 0.1μF capacitor between VREF and VCC.
15	IM_SET	Modulation current setting and control. The voltage applied to this pin will set the modulation current. To be connected to the MIC3003 pin 24 (VMOD+). Input impedance 25KΩ.
16	/EN	A low-level signal on this pin will enable the output stage of the driver. Internally pulled down with 75KΩ.

Truth Table

DIN+	DIN-	/EN	MOD+ ⁽¹⁾	MOD-	Laser Output ⁽²⁾
L	H	L	H	L	L
H	L	L	L	H	H
X	X	H	H	L	L

Notes:

1. $I_{MOD} = 0$ when MOD+ = H.
2. Assuming that the laser is tied to MOD+.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{IN}) -0.5V to +4.0V
 CML Input Voltage (V_{IN}) $V_{CC}-1.2V$ to $V_{CC}+0.5V$
 TTL Control Input Voltage (V_{IN}) 0V to V_{CC}
 Lead Temperature (soldering, 20sec.) +260°C
 Storage Temperature (T_s) -65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC}) +3.0V to +3.6V
 Ambient Temperature (T_A) -40°C to +85°C
 Package Thermal Resistance⁽³⁾
 QFN
 (θ_{JA}) Still-air 60°C/W
 (Ψ_{JB}) 33°C/W

DC Electrical Characteristics

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ and $V_{CC} = +3.0V$ to $+3.6V$, unless otherwise noted. Typical values are $V_{CC} = +3.3V$, $T_A = 25^\circ\text{C}$, $I_{MOD} = 60\text{mA}$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	Modulation currents excluded		48	65 ⁽⁴⁾	mA
V_{MOD_MIN}	Minimum Voltage Required at the Driver Output (headroom) for Proper Operation		0.6			V
$R_{IN(DATA)}$	Input Resistance (DIN+, DIN-)		45	50	55	Ω
V_{ID}	Differential Input Voltage Swing		200		2400	mV _{pp}
/EN Low					0.8	V
/EN High			2			V
$R_{IN(I_{MOD_SET})}$	I_{M_SET} Input Resistance			25		k Ω
$V_{I_{MOD_SET}}$	Voltage Range on I_{M_SET} Pin	I_{MOD} range 10mA to 90mA			1.2	V

AC Electrical Characteristics

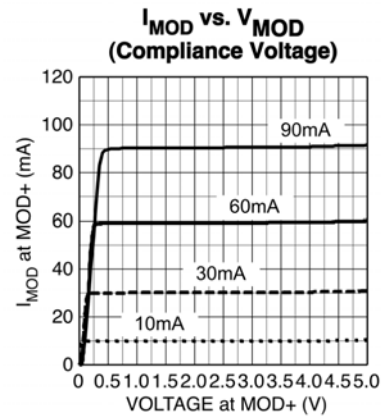
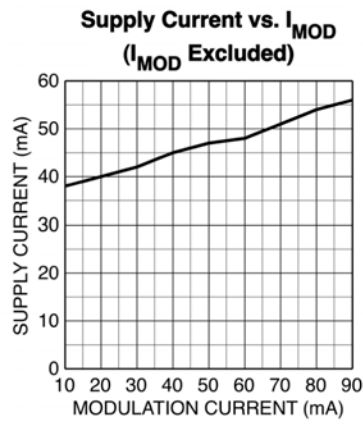
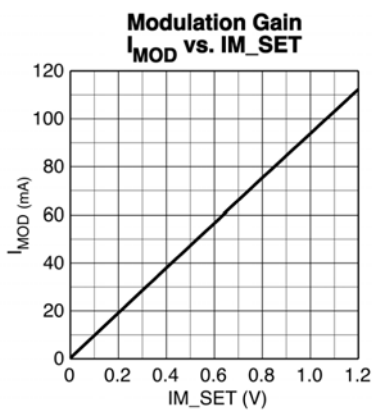
$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ and $V_{CC} = +3.0V$ to $+3.6V$, unless otherwise noted. Typical values are $V_{CC} = +3.3V$, $T_A = 25^\circ\text{C}$, $I_{MOD} = 60\text{mA}$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Data Rate	NRZ	0.05		1.25	Gbps
I_{MOD}	Modulation Current ⁽⁵⁾	AC-coupled	10		90	mA
		DC-coupled	10		70 ⁽⁶⁾	mA
I_{MOD_OFF}	Modulation OFF Current	Current at MOD+ when the device is disabled			750	μA
t_r	Output Current Rise Time	20% to 80%, $I_{MOD} = 60\text{mA}$		55	80	ps
t_f	Output Current Fall Time	20% to 80%, $I_{MOD} = 60\text{mA}$		55	80	ps
	Total Jitter	@1.25Gbps data rate			20	ps _{Pp}
	Pulse-Width Distortion				20	ps

Notes:

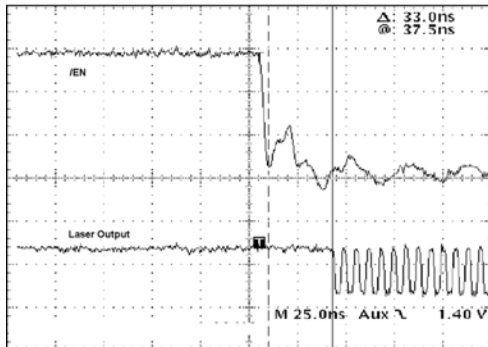
1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. Ψ_{JB} uses a 4-layer and θ_{JA} in still air unless otherwise stated.
4. $I_{CC} = 65\text{mA}$ for worst-case conditions with $I_{MOD} = 90\text{mA}$, $T_A = +85^\circ\text{C}$, $V_{CC} = 3.6V$.
5. Load = 15 Ω .
6. Assuming $V_{CC} = 3.0V$, Laser bandgap voltage = 1V, laser package inductance = 1nH, laser equivalent series resistor = 5 Ω , and damping resistor = 10 Ω .

Typical Operating Characteristics

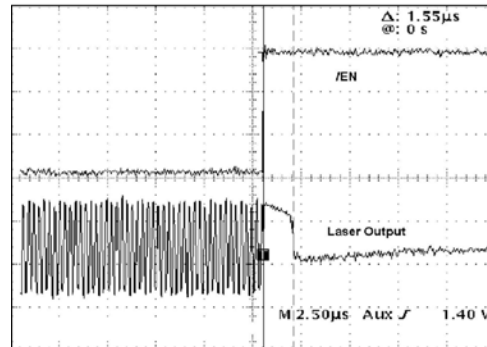


Functional Characteristics

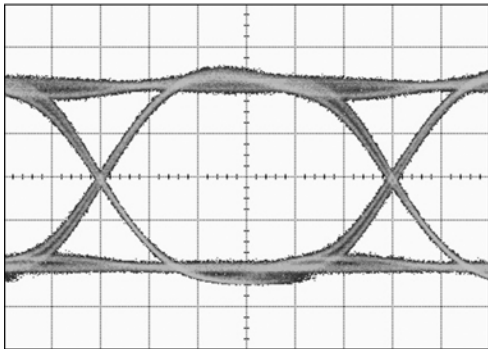
Transmitter Enable Time



Transmitter Disable Time

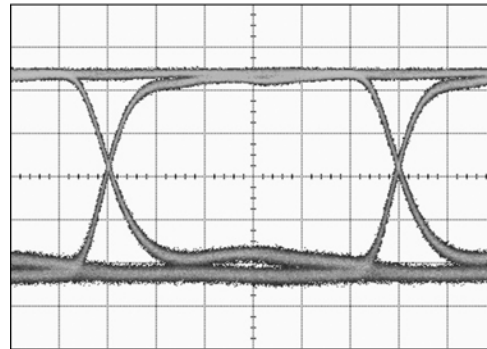


Optical Eye Diagram
1.25Gbps PRBS $2^{23}-1$, ER = 14dB, OC-48 Filter



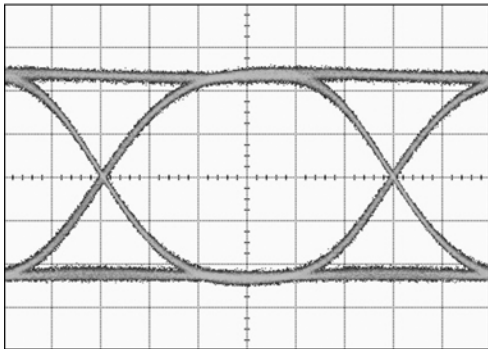
TIME (133ps/div.)

Electrical Eye Diagram
1.25Gbps PRBS $2^{23}-1$, Load = 15Ω



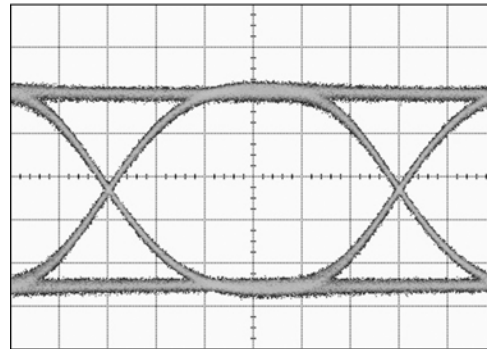
TIME (133ps/div.)

Optical Eye Diagram
622Mbps PRBS $2^{23}-1$, ER = 13dB, OC-12 Filter



TIME (270ps/div.)

Electrical Eye Diagram
155Mbps PRBS $2^{23}-1$, ER = 14dB, OC-3 Filter



TIME (1ns/div.)

Input and Output Stages

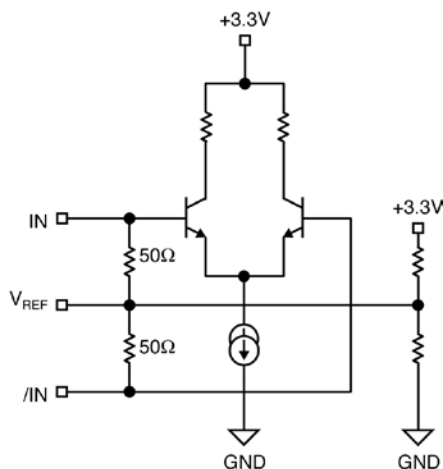


Figure 1a. Simplified Input Stage

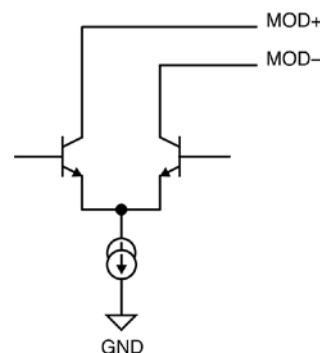


Figure 1b. Simplified Output Stage

Interface the Input to Different Logic Drivers

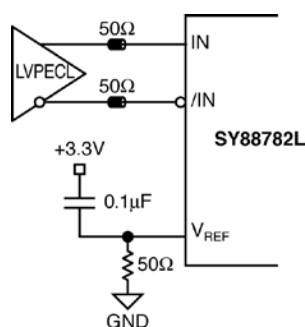


Figure 2a. DC-Coupling to LVPECL Driver

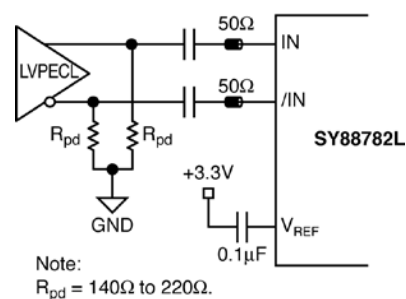


Figure 2b. AC-Coupling to LVPECL Driver

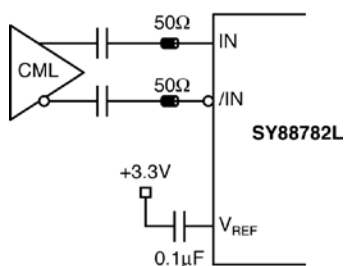


Figure 2c. AC-Coupling to CML Driver

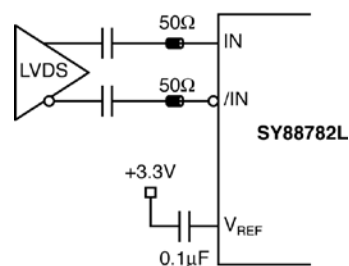
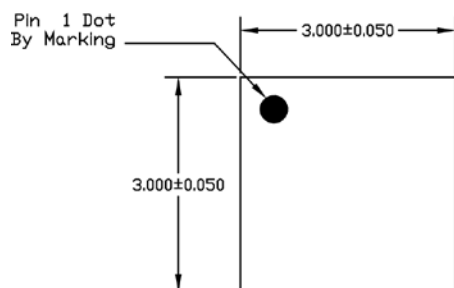
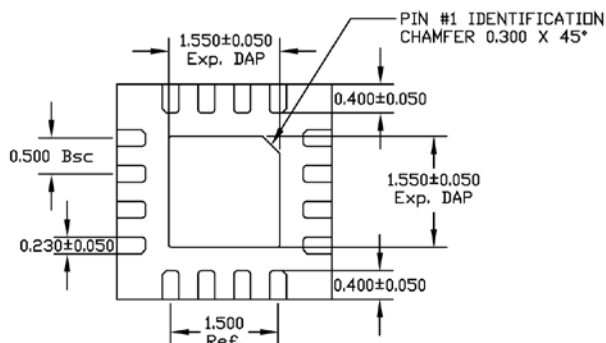
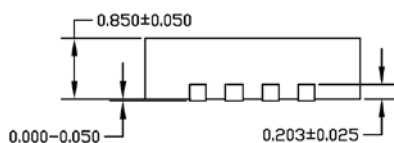


Figure 2d. AC-Coupling to LVDS Driver

16 LEAD (3mmx3mm)TOP VIEWBOTTOM VIEWSIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

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