R8051

8-bit RISC-like Microcontroller Core

The R8051 is a fast, small, single-chip, 8-bit microcontroller that executes all ASM51 instructions. It has the same instruction set as the 80C31, but its RISC-like design executes operations an average of 8 times faster.

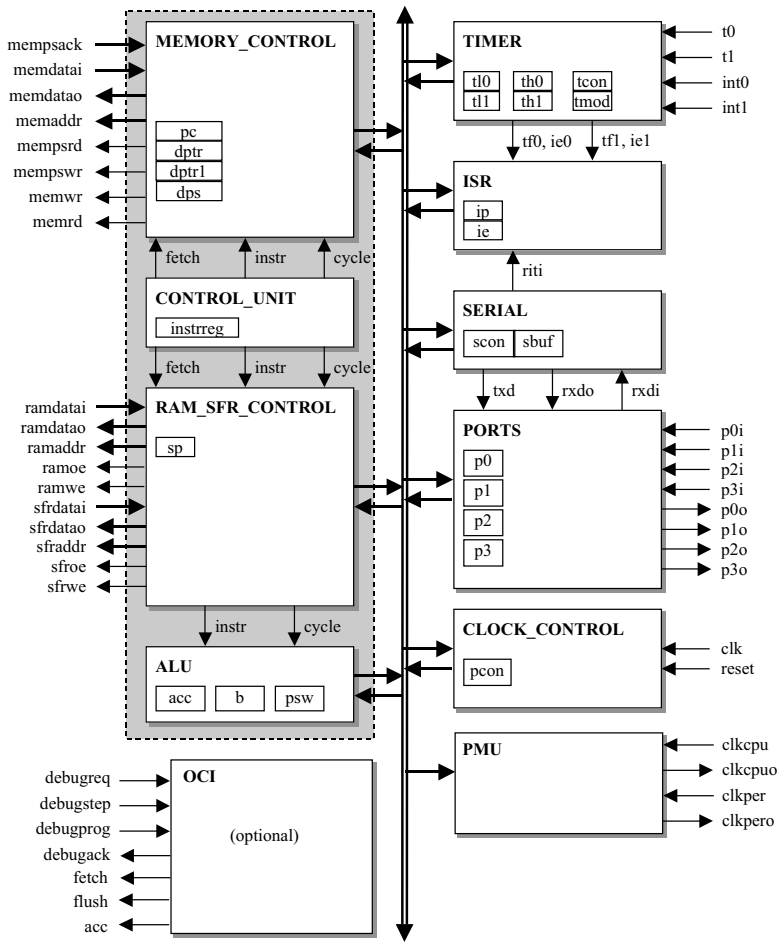
The R8051 provides software and hardware interrupts, a serial communications interface, two timers, and Intel peripherals support. On-chip debugging is an option.

The microcode-free design was developed for easy reuse and is available optimized for several Lattice devices, with competitive utilization and performance characteristics. Scan insertion is also straightforward.

Applications

- Embedded microcontroller systems
- Data computation and transfer
- Communication systems
- Professional audio and video

Block Diagram



Features

- Control Unit
  - 8-bit Instruction decoder
  - Reduced instruction cycle time up to 12 times
- 8-bit Arithmetic-Logic Unit
- 32-bit Input/Output ports
  - Four 8-bit I/O ports
  - Alternate port functions such as external interrupts and serial interface are separated, providing extra port pins when compared with the standard 8051
- Two 16-bit Timer/Counters
- Serial Peripheral Interfaces in full duplex mode
  - Synchronous mode, fixed baud rate
  - 8-bit UART mode, variable baud rate
  - 9-bit UART mode, fixed & variable baud rate
  - Multiprocessor communication
- Two priority/five sources Interrupt Controller
- Internal Data Memory interface
  - Can address up to 256 bytes of Read/Write Data Memory Space
- External Memory interface
  - Can address up to 64 KB of External Program Memory
  - Can address up to 64 KB of External Data Memory
  - De-multiplexed Address/Data Bus to allow easy connection to memories
  - Variable length MOVX to access fast/slow RAM/ or peripherals
  - Wait cycles to access fast/slow ROM
  - Dual data pointer register
  - Program Memory Write mode
- Special Function Registers interface - Services up to 104 External SFRs
- Power Management Unit – IDLE and STOP modes
- JTAG debugging interface (optional)

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Implementation Results

Performance

The architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Since a cycle is aligned with memory fetch when possible, most of the 1-byte instructions are performed in a single cycle. The R8051 uses 1 clock per cycle. This leads to performance improvement of rate 8x (in terms of MIPS) with respect to the Intel device working with the same clock frequency (the original 8051 had a 12-clock architecture. A machine cycle needed 12 clocks and most instructions were either one or two machine cycles. Thus except for the MUL and DIV instructions, the 8051 used either 12 or 24 clocks for each instruction. Furthermore, each cycle in the 8051 used two memory fetches. In many cases the second fetch was dummy, and extra clocks were wasted).

The table below illustrates the speed advantage of the R8051 over the standard 8051. A speed advantage of 12 means that the R8051 performs the same instruction twelve times faster that the 8051.

Speed advantage	Number of instructions	Number of opcodes
24	1	1
12	27	83
9.6	2	2
8	16	38
6	44	89
4.8	1	2
4	18	31
3	2	9
Average: 8.0	**Sum: 111**	**Sum: 255**

Implementation Results

The following are typical performance and utilization results using Lattice ispXPGA™ and ORCA™ devices.

Lattice Device	LUT-4s	Registers	PFUs	SysMEM EBRs	External I/Os	Speed (f_{max}, MHz)
LFX500C-4	4398	655	1160	5	71	26.7
OR4E02-3	4389	476	606	5	71	33.3

Support

The core as delivered is warranted against defects for one year from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The R8051 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 80C31 chip, and the results compared with the core's simulation outputs. The core has also been successfully implemented in commercial and prototype systems.

Deliverables

The core includes everything required for successful implementation:

- Post-synthesis EDIF netlist (firm core) optimized for a specific Lattice device (HDL RTL source code (soft core) is also available)
- Testbenches (self-checking)
- Simulation script, vectors, and expected results
- Synthesis (soft) or place and route (firm) script
- Comprehensive user documentation

Related Information

- CMOS single-chip 8-bit microcontrollers, Philips, 1996.
- Addendum to the MCS®51 Microcontroller Family, Intel, 1996.
- 8-bit Embedded Controllers, Intel, 1990

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