

KVR333S8R25/512

512MB 64M x 72-Bit DDR333 CL2.5 Registered 184-Pin ECC DIMM

DESCRIPTION

This document describes ValueRAM's 64M x 72-bit (512MB) DDR333 CL2.5 SDRAM (Synchronous DRAM) "single rank" Registered ECC memory module. The components on this module include nine 64M x 8-bit (16M x 8-bit x 4 Bank) DDR333 SDRAM in TSOP packages. This 184-pin DIMM uses gold contact fingers and requires +2.5V. The electrical and mechanical specifications are as follows:

SPECIFICATIONS

Clock Cycle Time (tCK) Row Cycle Time (tRC) Refresh Row Cycle Time (tRFC) Row Active Time (tRAS) Single Power Supply of Power 4.125 W (operating) UL Rating 60ns (min.) / 12ns (max.) 42ns (min.) / 70,000ns (max.) 42ns (win.) / 70,000ns (max.) 42ns (win.) / 70,000ns (max.) 42ns (win.) / 70,000ns (max.)		
Refresh Row Cycle Time (tRFC) Row Active Time (tRAS) 42ns (min.) / 70,000ns (max.) Single Power Supply of +2.5V (+/2V) Power 4.125 W (operating)	Clock Cycle Time (tCK)	6ns (min.) / 12ns (max.)
Row Active Time (tRAS) 42ns (min.) / 70,000ns (max.) Single Power Supply of +2.5V (+/2V) Power 4.125 W (operating)	Row Cycle Time (tRC)	60ns (min.)
Single Power Supply of +2.5V (+/2V) Power 4.125 W (operating)	Refresh Row Cycle Time (tRFC)	72ns (min.)
Power 4.125 W (operating)	Row Active Time (tRAS)	42ns (min.) / 70,000ns (max.)
	Single Power Supply of	+2.5V (+/2V)
UL Rating 94 V - 0	Power	4.125 W (operating)
	UL Rating	94 V - 0

Note: The module defined in this data sheet is one of several configurations available under this part number. While all configurations are compatible, the DRAM combination and/or the module height may vary from what is described here.

Figure 1: KVR333S8R25/512 184-Pin DIMM

