PROCESS CP354X

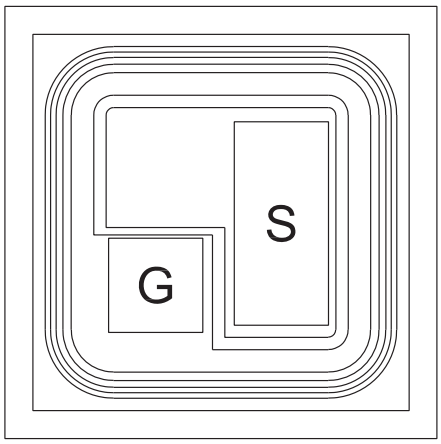
Small Signal MOSFET Transistor

N-Channel Enhancement-Mode Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	21.7 x 21.7 MILS
Die Thickness	5.5 MILS
Gate Bonding Pad Area	4.7 x 4.7 MILS
Source Bonding Pad Area	4.7 x 10.2 MILS
Top Side Metalization	Al-Si - 37,000Å
Back Side Metalization	Au - 12,000Å

GEOMETRY



BACKSIDE DRAIN R1

GROSS DIE PER 6 INCH WAFER

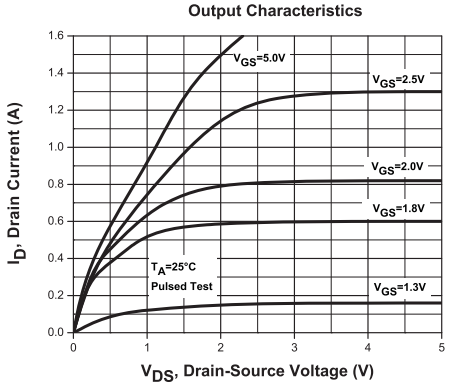
51,400

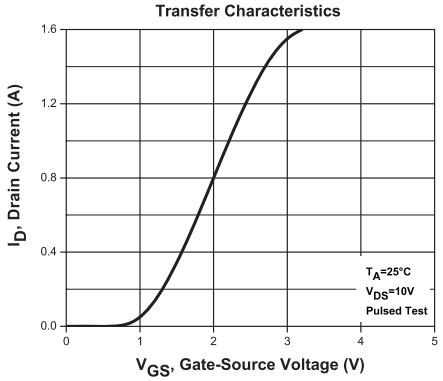
PRINCIPAL DEVICE TYPES

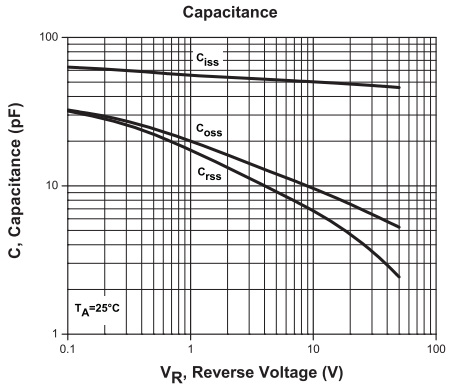
CMLM0305
CMLDM7003
CMPDM7003
CTLDM7003-M621

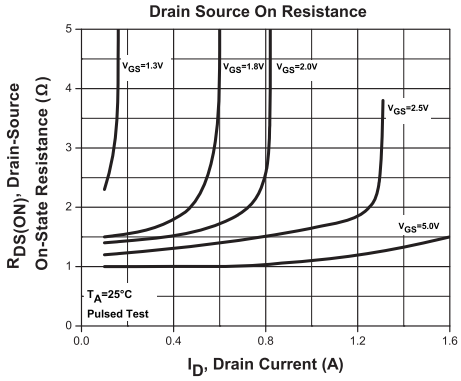
PROCESS CP354X

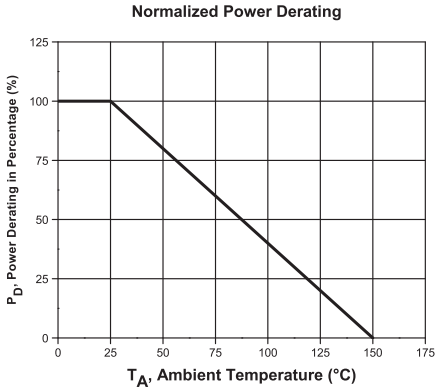
Typical Electrical Characteristics











R2 (22-March 2010)