BU2614
BU2614F
BU2614FS

PLL frequency synthesizer for tuners

The BU2614, BU2614F, and BU2614FS are PLL frequency synthesizers that can operate in the AM and FM bands. They have low power consumption and have internal high-sensitivity RF amplifiers.

Features

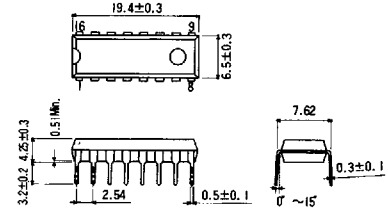
- available in DIP16, SOP16, and SSOP-A16 packages
- low power consumption: operating power = 4 mA, PLL off power = 100 μA
- internal high speed pre-scaler that can divide cycles from 130 MHz VCO
- uses a standard 75 kHz oscillator to reduce radiation noise
- has 7 reference FM and AM frequencies; 1 kHz, 3 kHz, 5 kHz, 3.125 kHz, 6.25 kHz, 12.5 kHz, and 25 kHz
- has an unlock detector
- has an intermediate frequency (IF) measurement counter
- has 3 output ports that are open drain. (For a 7 output port device, see BU2615.)
- serial data input interface (CE, CK, DA)

Applications

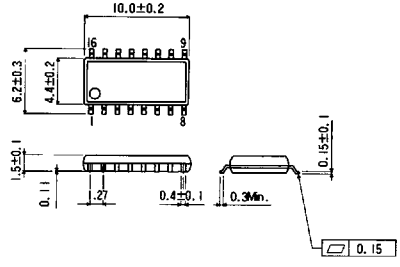
- Tuners (mini-component systems, radio cassette players, wireless devices)

Dimensions (Units : mm)

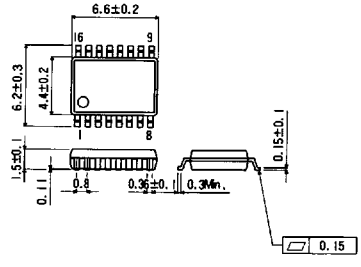
BU2614 (DIP16)



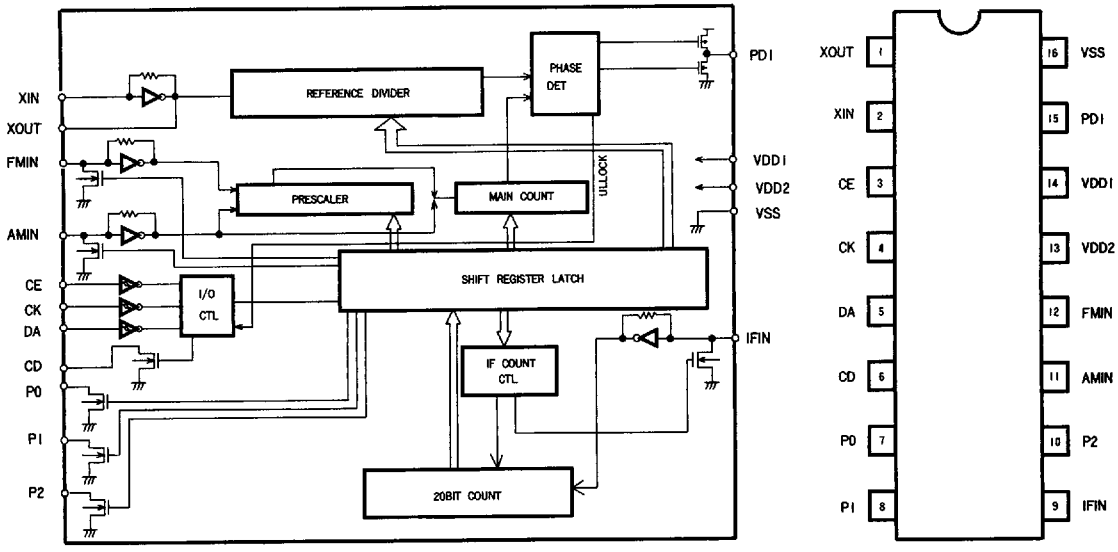
BU2614F (SOP16)



BU2614FS (SSOP-A16)



Block diagram and pin layout



Pin description

Pin	Symbol	Pin name	Pin function	
1	XOUT	Crystal oscillator	For standard frequency and internal clock generation. Connects 75 kHz crystal oscillator	OUT
2	XIN			IN
3	CE	Chip enable	When the CE pin is H, takes the DA, which is synchronized to the rising of the CK pin, into the internal shift register, and is latched by the timing of the fall of the CE pin. Output data is synchronized to the fall of the CK and output from the CD pin.	IN
4	CK	Clock signal		
5	DA	Serial data		
6	CD	Count data	Frequency data and unlock data is output	Nch open drain
7	P0	Output port	Controlled by input data	
8	P1			
9	IFIN	IF input	Input for frequency measurement	IN
10	P2	Output port	Controlled by input data	Nch open drain
11	AMIN	AM in	Oscillator input for AM	IN
12	FMIN	FM in	Oscillator input for FM	IN
13	VDD2	Power supply 2	Power supply 4.0 ~ 6.0 V for high speed circuits	
14	VDD1	Power supply 1	Logic power supply, 2.7 ~ 6.0 V	
15	PD1	Phase shift comp. output	When the value which has separated the local oscillation is higher than the standard frequency, these are HIGH, and when the value is lower , these are LOW. When values are equal, ports have high impedance	Tri-state
16	VSS	GND		

Absolute maximum ratings (T_a = 25°C)

Parameter		Symbol	Limits	Unit	Conditions
Power supply voltage		V_{DD}	−0.3 ~ +7.0	V	V_{DD1}, V_{DD2}
Maximum input voltage 1		V_{IN1}	−0.3 ~ V_{DD} + 0.3	V	CE, CK, CA
Maximum input voltage 2		V_{IN2}	−0.3 ~ V_{DD} + 0.3	V	XIN, FMIN, AMIN, IFIN
Maximum output voltage 1		V_{OUT1}	−0.3 ~ +10.0	V	P0, P1, P2, CD
Maximum output voltage 2		V_{OUT2}	−0.3 ~ V_{DD} + 0.3	V	PD1, XOUT
Maximum output current		I_{OUT}	0 ~ 3.0	mA	P0, P1, P2, CD
Power dissipation	BU2614	P_d	1000	mW	Reduce power by 10 mW for each degree above 25°C.
	BU2614F/FS		500		Reduce power by 5 mW for each degree above 25°C.
Operating temperature		T_{opr}	−10 ~ +75	°C	
Storage temperature		T_{stg}	−55 ~ +125	°C	

Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD1}	2.7 ~ 6.0	V
	V_{DD2}	4.0 ~ 6.0	V

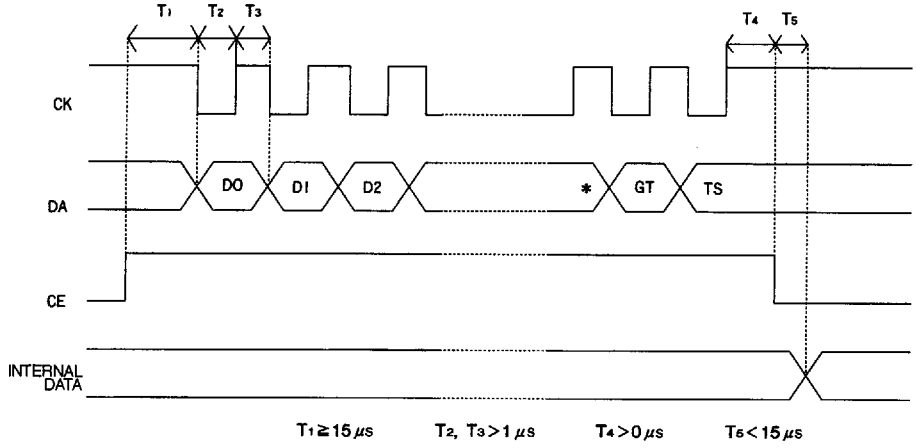
Electrical characteristics (T_a = 25°C, V_{DD1} = V_{DD2} = 5.0 V) (Sheet 1 of 2)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Operating current 1	I_{DD1}		5.0	10.0	mA	FM_{IN} = 130 MHz, 100 mV_{rms}, pin 13 current
Operating current 2	I_{DD2}		100	150	µA	FM_{IN} = 130 MHz, 100 mV_{rms}, pin 14 current
Quiescent current	I_{DD3}		150	300	µA	No input, PLL = OFF, pin 13 current
[H] level input voltage	V_{IH}	4.0			V	CE, CK, DA
[L] level input voltage	V_{IL}			1.0	V	CE, CK, DA
[H] level input current 1	I_{IH1}			1.0	µA	CE, CK, DA, V_{IN} = V_{DD}
[H] level input current 2	I_{IH2}		0.3		µA	XIN, V_{IN} = V_{DD}
[H] level input current 3	I_{IH3}		6.0		µA	FMIN, AMIN, IFIN, V_{IN} = V_{DD}
[L] level input current 1	I_{IL1}	−1.0			µA	CE, CK, DA, V_{IN} = V_{SS}
[L] level input current 2	I_{IL2}		−0.3		µA	XIN, V_{IN} = V_{SS}
[L] level input current 3	I_{IL3}		−6.0		µA	FMIN, AMIN, IFIN, V_{IN} = V_{SS}
[L] level output voltage 1	V_{OL1}		0.2	0.5	V	P_0, P_1, P_2, CD, I_O = 1.0 mA
[OFF] level leak current 1	I_{OFF1}			1.0	µA	P_0, P_1, P_2, CD, V_O = 10 V

Electrical characteristics (T_a = 25°C, V_{DD1} = V_{DD2} = 5.0 V) (Sheet 2 of 2)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
[L] level output voltage 2	V_{OL2}		0.1	0.5	V	FMIN, AMIN, IFIN, I_{OUT} = 0.1 mA
[H] level output voltage	V_{OH}	V_{DD} −1.0	V_{DD} −3.0		V	PD1, I_{OUT} = −1.0 mA
[L] level output voltage	V_{OL}		0.2	1.0	V	PD1, I_{OUT} = 1.0 mA
[OFF] level leak current 2	I_{OFF2}			100	nA	PD1, V_{OUT} = V_{DD}
[OFF] level leak current 3	I_{OFF3}	−100			nA	PD1, V_{OUT} = V_{SS}
Int feedback resistance 1	R_{F1}		10		MΩ	XIN
Int feedback resistance 2	R_{F2}		500		kΩ	FMIN, ANIN, IFIN
Input frequency 1	F_{IN1}	10	75	160	kHz	XIN, sine wave, C-coupling
Input frequency 2	F_{IN2}	10		130	MHz	FMIN, sine wave, C-coupling, V_{IN} = 50 V_{rms}
Input frequency 3	F_{IN3}	0.4		30	MHz	AMIN1, sine wave, C-coupling, V_{IN} = 70 V_{rms}
Input frequency 4	F_{IN4}	0.4		16	MHz	IFIN, sine wave, C-coupling, V_{IN} = 70 V_{rms}
Input amplitude	F_{INmax}			1.5	V_{rms}	XIN, FMIN, AMINI, IFIN, sine wave, C-coupling
Minimum pulse width	t_W		1.0		µs	CK, DA
Input rise time	t_R			500	ns	CE, CK, DA
Input fall time	t_F			500	ns	CE, CK, DA

Input data format



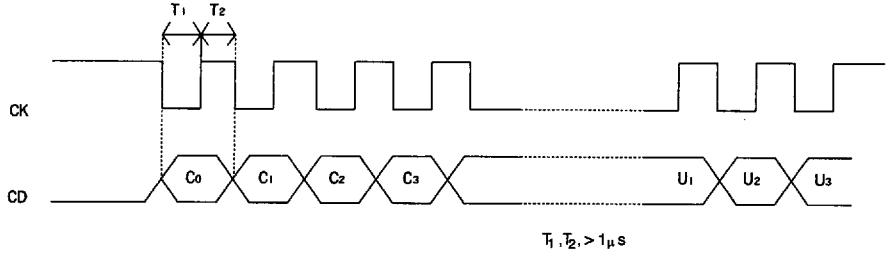
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

← Input from D0

P_0	P_1	P_2	*	*	*	*	CT	R_0	R_1	R_2	S	PS	*	GT	TS

* = any input

Output data format: Make CE output to LO



Output when applying pull-up resistance
Output data format

C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

← Output from C0

C_{15}	C_{16}	C_{17}	C_{18}	U_0	U_1	U_2	U_3

Data output is only possible when CT = 1 or GT = 1

Explanation of data formats

(1) Dividing frequency data: D0 - 15, S = 1, uses D4 - D15.

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

Example:

Divided frequency = 1100 (D) = 1100 ÷ 2 = 550(D) = 226(H) S = 0, PS = 0
(Divided frequency is 2 times the set value)

	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0
Divided frequency = 1107(D) = 453(H) S = 1 PS = 1	1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0
Divided frequency = 926(D) = 39E(H) S = 1 PS = 0	X	X	X	X	0	1	1	1	1	0	0	1	1	1	0	0

(2) CT: Frequency measurement Initiation data
- 1: Measurement initiation
- 0: Internal counter is reset, IFIN is pulled down

(3) Output port control data PO, P1, P2
- 1: Open drain output ON
- 0: Open drain output OFF

Data			Standard frequency (kHz)
R_O	R_1	R_2	
0	0	0	25
0	0	1	12.5
0	1	0	6.25
0	1	1	5
1	0	0	3.125
1	0	1	3
1	1	0	1
1	1	1	PLL OFF (see note)

F

Note: FMIN = pull down, AMIN = pull down, PD = high impedance

(5) S: switching of FMIN and AMIN
0: FMIN
1: AMIN

(6) PS: when AMIN is selected, divide cycles by turning ON this bit.

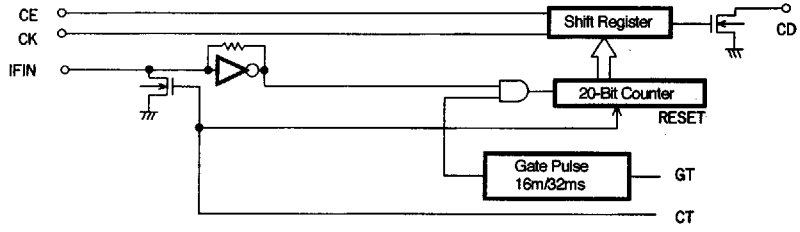
(7) GT: Frequency measurement time and unlock detection ON / OFF.

CT	GT	Frequency measurement	Unlock detector	Data output
0	0	OFF	OFF	NG
0	1	OFF	ON	OK
1	0	ON gate time 16 ms	ON	
1	1	ON gate time 32 ms	ON	

(8) TS: Data for testing Input (0).

Frequency counter

Configuration



Operation of the frequency counter

When the control data CT = 1, the 20-bit counter and the amplifier are in operation.

When CT = 0, the input is pulled down and the counter is reset.

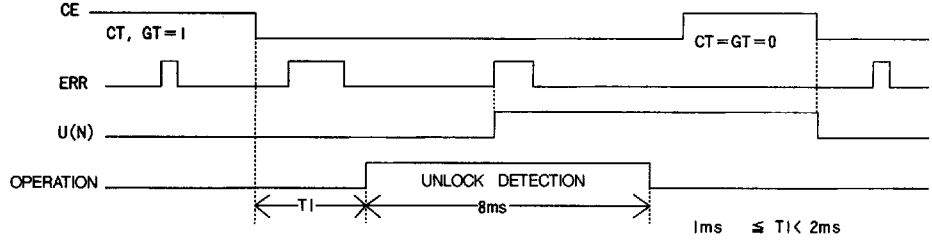
The gate pulse (measurement time) (16 or 32 ms) is selected depending on the control data GT. The counter is reset when control data (CT) = 0.

Explanation of output data

Unlock detection circuit operation

D_0 is the least significant bit and D_{19} is the most significant bit.

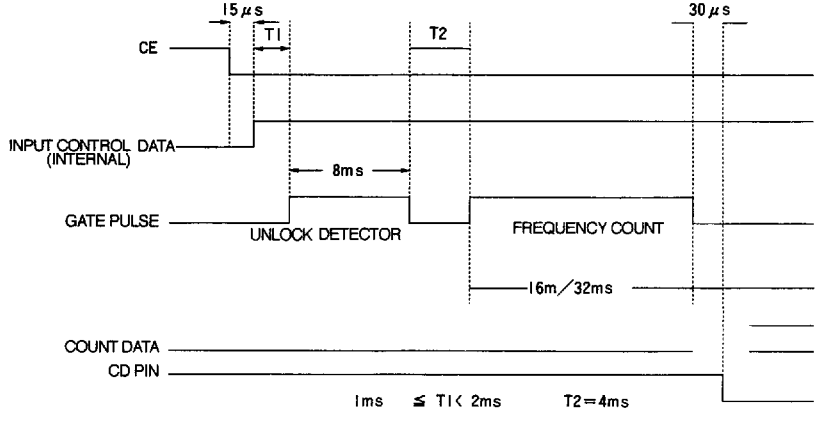
When the control data is GT = 1 or CT = 1, the unlock detection circuit operates for 8 ms. When CT = 1, the unlock detector operation ends before the frequency counter gate pulse emerges. The unlock detection circuit is reset in the interval when CT = 0 and GT = 0.



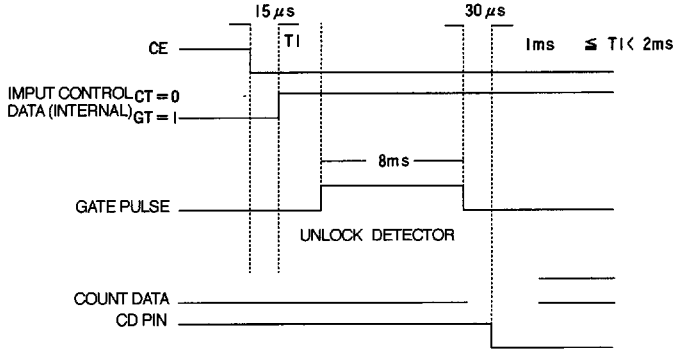
U0	U1	U2	U3					
0	0	0	0			ERR	<	7 µs
1	0	0	0	7 µs	<	ERR	<	13 µs
1	1	0	0	13 µs	<	ERR	<	26 µs
1	1	1	0	26 µs	<	ERR	<	54 µs
1	1	1	1	54 µs	<	ERR		

Operation of the frequency counter and unlock detection

When CT = 1, the frequency counter operates and unlock detection occurs.



When CT = 0 and GT = 1: only unlock detection occurs.



Explanation of the CD pin

The CD pin becomes LOW when frequency measurement or unlock detector operation ends. This makes it clear that the counter or unlock detector operation has come to an end. The counter data is synchronized to the CK pin and to the output. It is set HIGH by input of the following data.