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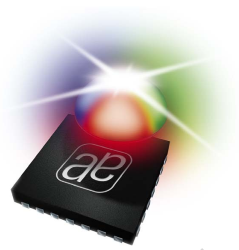
AS3687/87XM

Flexible Lighting Management (Charge Pump, DCDC Step Up, Seven Current Sinks, ADC, LED Test, Audio Light)



1 General Description

The AS3687/87XM is a highly-integrated CMOS Lighting Management Unit for mobile telephones, and other 1-cell Li+ or 3-cell NiMH powered devices.

The AS3687/87XM incorporates one Step Up DC/DC Converter for white backlight LEDs, one low noise Charge Pump for indicator- or RGB- LEDs, LED test circuit (production test of the soldered LEDs at the customer site), one Analog-to-Digital Converter, seven current sinks, a two wire serial interface, and control logic all onto a single device. Output voltages and output currents are fully programmable. The AS3687XM has an audio input to control one or two RGB LEDs.

The AS3687/87XM is a successor to the austrimicrosystems AS3689 and therefore **software compatible** to the **AS3689** (software written for the AS3689 can be easily reused for the AS3687/87XM).

2 Key Features

- High-Efficiency Step Up DC/DC Converter
  - Up to 25V/50mA for White LEDs
  - Programmable Output Voltage with External Resistors and Serial Interface
  - Overvoltage Protection
- High-Efficiency Low Noise Charge Pump
  - 1:1, 1:1.5, and 1:2 Mode
  - Automatic Up Switching (can be disabled and 1:2 mode can be blocked)
  - Output Current up to 150mA
  - Efficiency up to 95%
  - Only 4 External Capacitors Required: 2 x 500nF Flying Capacitors, 2 x 1µF Input/Output Capacitors
  - Supports LCD White Backlight or RGB LEDs
- Seven Current Sinks
  - All seven current sinks fully Programmable (8-bit) from: 0.15mA to 38.5mA (CURR1, CURR2, CURR6, CURR30, CURR31, CURR32, CURR33)
  - Three current sinks are High Voltage capable (CURR1, CURR2, CURR6)
  - Selectively Enable/Disable Current Sinks
- Internal PWM Generation
  - 8 Bit resolution
  - Autonomous Logarithmic up/down dimming
- Led Pattern Generator
  - Autonomous driving for Fun RGB LEDs
  - Support indicator LEDs
- 10-bit Successive Approximation ADC
  - 27µs Conversion Time
  - Selectable Inputs: all current sources, VBAT, CP_OUT, DCDC_FB
  - Internal Temp. Measurement
- Support for automatic LED testing (open and shorted LEDs can be identified in-circuit)
- Standby LDO always on if serial interface is on
  - Regulated 2.5V max. output 10mA
  - 3µA Quiescent Current
  - Automatic wakeup if serial interface is enabled (allows ultra low power for device shutdown)
- Audio can be used to drive RGB LED (AS3687XM only)
  - RGB Color and Brightness is dependent on audio input amplitude
  - Can drive one or two RGB LEDs
- Wide Battery Supply Range: 3.0 to 5.5V
- Two Wire Serial Interface Control
- Overcurrent and Thermal Protection
- Small Package
  WL-CSP 4x5 balls 0.5mm pitch

3 Application

Lighting-management for mobile telephones and other 1-cell Li+ or 3-cell NiMH powered devices.

4 Block Diagram

Figure 1 – Application Diagram of the AS3687/AS3687XM

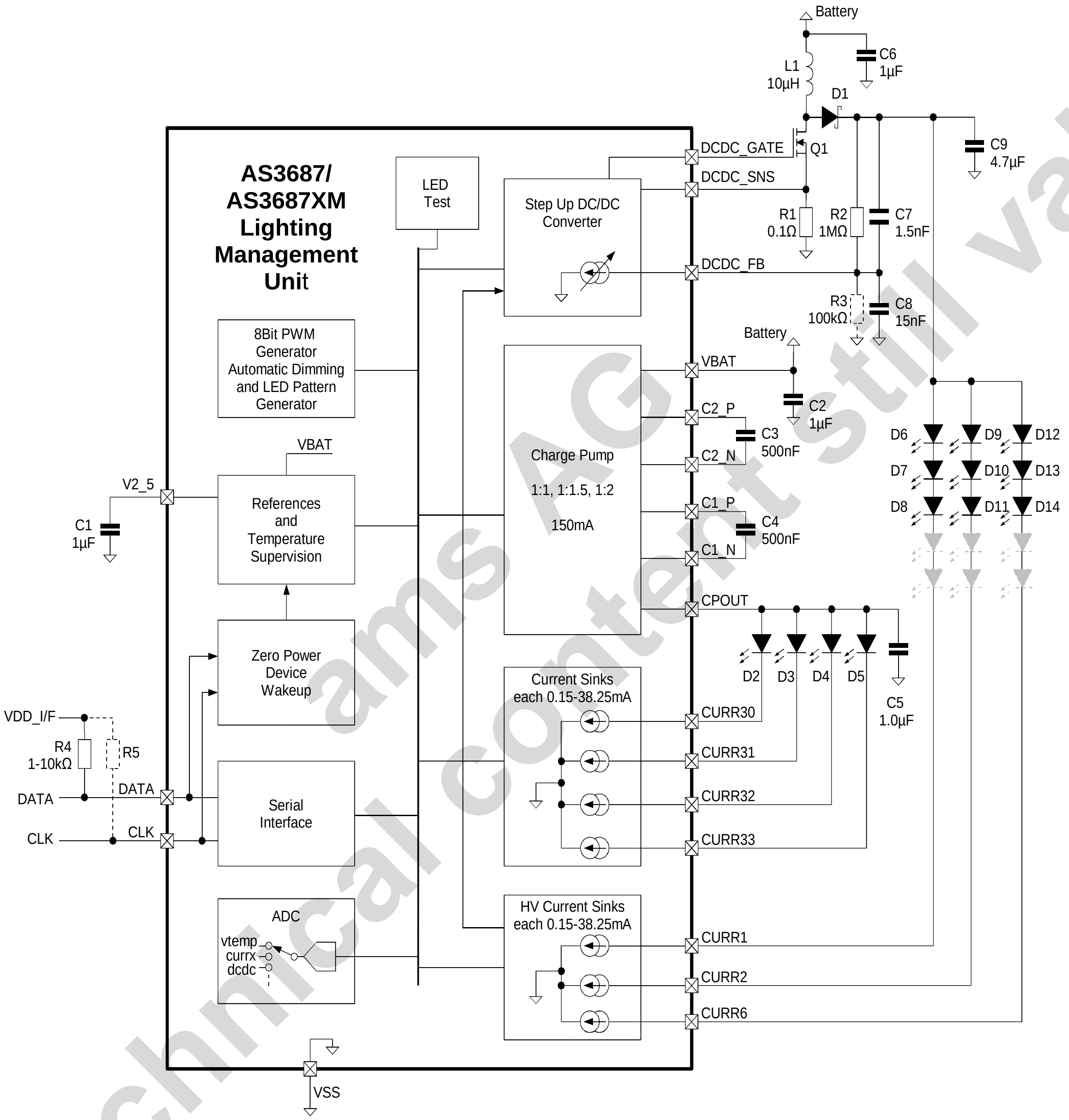


Figure 2 – Application Diagram of the AS3687XM

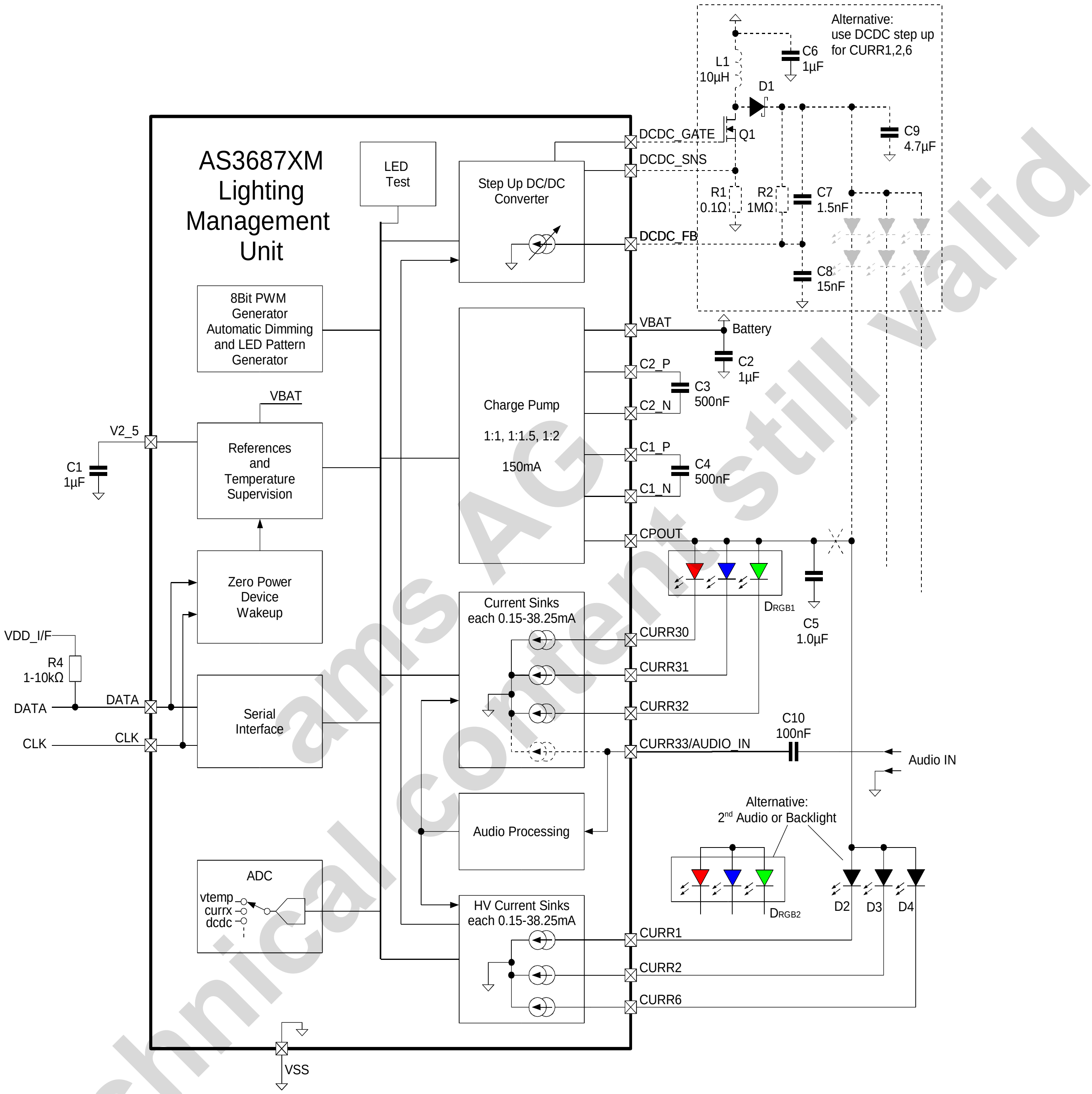


Table of Contents

1 General Description 1
2 Key Features..... 1
3 Application 1
4 Block Diagram..... 2
5 Characteristics 5
5.1 Absolute Maximum Ratings 5
5.2 Operating Conditions 5
6 Typical Operating Characteristics 6
7 Detailed Functional Description 8
7.1 Step Up DC/DC Converter..... 8
7.1.1 Feedback Selection 9
7.1.2 Overvoltage Protection in Current Feedback Mode 9
7.1.3 Voltage Feedback..... 10
7.1.4 PCB Layout Hints 11
7.1.5 Step up Registers 11
7.2 Charge Pump..... 13
7.2.1 Charge Pump Mode Switching 15
7.2.2 Soft Start..... 16
7.2.3 Charge Pump Registers 16
7.3 Current Sinks 18
7.3.1 High Voltage Current Sinks CURR1, CURR2, CURR6..... 19
7.3.2 Current Sinks CURR30, CURR31, CURR32, CURR33..... 21
7.3.3 LED Pattern Generator 24
7.3.4 PWM Generator..... 28
7.4 LED Test..... 33
7.4.1 Function Testing for single LEDs connected to the Charge Pump 33
7.4.2 Function Testing for LEDs connected to the Step Up DCDC Converter 34
7.5 Analog-To-Digital Converter 34
7.5.1 ADC Registers..... 35
7.6 Audio controlled RGB LEDs (only AS3687XM)..... 37
7.6.1 AGC..... 39
7.6.2 Audio Control Registers..... 41
7.7 Power-On Reset 42
7.7.1 Reset control register..... 43
7.8 Temperature Supervision..... 43
7.8.1 Temperature Supervision Registers 44
7.9 Serial Interface..... 44
7.9.1 Serial Interface Features 44
7.9.2 Device Address Selection..... 45
7.10 Operating Modes 47
8 Register Map..... 48
9 External Components 50
10 Pinout and Packaging 51
10.1 Pin Description..... 51
10.2 Package Drawings and Markings 52
11 Ordering Information 53

5 Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 1 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 5 Electrical Characteristics is not implied.
Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1 – Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
VIN_HV	15V Pins	-0.3	17	V	Applicable for high-voltage current sink pins CURR1,CURR2, CURR6
VIN_MV	5V Pins	-0.3	7.0	V	Applicable for 5V pins VBAT, CURR30-33, CURR33/AUDIO_IN, C1_N, C2_N, C1_P, C2_P, CPOUT, DCDC_FB, DCDC_GATE, CLK, DATA;
VIN_LV	3.3V Pins	-0.3	5.0	V	Applicable for 3.3V pins V2_5; DCDC_SNS
IIN	Input Pin Current	-25	+25	mA	At 25ºC, Norm: JEDEC 17
T_{strg}	Storage Temperature Range	-55	125	°C	
	Humidity	5	85	%	Non-condensing
VESD	Electrostatic Discharge Norm: MIL 883 E Method 3015	-2000	2000	V	All pins except CURR33/AUDIO_IN
		-1000	1000	V	Pin CURR33/AUDIO_IN
VCDM	Norm: JEDEC JESD 22-A115-A level A	-500	500	V	
P_t	Total Power Dissipation		0.75	W	T_A = 70 ºC, T_{junc_max} = 125ºC
TBODY	Peak Body Temperature		260	°C	T = 20 to 40s, in accordance with *IPC/JEDEC J-STD 020.*

5.2 Operating Conditions

Table 2 – Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
VHV	High Voltage	0.0		15.0	V	Applicable for high-voltage current sink pins CURR1, CURR2 and CURR6.
VBAT	Battery Voltage	3.0	3.6	5.5	V	VBAT
VDDI/F	Interface Supply Voltage	1.5	1.8 / 2.8	5.5	V	For serial interface pins.
V2_5	Voltage on Pin V2_5	2.4	2.5	2.6	V	Internally generated
TAMB	Operating Temperature Range	-30	25	85	°C	
IACTIVE	Battery current		70		µA	Normal Operating current – see section 'Operating Modes'; interface active (excluding current of the enabled blocks)
ISTANDBY	Standby Mode Current		5.8	13	µA	Current consumption in standby mode. Only 2.5V regulator on, interface active
ISHUTDOWN	Shutdown Mode Current		0.1	3	µA	interface inactive (CLK and DATA set to 0V)

6 Typical Operating Characteristics

Note: Typical conditions are measured at 25°C and 3.6V (unless otherwise noted).

Figure 3 – DCDC Step Up Converter: Efficiency of +15V Step Up to 15V vs. Load Current at VBAT = 3.8V

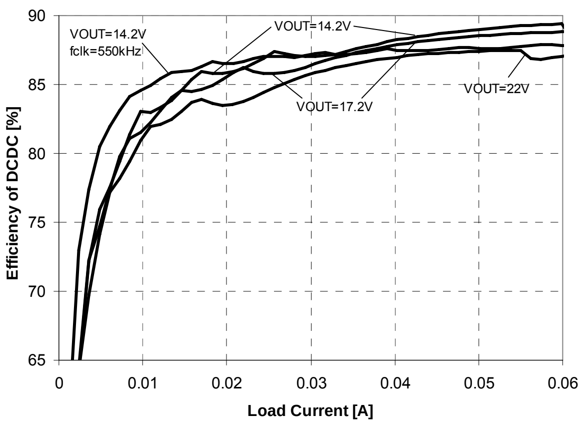


Figure 4 – Charge Pump: Efficiency vs. VBAT

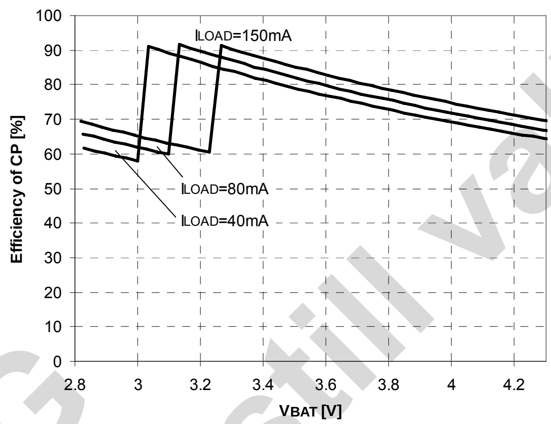


Figure 5 – Charge Pump: Battery Current vs. VBAT

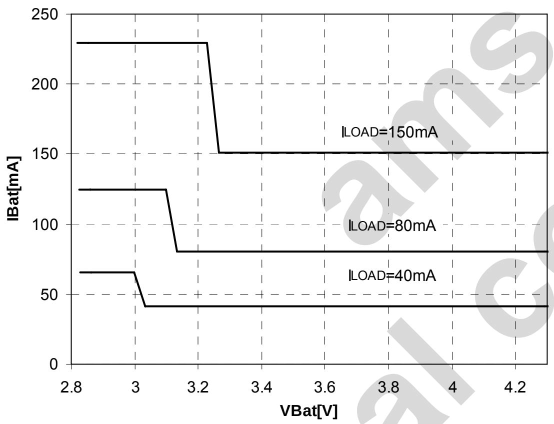


Figure 6 – Current Sink CURR1 vs. V(CURRx)

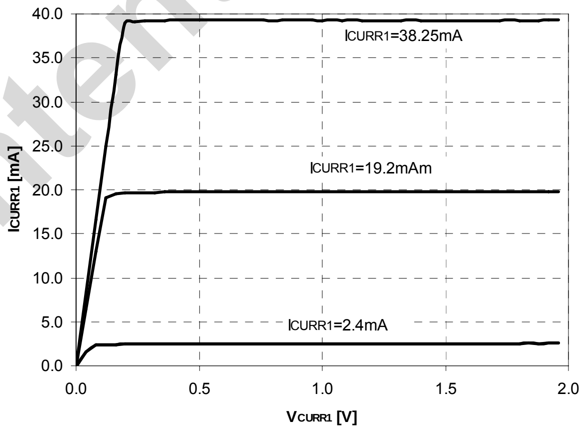
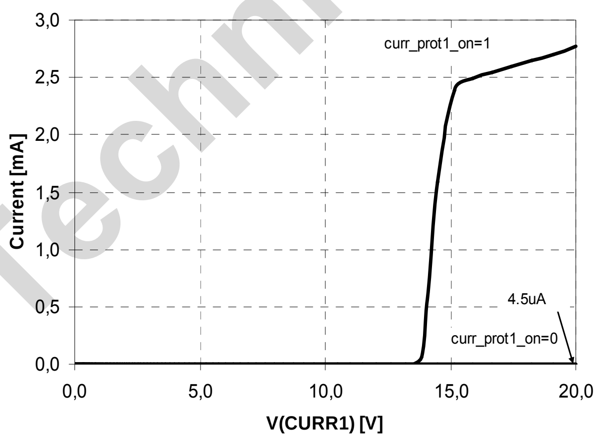


Figure 7 – Current Sink CURR1 Protection Current



Protection Current vs. Voltage (curr sinks off, curr_protX_on=0/1)

Figure 8 – Current Sink CURR3x vs. VBAT

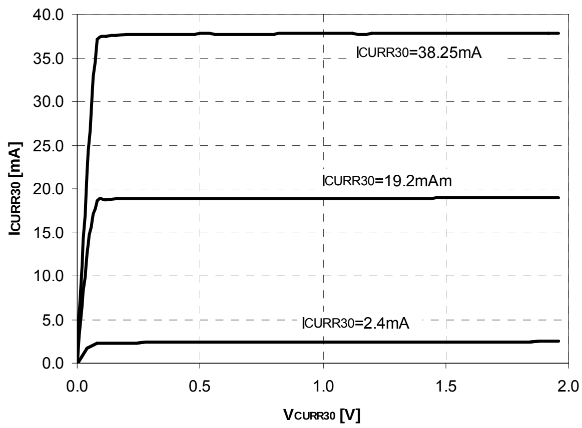
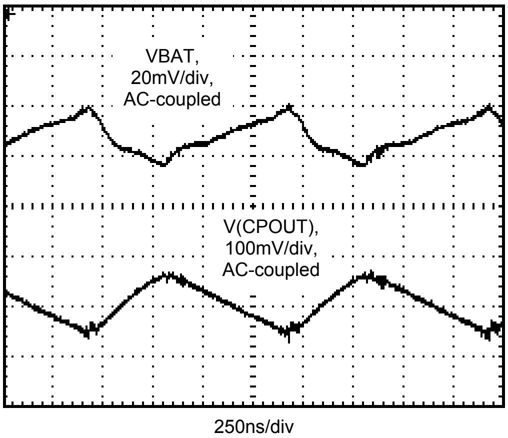
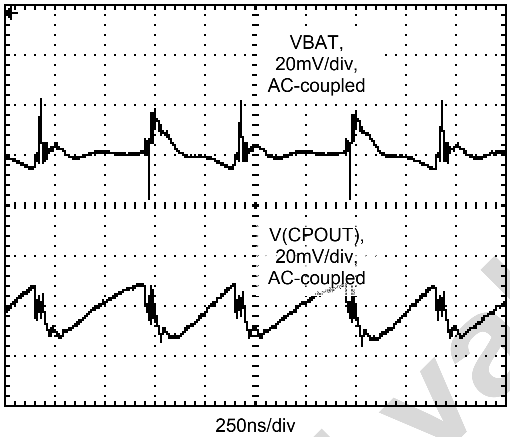


Figure 9 – Charge Pump Input and Output Ripple 1:1.5 Mode, 100mA load



Measured with battery (3.8V) on demoboard

Figure 10 – Charge Pump Input and Output Ripple 1:2 Mode, 100mA load



Measured with battery (3.0V) on demoboard

7 Detailed Functional Description

7.1 Step Up DC/DC Converter

The Step Up DC/DC Converter is a high-efficiency current mode PWM regulator, providing output voltage up to e.g. 25V/35mA or e.g. 16V/55mA. A constant switching-frequency results in a low noise on the supply and output voltages.

Figure 11 – Step Up DCDC Converter Block Diagramm Option: Current Feedback with Overvoltage protection

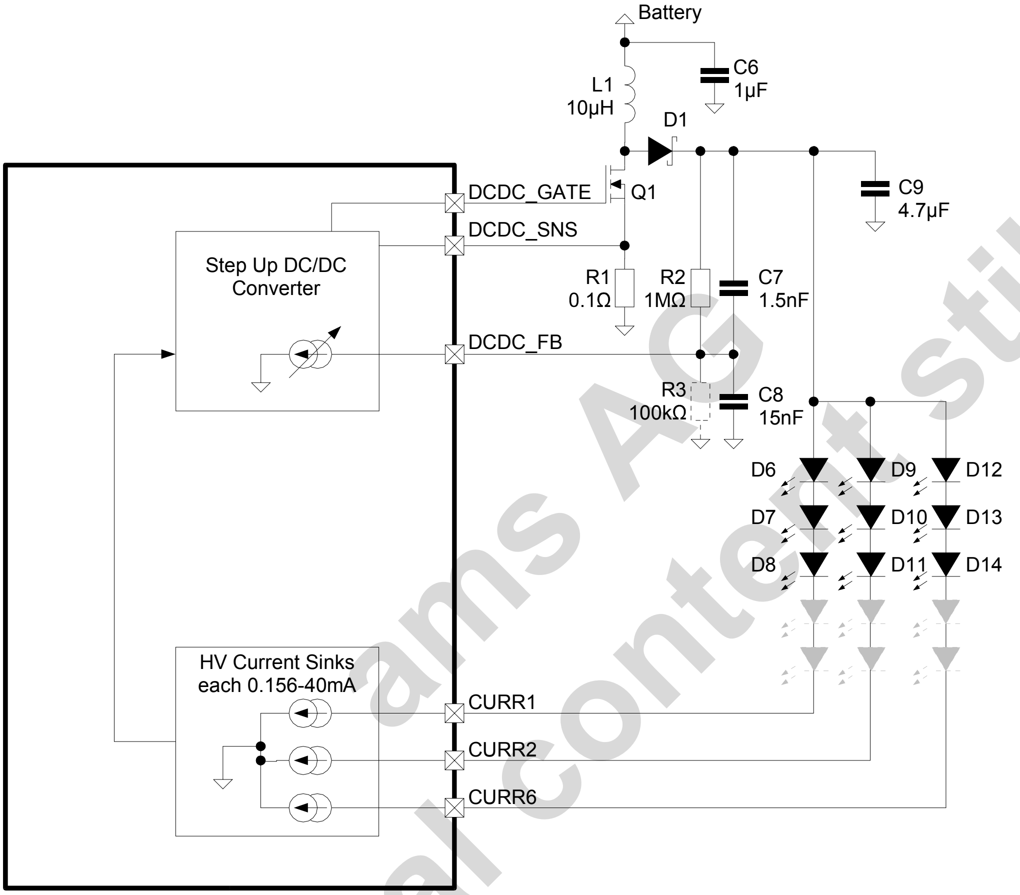


Table 3 – Step Up DC/DC Converter Parameters

Symbol	Parameter	Min	TYP	Max	Unit	Note
IVDD	Quiescent Current		140		µ A	Pulse skipping mode.
VFB1	Feedback Voltage for External Resistor Divider	1.20	1.25	1.30	V	For constant voltage control. *step_up_res* = 1
VFB2	Feedback Voltage for Current Sink Regulation	0.4	0.5	0.6	V	on CURR1, CURR2 or CURR6 in regulation. *step_up_res* = 0
IDCDC_FB	Additional Tuning Current at Pin DCDC_FB and overvoltage protection	0		31	µ A	Adjustable by software using Register DCDC control1 1µA step size (0-15µA) $V_{PROTECT}$ = 1.25V + I_{DCDC_FB} * R2
	Accuracy of Feedback Current at full scale	-6		6	%	

Table 3 – Step Up DC/DC Converter Parameters

Symbol	Parameter	Min	TYP	Max	Unit	Note
Vrsense_max	Current Limit Voltage at RSENSE (R1)	46	66	85	mV	e.g., 0.66A for 0.1Ω sense resistor
Vrsense_max_start		25	33	43		For fixed startup time of 500us
Vrsense_max_lc		30	43	57		If *stepup_lowcur*= 1
RSW	Switch Resistance			1	Ω	ON-resistance of external switching transistor.
Iload	Load Current	0		55	mA	At 16V output voltage.
		0		35		At 25V output voltage.
f_{IN}	Switching Frequency	0.9	1	1.1	MHz	Internally trimmed.
Cout	Output Capacitor	0.7	4.7		μF	Ceramic, ±20%. Use nominal 4.7μF capacitors to obtain at least 0.7μF under all conditions (voltage dependance of capacitors)
L	Inductor	7	10	13	μH	Use inductors with small $C_{parasitic}$ (<100pF) to get high efficiency.
t_{MIN_ON}	Minimum on Time	90	140	190	ns	
MDC	Maximum Duty Cycle	88	91		%	
Vripple	Voltage ripple >20kHz			160	mV	Cout=4.7uF,Iout=0..45mA, Vbat=3.0...4.2V
	Voltage ripple <20kHz			40	mV	
Efficiency	Efficiency		85		%	Iout=20mA,Vout=17V,Vbat=3.8V

To ensure soft startup of the dcdc converter, the overcurrent limits are reduced for a fixed time after enabling the dcdc converter. The total startup time for an output voltage of e.g. 25V is less than 2ms.

7.1.1 Feedback Selection

Register 12 (DCDC Control) selects the type of feedback for the Step Up DC/DC Converter.

The feedback for the DC/DC converter can be selected either by current sinks (CURR1, CURR2, CURR6) or by a voltage feedback at pin DCDC_FB. If the register bit step_up_fb_auto is set, the feedback path is automatically selected between CURR1, CURR2 and CURR6 (the lowest voltage of these current sinks is used).

Setting step_up_fb enables feedback on the pins CURR1, CURR2 or CURR6. The Step Up DC/DC Converter is regulated such that the required current at the feedback path can be supported. (Bit step_up_res should be set to 0 in this configuration)

Note: Always choose the path with the highest voltage drop as feedback to guarantee adequate supply for the other (unregulated) paths or enable the register bit step_up_fb_auto.

7.1.2 Overvoltage Protection in Current Feedback Mode

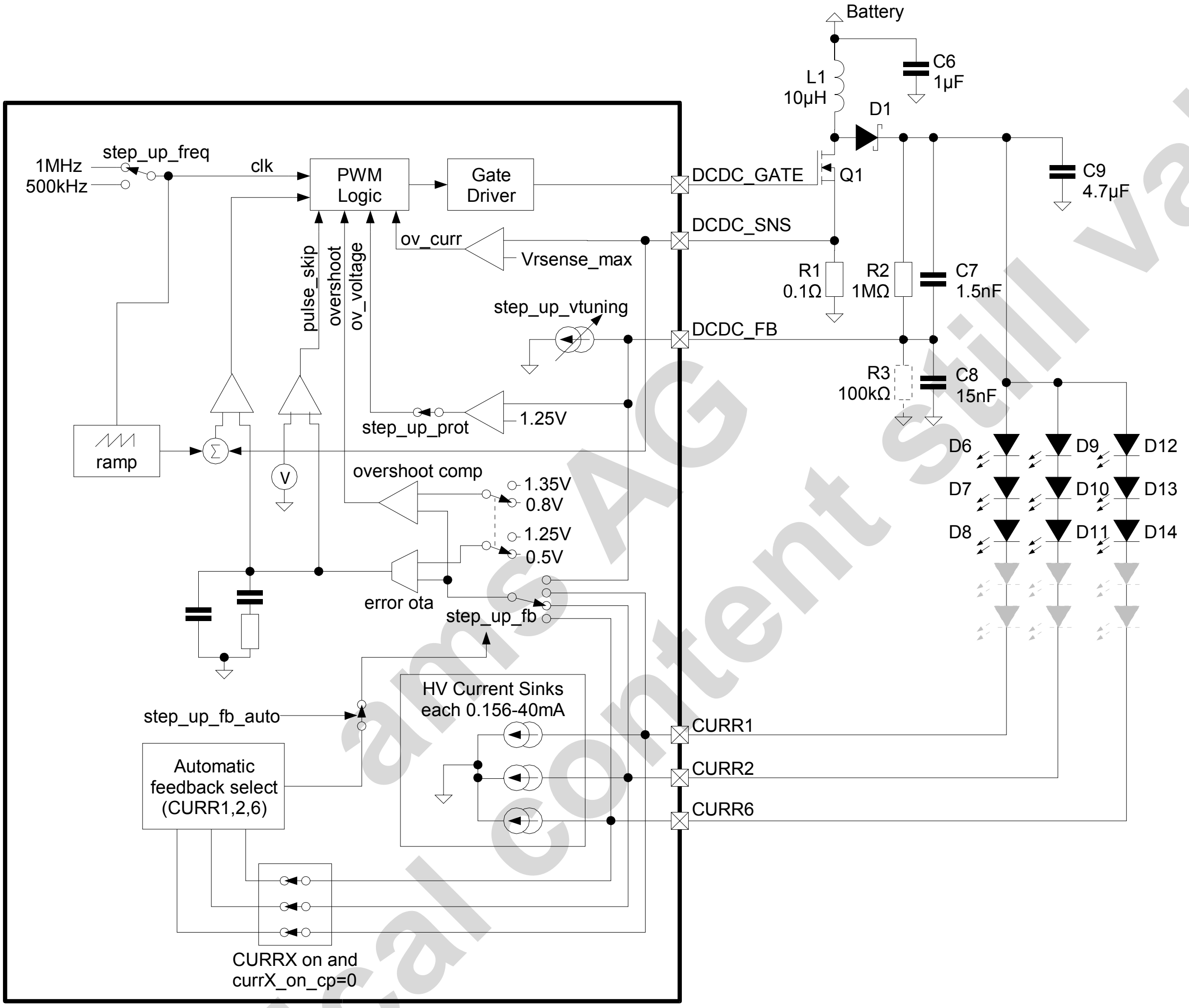
The overvoltage protection in current feedback mode (step_up_fb = 01, 10 or 11 or step_up_fb_auto = 1) works as follows: Only resistor R3 and C10/C11 is soldered and R4 is omitted. An internal current source (sink) is used to generate a voltage drop across the resistor R3. If then the voltage on DCDC_FB is above 1.25V, the DCDC is momentarily disabled to avoid too high voltages on the output of the DCDC converter.
The protection voltage can be calculated according to the following formula:

$$V_{PROTECT} = 1.25V + I_{DCDC\_FB} * R_2$$

Notes:

1. The voltage on the pin DCDC_FB is limited by an internal protection diode to VBAT + one diode forward voltage (typ. 0.6V).
2. If the overvoltage protection is not used in current feedback mode, connect DCDC_FB to ground.

Figure 12 –Step Up DC/DC Converter Detail Diagram; Option: Regulated Output Current, Feedback is automatically selected between CURR1, CURR2, CURR6 (step_up_fb_auto=1); overvoltage protection is enabled (step_up_prot=1); 1MHz clock frequency (step_up_freq=0)



7.1.3 Voltage Feedback

Setting bit step_up_fb = 00 enables voltage feedback at pin DCDC_FB..

The output voltage is regulated to a constant value, given by (Bit step_up_res should be set to 1 in this configuration)

$$U_{stepup\_out} = (R2+R3)/R3 \times 1.25 + I_{DCDC\_FB} \times R2$$

If R3 is not used, the output voltage is by (Bit step_up_res should be set to 0 in this configuration):

$$U_{stepup\_out} = 1.25 + I_{DCDC\_FB} \times R2$$

Where:

U_{stepup_out} = Step Up DC/DC Converter output voltage.

R2 = Feedback resistor R2.

R3 = Feedback resistor R3.

I_{DCDC_FB} = Tuning current at pin 29 (DCDC_FB); 0 to 31µA.

Table 4 – Voltage Feedback Example Values

$I_{vtuning}$	U_{stepup_out}	U_{stepup_out}
µ A	R2 = 1MΩ, R3 not used	R2 = 500kΩ, R3 = 50kΩ
0	-	13.75
1	-	14.25
2	-	14.75
3	-	15.25
4	-	15.75
5	6.25	16.25
6	7.25	16.75
7	8.25	17.25
8	9.25	17.75
9	10.25	18.25
10	11.25	18.75
11	12.25	19.25
12	13.25	19.75
13	14.25	20.25
14	15.25	20.75
15	16.25	21.25
…	…	…
30	31.25	28.75
31	32.25	29.25

Caution: The voltage on CURR1, CURR2 and CURR6 must not exceed 15V – see also section 'High Voltage Current Sinks'.

7.1.4 PCB Layout Hints

To ensure good EMC performance of the DCDC converter, keep its external power components C2, R2, L1, Q1, D1 and C9 close together. Connect the ground of C2, Q1 and C9 locally together and connect this path with a single via to the main ground plane. This ensures that local high-frequency currents will not flow to the battery.

7.1.5 Step up Registers

Addr: 00		Reg. Control		
		This register enables/disables the Charge Pump and the Step Up DC/DC Converter		
Bit	**Bit Name**	**Default**	**Access**	**Description**
3	step_up_on	0	R/W	Enable the step up converter 0b = Disable the Step Up DC/DC Converter. 1b = Enable the Step Up DC/DC Converter.

Addr: 21h		DCDC Control 1 This register controls the Step Up DC/DC Converter.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	step_up_frequ	0	R/W	Defines the clock frequency of the Step Up DC/DC Converter. 0 = 1 MHz 1 = 500 kHz
2:1	step_up_fb	00	R/W	Controls the feedback source if step_up_fb_auto = 0 00 = DCDC_FB enabled (external resistor divider). Set step_up_fb=00 (DCDC_FB), if external PWM is enabled for CURR1, CURR2 or CURR6 01 = CURR1 feedback enabled (feedback via white LEDs. 10 = CURR2 feedback enabled (feedback via white LEDs. 11 = CURR6 feedback enabled (feedback via white LEDs.
7:3	step_up_vtuning	00000	R/W	Defines the tuning current at pin DCDC_FB. 00000 = 0 µA 00001 = 1 µA 00010 = 2 µA … 10000 = 15 µA … 11111 = 31 µA

Addr: 22h		DCDC Control 2 This register controls the Step Up DC/DC Converter and low-voltage current sinks CURR3x.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	step_up_res	0	R/W	Gain selection for Step Up DC/DC Converter. 0 = Select 0 if Step Up DC/DC Converter is used with current feedback (CURR1, CURR2 , CURR6) or if DCDC_FB is used with current feedback only – only R1, C1 connected 1 = Select 1 if DCDC_FB is used with external resistor divider (2 resistors).
1	skip_fast	0	R/W	Step Up DC/DC Converter output voltage at low loads, when pulse skipping is active. 0 = Accurate output voltage, more ripple. 1 = Elevated output voltage, less ripple.
2	step_up_prot	1	R/W	Step Up DC/DC Converter protection. 0 = No overvoltage protection. 1 = Overvoltage protection on pin DCDC_FB enabled voltage limitation =1.25V on DCDC_FB
3	stepup_lowcur	1	R/W	Step Up DC/DC Converter coil current limit. 0 = Normal current limit 1 = Current limit reduced by approx. 33%
4	curr1_prot_on	0	R/W	0 = No overvoltage protection 1 = Pull down current switched on, if voltage exceeds 13.75V, and step_up_on=1
5	curr2_prot_on	0	R/W	0 = No overvoltage protection 1 = Pull down current switched on, if voltage exceeds 13.75V, and step_up_on=1
6	curr6_prot_on	0	R/W	0 = No overvoltage protection 1 = Pull down current switched on, if voltage exceeds 13.75V, and step_up_on=1
7	step_up_fb_auto	0	R/W	0 = step_up_fb select the feedback of the DCDC converter 1 = The feedback is automatically chosen within the current sinks CURR1, CURR2 and CURR6 (never DCDC_FB).

Addr: 22h	DCDC Control 2 This register controls the Step Up DC/DC Converter and low-voltage current sinks CURR3x.			
Bit	**Bit Name**	**Default**	**Access**	**Description**
				Only those are used for this selection, which are enabled (currX_mode must not be 00) and not connected to the charge pump (currX_on_cp must be 0). Don't use automatic feedback selection together with external PWM for the current sources CURR1, CURR2 or CURR6.

7.2 Charge Pump

The Charge Pump uses two external flying capacitors C6, C7 to generate output voltages higher than the battery voltage. There are three different operating modes of the charge pump itself:

- 1:1 Bypass Mode
  - Battery input and output are connected by a low-impedance switch
  - battery current = output current.
- 1:1.5 Mode
  - The output voltage is up to 1.5 times the battery voltage (without load), but is limited to VCPOUTmax all the time
  - battery current = 1.5 times output current.
- 1:2 Mode
  - The output voltage is up to 2 times the battery voltage (without load), but is limited to VCPOUTmax all the time
  - battery current = 2 times output current

As the battery voltage decreases, the Charge Pump must be switched from 1:1 mode to 1:1.5 mode and eventually in 1:2 mode in order to provide enough supply for the current sinks. Depending on the actual current the mode with best overall efficiency can be automatically or manually selected:

Examples:

- Battery voltage = 3.7V, LED dropout voltage = 3.5V. The 1:1 mode will be selected and there is 200mV drop on the current sink and on the Charge Pump switch. Efficiency 95%.
- Battery voltage = 3.5V, LED dropout voltage = 3.5V. The 1:1.5 mode will be selected and there is 1.5V drop on the current sink and 250mV on the Charge Pump. Efficiency 66%.
- Battery voltage = 3.8V, LED dropout voltage = 4.5V (Camera Flash). The 1:2 mode can be selected and there is 600mV drop on the current sink and 2.5V on the Charge Pump. Efficiency 60%.

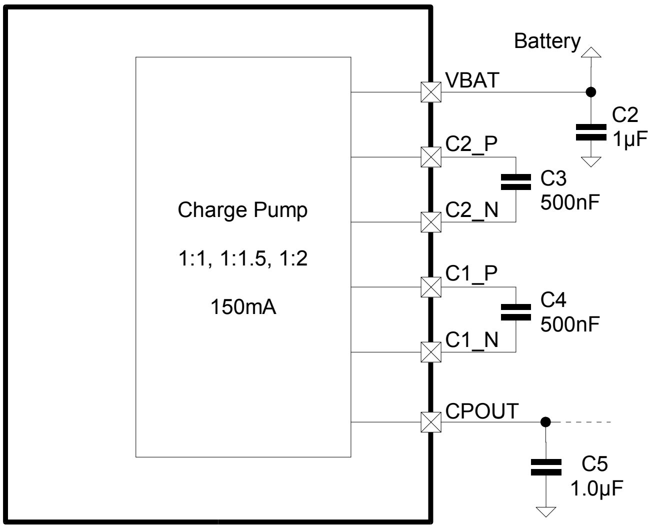
The efficiency is dependent on the LED forward voltage given by:

$$Eff=(V\_LED*Iout)/(U_{in}*I_{in})$$

The charge pump mode switching can be done manually or automatically with the following possible software settings:

- Automatic up all modes allowed (1:1, 1:1.5, 1:2)
  - Start with 1:1 mode
  - Switch up automatically 1:1 to 1:1.5 to 1:2
- Automatic up, but only 1:1 and 1:1.5 allowed
  - Start with 1:1 mode
  - Switch up automatically only from 1:1 to 1:1.5 mode; 1:2 mode is not used
- Manual
  - Set modes 1:1, 1:1.5, 1:2 by software

Figure 13 – Charge Pump Pin Connections



The Charge Pump requires the external components listed in the following table:

Table 5 – Charge Pump External Components

Symbol	Parameter	Min	Typ	Max	Unit	Note
C_2	External Decoupling Capacitor		1.0		µF	Ceramic low-ESR capacitor between pins VBAT and VSS.
C_3, C_4	External Flying Capacitor (2x)		500		nF	Ceramic low-ESR capacitor between pins C1_P and C1_N, between pins C2_P and C2_N and between VBAT and VSS.
C_5	External Storage Capacitor		1.0		µF	Ceramic low-ESR capacitor between pins CP_OUT and VSS, pins CP_OUT and VSS. Use nominal 1µF capacitors (size 0603)

Note:

1.) The connections of the external capacitors C2, C3, C4 and C5 should be kept as short as possible.

2.) The maximum voltage on the flying capacitors C3 and C4 is VBAT

Table 6 – Charge Pump Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
ICPOUT	Output Current Continuous	0.0		150	mA	Depending on PCB layout
VCPOUTmax	Output Voltage			5.5	V	Internally limited, Including output ripple
η	Efficiency	60		90	%	Including current sink loss; ICPOUT < 100mA.
$I_{CP1\_1.5}$	Power Consumption without Load fclk = 1 MHz		3.4		mA	1:1.5 Mode
I_{CP1_2}			3.8			1:2 Mode
R_{cp1_1}	Effective Charge Pump Output Resistance		0.57		Ω	1:1 Mode; V_{BAT} >= 3.5V
$R_{cp1\_1.5}$			2.65		Ω	1:1.5 Mode; V_{BAT} >= 3.3V

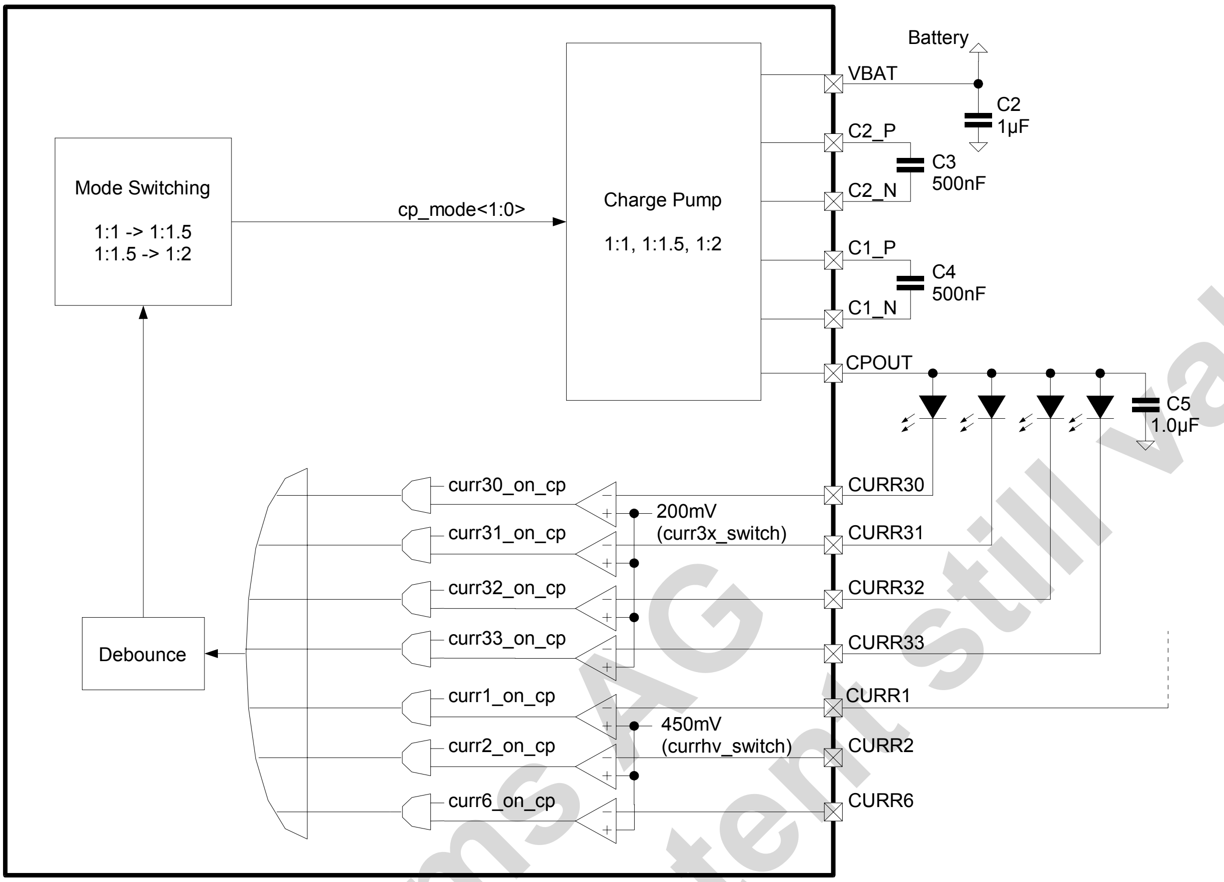
Table 6 – Charge Pump Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
R_{cp1_2}	(Open Loop, fclk = 1MHz)		3.25		Ω	1:1.2 Mode; V_{BAT} >= 3.1V
fclk Accuracy	Accuracy of Clock Frequency	-10		10	%	
currhv_switch	CURR1, 2, 6 minumum voltage			0.45	V	If the voltage drops below this threshold, the charge pump will use the next available mode (1:1 -> 1:1.5 or 1:1.5 -> 1:2)
Vcurr3x_switch	CURR30-33 minumum voltage			0.2	V	
t_{deb}	CP automatic up-switching debounce time		240		µsec	cp_start_debounce=0
			2000		µsec	After switching on CP (cp_on set to 1), if cp_start_debounce=1

7.2.1 Charge Pump Mode Switching

If automatic mode switching is enabled (cp_mode_switching = 00 or cp_mode_switching = 01) the charge pump monitors the current sinks, which are connected via a led to the output CP_OUT. To identify these current sources (sinks), the registers cp_mode_switch1 and cp_mode_switch2 (register bits curr30_on_cp … curr33_on_cp, curr1_on_cp, curr2_on_cp, curr6_on_cp) should be setup before starting the charge pump (cp_on = 1). If any of the voltage on these current sources drops below the threshold (currlv_switch, currhv_switch, curr3x_switch), the next higher mode is selected after the debounce time.
To avoid switching into 1:2 mode (battery current = 2 times output current), set cp_mode_switching = 10.
If the currX_on_cp=0 and the according current sink is connected to the chargepump, the current sink will be functional, but there is no up switching of the chargepump, if the voltage compliance is too low for the current sink to supply the specified current.

Figure 14 – Automatic Mode Switching



7.2.2 Soft Start

An implemented soft start mechanism reduces the inrush current. Battery current is smoothed when switching the charge pump on and also at each switching condition. This precaution reduces electromagnetic radiation significantly.

7.2.3 Charge Pump Registers

Addr: 00h		Reg. Control This register enables/disables the Charge Pump and the Step Up DC/DC Converter.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2	cp_on	0	R/W	0 = Set Charge Pump into 1:1 mode (off state) unless cp_auto_on is set 1 = Enable manual or automatic mode switching – see register CP Control for actual settings

Addr: 23h		CP Control This register controls the Charge Pump.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	cp_clk	0	R/W	Clock frequency selection. 0 = 1 MHz 1 = 500 kHz
2:1	cp_mode	00b	R/W	Charge Pump mode (in manual mode sets this mode, in automatic mode reports the actual mode used) 00 = 1:1 mode 01 = 1:1.5 mode 10 = 1:2 mode 11 = NA **Note:** Direct switching from 1:1.5 mode into 1:2 in manual mode and vice versa is not allowed. Always switch over 1:1 mode.
4:3	cp_mode_switching	00b	R/W	Set the mode switching algorithm: 00 = Automatic Mode switching; 1:1, 1:1.5 and 1:2 allowed[1] 01 = Automatic Mode switching; only 1:1 and 1:1.5 allowed[1] 10 = Manual Mode switching; register cp_mode defines the actual charge pump mode used 11 = reserved
5	cp_start_debounce	0	R/W	0 = Mode switching debounce timer is always 240us 1 = Upon startup (cp_on set to 1) the mode switching debounce time is first started with 2ms then reduced to 240us
6	cp_auto_on	0	R/W	0 = Charge Pump is switched on/off with cp_on 1 = Charge Pump is automatically switched on if a current sink, which is connected to the charge pump (defined by registers CP Mode Switch 1 & 2) is switched on

Note :

1. Don't use automatic mode switching together with external PWM for the current sources connceted to the charge pump with less than 500us high time.

Addr: 24h		CP Mode Switch 1 Setup which current sinks are connected (via leds) to the charge pump; if set to '1' the correspond current source (sink) is used for automatic mode selection of the charge pump		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr30_on_cp	0	R/W	0 = current Sink CURR30 is not connected to charge pump 1 = current sink CURR30 is connected to charge pump
1	curr31_on_cp	0	R/W	0 = current Sink CURR31 is not connected to charge pump 1 = current sink CURR31 is connected to charge pump
2	curr32_on_cp	0	R/W	0 = current Sink CURR32 is not connected to charge pump 1 = current sink CURR32 is connected to charge pump
3	curr33_on_cp	0	R/W	0 = current Sink CURR33 is not connected to charge pump 1 = current sink CURR33 is connected to charge pump

Addr: 25h		**CP Mode Switch 2** Setup which current sinks are connected (via leds) to the charge pump; if set to ‘1’ the correspond current source (sink) is used for automatic mode selection of the charge pump		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr1_on_cp	0	R/W	0 = current Sink CURR1 is not connected to charge pump 1 = current sink CURR1 is connected to charge pump
1	curr2_on_cp	0	R/W	0 = current Sink CURR2 is not connected to charge pump 1 = current sink CURR2 is connected to charge pump
7	curr6_on_cp	0	R/W	0 = current Sink CURR6 is not connected to charge pump 1 = current sink CURR6 is connected to charge pump

Addr: 2Ah		**Curr low voltage status 1** Indicates the low voltage status of the current sinks. If the currX_low_v bit is set, the voltage on the current sink is too low, to drive the selected output current		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr30_low_v	1	R	0 = voltage of current Sink CURR30 >curr3x_switch 1 = voltage of current Sink CURR30 <curr3x_switch
1	curr31_low_v	1	R	0 = voltage of current Sink CURR31 >curr3x_switch 1 = voltage of current Sink CURR31 <curr3x_switch
2	curr32_low_v	1	R	0 = voltage of current Sink CURR32 >curr3x_switch 1 = voltage of current Sink CURR32 <curr3x_switch
3	curr33_low_v	1	R	0 = voltage of current Sink CURR33 >curr3x_switch 1 = voltage of current Sink CURR33 <curr3x_switch
7	curr6_low_v	0	R	0 = voltage of current Sink CURR6 >currlv_switch 1 = voltage of current Sink CURR6 <currlv_switch

Addr: 2Bh		**Curr low voltage status 2** Indicates the low voltage status of the current sinks. If the currX_low_v bit is set, the voltage on the current sink is too low, to drive the selected output current		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr1_low_v	0	R	0 = voltage of current Sink CURR1 >currhv_switch 1 = voltage of current Sink CURR1 <currhv_switch
1	curr2_low_v	0	R	0 = voltage of current Sink CURR2 >currhv_switch 1 = voltage of current Sink CURR2 <currhv_switch

7.3 Current Sinks

The AS3687/87XM contains general purpose current sinks intended to control backlights, buzzers, and vibrators. All current sinks have an integrated protection against overvoltage.

CURR1, CURR2 and CURR6 is also used as feedback for the Step Up DC/DC Converter (regulated to 0.5V in this configuration).

- Current sinks CURR1, CURR2 and CURR6 are high-voltage compliant (15V) current sinks, used e.g., for series of white LEDs
- Current sinks CURR3*x* (CURR30, CURR31, CURR32 and CURR33) are parallel 5V current sinks, used for backlighting or indicator LEDs.

7.3.1 High Voltage Current Sinks CURR1, CURR2, CURR6

The high voltage current sinks have a resolution of 8 bits. Additionally an internal protection circuit monitors with a voltage divider (max 3µA @ 15) the voltage on CURR1, CURR2 and CURR6 and increases the current in off state in case of overvoltage.

Table 8 – HV - Current Sinks Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{BIT7}	Current sink if Bit7 = 1		19.2		mA	For V(CURRx) > 0.45V
I_{BIT6}	Current sink if Bit6 = 1		9.6			
I_{BIT5}	Current sink if Bit5 = 1		4.8			
I_{BIT4}	Current sink if Bit4 = 1		2.4			
I_{BIT3}	Current sink if Bit3 = 1		1.2			
I_{BIT2}	Current sink if Bit2 = 1		0.6			
I_{BIT1}	Current sink if Bit1 = 1		0.3			
I_{BIT0}	Current sink if Bit0 = 1		0.15			
Δm	matching Accuracy	-10		+10	%	CURR1,CURR2,CURR6
Δ	absolute Accuracy	-15		+15	%	
V_{CURRx}	Voltage compliance	0.45		15	V	
Ov_prot_ 13V	Overvoltage Protection of current sink CURR1,2,6			3.0	µA	At 13V, independent of curr1_prot_on, curr2_prot_on or curr6_prot_on
Ov_prot_ 15V	Overvoltage Protection of current sink CURR1,2,6	0.8		4.0	mA	At 15V, step_up_on=1, curr1_prot_on=1 for CURR1, curr2_prot_on=1 for CURR2, curr6_prot_on=1 for CURR6

7.3.1.1 High Voltage Current Sinks CURR1, CURR2, CURR6 Registers

Addr: 09h		**Curr1 current**		
		This register controls the High voltage current sink current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr1_current	0	R/W	Defines current into Current sink curr1 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

Addr: 0Ah		**Curr2 current**		
		This register controls the High voltage current sink current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr2_current	0	R/W	Defines current into Current sink curr2 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

Addr: 2Fh		Curr6 current This register controls the High voltage current sink current.		
Bit	Bit Name	Default	Access	Description
7:0	curr6_current	0	R/W	Defines current into Current sink curr6 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

Addr: 01h		curr12 control This register select the mode of the current sinkscontrols High voltage current sink current.		
Bit	Bit Name	Default	Access	Description
1:0	curr1_mode	0	R/W	Select the mode of the current sink curr1 00b = off 01b = on 10b = PWM controlled 11b = LED pattern controlled
3:2	curr2_mode	0	R/W	Select the mode of the current sink curr2 00b = off 01b = on 10b = PWM controlled 11b = LED pattern controlled

Addr: 02h		curr 6 control This register select the mode of the current sinks CURR6		
Bit	Bit Name	Default	Access	Description
7:6	curr6_mode	0	R/W	Select the mode of the current sink CURR6 00b = off 01b = on 10b = PWM controlled 11b = LED pattern controlled

Addr: 22h		DCDC Control 2 This register controls the Step Up DC/DC Converter and low-voltage current sinks CURR3x.		
Bit	Bit Name	Default	Access	Description
0	step_up_res	0	R/W	Gain selection for Step Up DC/DC Converter. Select 0 if Step Up DC/DC Converter is used with current feedback (CURR1, CURR2) or if DCDC_FB is used with current feedback only – only R1, C1 connected Select 1 if DCDC_FB is used with external resistor divider (2 resistors).
1	skip_fast	0	R/W	Step Up DC/DC Converter output voltage at low loads, when pulse skipping is active. 0 = Accurate output voltage, more ripple. 1 = Elevated output voltage, less ripple.
2	stepup_prot	1	R/W	Step Up DC/DC Converter protection. 0 = No overvoltage protection. 1 = Overvoltage protection on pin DCDC_FB enabled voltage limitation =1.25V on DCDC_FB

Addr: 22h		DCDC Control 2 This register controls the Step Up DC/DC Converter and low-voltage current sinks CURR3x.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
3	stepup_lowcur	1	R/W	Step Up DC/DC Converter coil current limit. 0: Normal current limit 1: Current limit reduced by approx. 33%
4	curr1_prot_on	0	R/W	0 = No overvoltage protection 1 = Pull down current on CURR1 switched on, if voltage on CURR1 exceeds 13.75V, and step_up_on=1
5	curr2_prot_on	0	R/W	0 = No overvoltage protection 1 = Pull down current on CURR2 switched on, if voltage exceeds on CURR2 13.75V, and step_up_on=1
6	curr6_prot_on	0	R/W	0 = No overvoltage protection 1 = Pull down current on CURR6 switched on, if voltage on CURR6 exceeds 13.75V, and step_up_on=1
7	step_up_fb_auto	0	R/W	0 = step_up_fb select the feedback of the DCDC converter 1 = The feedback is automatically chosen within the current sinks CURR1and CURR2 (never DCDC_FB). Only those are used for this selection, which are enabled (currX_mode must not be 00) and not connected to the charge pump (currX_on_cp must be 0).

7.3.2 Current Sinks CURR30, CURR31, CURR32, CURR33

These current sinks have a resolution of 8 bits and can sink up to 40mA. The current values can be controlled individually with ***curr30_current*** – ***curr33_current*** or common with ***curr3x_strobe*** or ***curr3x_preview***.

Table 9 – Current Sinks CURR30,31,32,33 Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{BIT7}	Current sink if Bit7 = 1		19.2		mA	For V(CURR3x) > 0.2V
I_{BIT6}	Current sink if Bit6 = 1		9.6			
I_{BIT5}	Current sink if Bit5 = 1		4.8			
I_{BIT4}	Current sink if Bit4 = 1		2.4			
I_{BIT3}	Current sink if Bit3 = 1		1.2			
I_{BIT2}	Current sink if Bit2 = 1		0.6			
I_{BIT1}	Current sink if Bit1 = 1		0.3			
I_{BIT0}	Current sink if Bit0 = 1		0.15			
Δm	matching Accuracy	-10		+10	%	CURR30-33
Δ	absolute Accuracy	-15		+15	%	
V_{CURR3X}	Voltage compliance	0.2		CPOUT	V	

7.3.2.1 Current Sinks CURR3x Registers

Addr: 12h		Curr3 control1 This register select the modes of the current sinks30..33 current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	preview_off_after strobe	0b	R/W	Select the switch off mode after strobe pulse 0 = normal preview/strobe mode, 1 = switch off preview after strobe duration has expired. To reinitiate the torch mode the preview_ctrl has to be set off and on again

Addr: 12h		**Curr3 control1**		
		This register select the modes of the current sinks30..33 current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2:1	preview_ctrl	00b	R/W	Preview is triggered by 00 = off 01 = software trigger (setting this bit automatically triggers preview)

Addr: 11h		**Curr3 strobe control**		
		This register select the modes of the current sinks30..33 current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	strobe_ctrl	00b	R/W	Strobe is triggered by 00b = off 01b = software trigger (setting this bit automatically triggers strobe)
3:2	strobe_mode	00b	R/W	Selects strobe mode 00b = Mode1 (Tstrobe=Ts; strobe trigger signal >= 10µs) 01b = Mode 2 (Tstrobe=max Ts) 10b = Mode 3 (Tstrobe = strobe signal) 11b = not used
7:4	strobe_timing	0000b	R/W	Selects strobe time (Ts) 0000b = 100 msec 0001b = 200 msec 0010b = 300 msec 0011b = 400 msec 0100b = 500 msec 0101b = 600 msec 0110b = 700 msec 0111b = 800 msec 1000b = 900 msec 1001b = 1000 msec 1010b = 1100 msec 1011b = 1200 msec 1100b = 1300 msec 1101b = 1400 msec 1110b = 1500 msec 1111b = 1600 msec

Addr: 0Eh		**Curr3x strobe**		
		This register select the strobe current of the current sinks30..33		
Bit	**Bit Name**	**Default**	**Access**	**Description**
5:0	curr3x_strobe	00	R/W	Defines Strobe current of Current sinks curr30-33 00h = 0 mA 01h = 0.6 mA ... 3Fh = 37.8 mA

Addr: 0Fh		**Curr3x preview**		
		This register select the preview current of the current sinks30..33		
Bit	**Bit Name**	**Default**	**Access**	**Description**
5:0	curr3x_preview	00	R/W	Defines Preview current of Current sinks curr30-33 00h = 0 mA 01h = 0.6 mA ... 3Fh = 37.8 mA

Addr: 10h		Curr3x other		
		This register selects the current of the current sinks30..33		
Bit	**Bit Name**	**Default**	**Access**	**Description**
5:0	curr3x_other	00	R/W	Selects curr30 current, if curr30 is not used for strobe/preview (curr30_mode=11b) 00h = 0 mA 01h = 0.6 mA ... 3Fh = 37.8 mA

Addr: 40h		Curr30 Current		
		This register selects the current of the current sink30		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr30_current	00	R/W	Selects curr30 current, if curr30 is not used for strobe/preview (curr30_mode=11b) 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

Addr: 41h		Curr31 Current		
		This register selects the current of the current sink31		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr31_current	00	R/W	Selects curr30 current, if curr30 is not used for strobe/preview (curr30_mode=11b) 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

Addr: 42h		Curr32 Current		
		This register selects the current of the current sink32		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr32_current	00	R/W	Selects curr32 current, if curr32 is not used for strobe/preview (curr32_mode=11b) 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

Addr: 43h		Curr33 Current		
		This register selects the current of the current sink33		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	curr33_current	00	R/W	Selects curr33 current, if curr33 is not used for strobe/preview (curr33_mode=11b) 00h = 0 mA 01h = 0.15 mA ... FFh = 38.25 mA

Addr: 03h		curr3 control This register select the mode of the current sinks30 - 33		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	curr30_mode	0	R/W	Select the mode of the current sink curr30 00b = off 01b = strobe/preview 10b = curr30_other PWM controlled 11b = curr30_current [1)]
3:2	curr31_mode	0	R/W	Select the mode of the current sink curr31 00b = off 01b = strobe/preview 10b = curr31_other PWM controlled 11b = curr31_current [1)]
5:4	curr32_mode	0	R/W	Select the mode of the current sink curr32 00b = off 01b = strobe/preview 10b = curr32_other PWM controlled 11b = curr32_current [1)]
7:6	curr33_mode	0	R/W	Select the mode of the current sink curr33 00b = off 01b = strobe/preview 10b = curr33_other PWM controlled 11b = curr33_current [1)]

[1)] don't use this mode (11b) if softdim_pattern=1, use strobe/preview instead

Addr: 18h		Pattern control This register controls the LED pattern		
Bit	**Bit Name**	**Default**	**Access**	**Description**
4	curr30_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR30 controlled according curr30_mode register 1b = CURR30 controlled by LED pattern generator
5	curr31_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR31 controlled according curr31_mode register 1b = CURR31 controlled by LED pattern generator
6	curr32_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR32 controlled according curr32_mode register 1b = CURR32 controlled by LED pattern generator
7	curr33_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR33 controlled according curr33_mode register 1b = CURR33 controlled by LED pattern generator

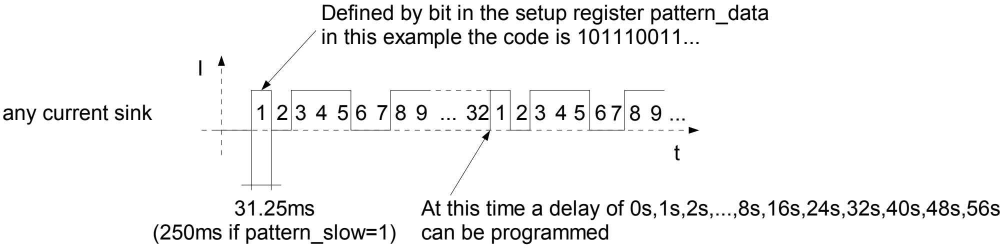
7.3.3 LED Pattern Generator

The LED pattern generator is capable of producing a pattern with 32 bits length and 1 second duration (31.25ms for each bit). The pattern itself can be started every second, every 2^{nd}, 3^{rd} or 4^{th} second.

With this pattern all current sinks can be controlled. The pattern itself switches the configured current sources between 0 and their programmed current.

If everything else is switched off, the current consumption in this mode is I_{ACTIVE}. (excluding current through switched on current source) and the charge pump, if required. The charge pump can be automatically switched on/off depending on the pattern (see register cp_auto_on in the charge pump section) to reduce the overall current consumption.

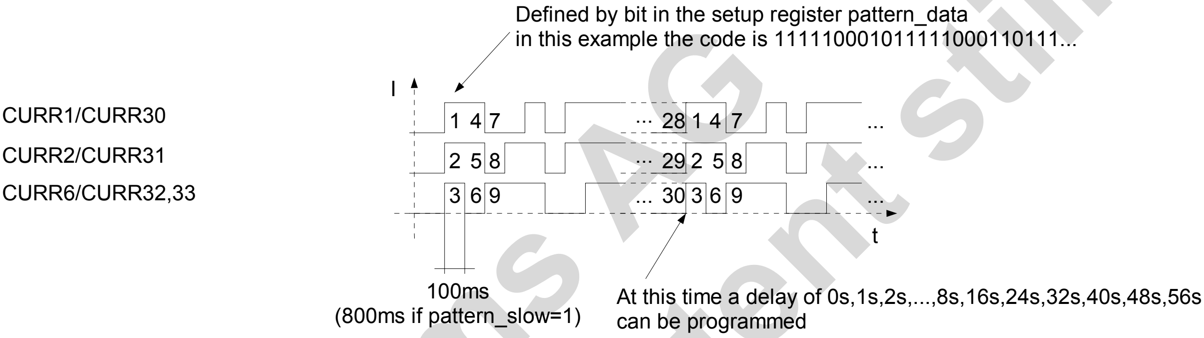
Figure 15 – LED Pattern Generator AS3687/87XM for pattern_color = 0



To select the different current sinks to be controlled by the LED pattern generator, see the 'xxxx'_mode registers (where 'xxxx' stands for the to be controlled current sink, e.g. curr1_mode for CURR1 current sink). See also the descirption of the different current sinks.

To allow the generator of a color patterns set the bit pattern_color to '1'. Then the pattern can be connected to CURR30-32 as follows:

Figure 16 – LED Pattern Generator AS3687/87XM for pattern_color = 1



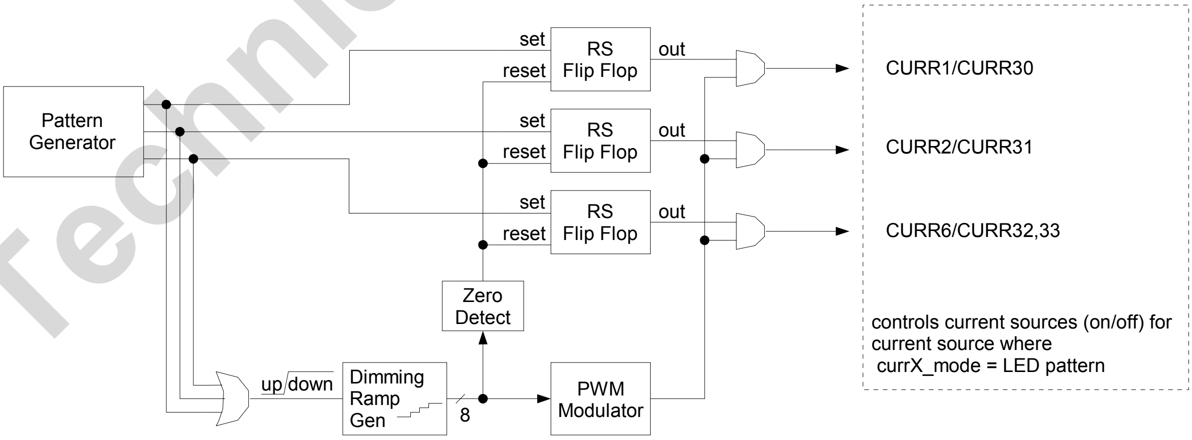
Only those current sinks will be controlled, where the 'xxxx'_mode register is configured for LED pattern.

If the register bit pattern_slow is set, all pattern times are increased by a factor of eigth. (bit duration: 250ms if pattern_color=0 / 800ms if pattern_color=1, delays between pattern up to 24s).

7.3.3.1 Soft Dimming for Pattern

The internal pattern generator can be combined with the internal pwm dimming modulator to obtain as shown in the following figure:

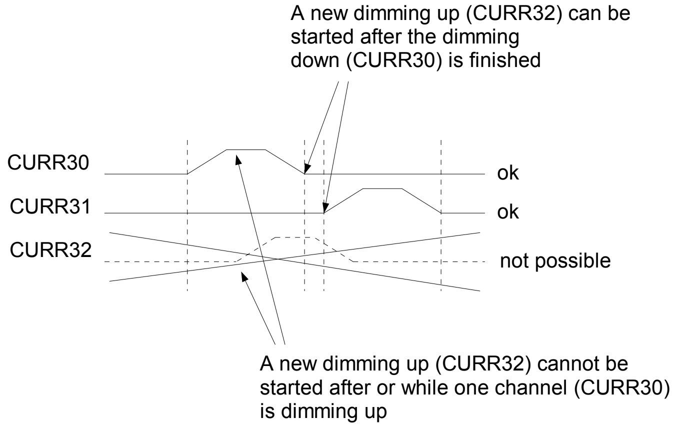
Figure 17 – Softdimming Architecture for the AS3687/87XM (softdim_pattern=1 and pattern_color = 1)



With the AS3687/87XM smooth fade-in and fade-out effects can be automatically generated.

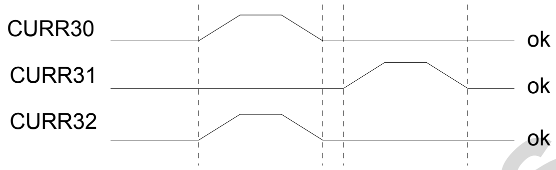
As there is only one dimming ramp generator and one pwm modulator following constraints have to be considered when setting up the pattern (applies only if pattern_color=1):

Figure 18 – Softdimming example Waveform for CURR30-32



However using the identical dimming waveform for two channels is possible as shown in the following figure:

Figure 19 – Softdimming example Waveform for CURR30-32



7.3.3.2 LED Pattern Registers

Addr: 19h,1Ah,1Bh,1Ch		Pattern data0, Pattern data1, Pattern data2, Pattern data3		
		This registers contains the pattern data for the current sinks.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	pattern_data0[7:0] [1]	0	R/W	Pattern data0
7:0	pattern_data1[15:8] [1]	0	R/W	Pattern data1
7:0	pattern_data2[23:16] [1]	0	R/W	Pattern data2
7:0	pattern_data3[31:24] [1]	0	R/W	Pattern data3

Note:

1. Update any of the pattern register only if none of the current sources is connected to the pattern generator (‘xxxx’_mode must not be 11b). The pattern generator is automatically started at the same time when any of the current sources is connected to the pattern generator

Addr: 18h		Pattern control This register controls the LED pattern		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	pattern_color	0	R/W	Defines the pattern type for the current sinks 0b = single 32 bit pattern (also set currX_mode = 11) 1b = RGB pattern with each 10 bits (set all currX_mode = 11)
2:1	pattern_delay	00b	R/W	Delay between pattern, details see table *LED Pattern timing;* together with pattern_delay2 sets the delay time between patterns
3	softdim_pattern	0b	R/W	Enable the 'soft' dimming feature for the pattern generator 0 = Pattern generator directly control current sources 1 = 'Soft Dimming' is performed – see section 'Soft Dimming for pattern'
4	curr30_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR30 controlled according curr30_mode register 1b = CURR30 controlled by LED pattern generator
5	curr31_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR31 controlled according curr31_mode register 1b = CURR31 controlled by LED pattern generator
6	curr32_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR32 controlled according curr32_mode register 1b = CURR32 controlled by LED pattern generator
7	curr33_pattern	0b	R/W	Additional CURR33 LED pattern control bit 0b = CURR33 controlled according curr33_mode register 1b = CURR33 controlled by LED pattern generator

Addr: 2Ch		gpio_current		
Bit	**Bit Name**	**Default**	**Access**	**Description**
4	pattern_delay2	0	R/W	Delay between pattern see table *LED Pattern timing;* together with pattern_delay sets the delay time between patterns
6	pattern_slow	0	R/W	Pattern timing control 0b = normal mode 1b = slow mode (all pattern times are increased by a factor of eight)

Figure 20 –LED Pattern timing

pattern_slow	pattern_delay2	pattern_delay[1..0]	bit duration [ms]		delay [s] between patterns	pattern duration [s] (total cycle time: pattern + delay)
	delay between patterns		pattern_color=0	pattern_color=1		
0	0	00	31	100	0[1]	1
0	0	01	31	100	1	2
0	0	10	31	100	2	3
0	0	11	31	100	3	4
0	1	00	31	100	4	5
0	1	01	31	100	5	6
0	1	10	31	100	6	7
0	1	11	31	100	7	8
1	0	00	250	800	0	8

[1] Even by setting 000 for pattern delay, there is a small delay before the new patterns starts.

Figure 20 –LED Pattern timing

pattern_slow	pattern_delay2	pattern_delay[1..0]	bit duration [ms]		delay [s]	pattern duration [s]
	delay between patterns		pattern_color=0	pattern_color=1	between patterns	(total cycle time: pattern + delay)
1	0	01	250	800	8	16
1	0	10	250	800	16	24
1	0	11	250	800	24	32
1	1	00	250	800	32	40
1	1	01	250	800	40	48
1	1	10	250	800	48	56
1	1	11	250	800	56	64

7.3.4 PWM Generator

The PWM generator can be used for any current sink (CURR1, CURR2, CURR3x, CURR6). The setting applies for all current sinks, which are controlled by the pwm generator (e.g. CURR1 is pwm controlled if curr1_mode = 10). The pwm modulated signal can switch on/off the current sinks and therefore depending on its duty cycle change the brightness of an attached LED.

7.3.4.1 Internal PWM Generator

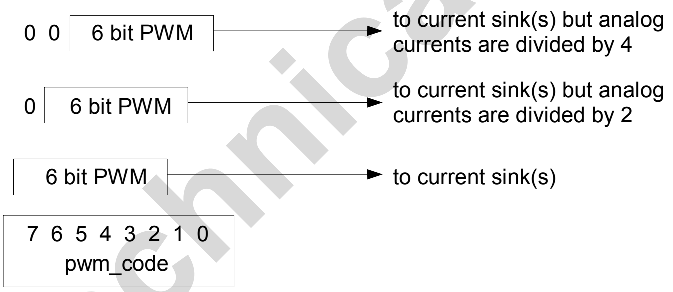
The internal PWM generator uses the 2MHz internal clock as input frequency and its dimming range is 6 bits digital (2MHz / 2^6 = 31.3kHz pwm frequency) and 2 bits analog. Depending on the actual code in the register 'pwm_code' the following algorithm is used:

- If pwm_code bit 7 = 1
  Then the upper 6 bits (Bits 7:2) of pwm_code are used for the 6 bits PWM generation, which controls the selected currents sinks directly

- If pwm_code bit 7 =0 and bit 6 = 1
  Then bits 6:1 of pwm_code are used for the 6 bits PWM generation. This signal controls the selected current sinks, but the analog current of these sinks is divided by 2

- If pwm_code bit 7 and bit 6 = 0
  Then bits 5:0 of pwm_code are used for the 6 bits PWM generation. This signal controls the selected current sinks, but the analog current of these sinks is divided by 4

Figure 21 – PWM Control

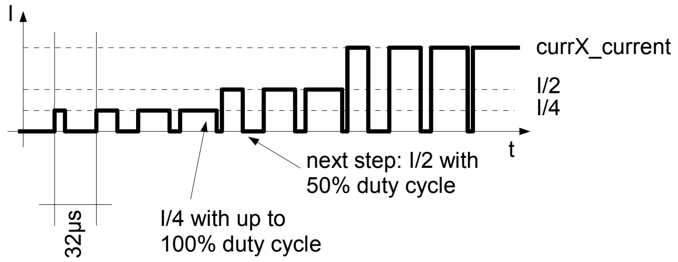


Automatic Up/Down Dimming

If the register pwm_dim_mode is set to 01 (up dimming) or 10 (down dimming) the value within the register pwm_code is increased (up dimming) or decreased (down dimming) every time and amount (either 1/4th or 1/8th) defined by the register pwm_dim_speed. The maximum value of 255 (completely on) and the minimum value of 0 (off) is never exceeded. It is used to smoothly and automatically dim the brightness of the LEDs connceted to any of the current sinks. The PWM code is readable all the time (Also during up and down dimming)

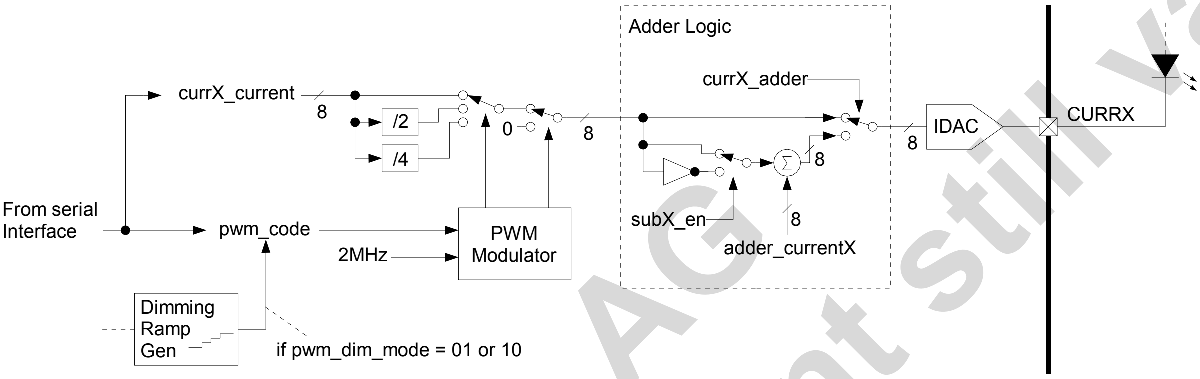
The waveform for up dimming looks as follows (cycles omitted for simplicity):

Figure 22 – PWM Dimming Waveform for up dimming (pwm_dim_mode = 01); currX_mode = PWM controlled (not all steps shown)



The internal pwm modulator circuit controls the current sinks as shown in the following figure:

Figure 23 – PWM Control Circuit (currX_mode = 10b (PWM controlled)); X = any current sink



The adder logic (available for CURR30-32, CURR1, CURR2 and CURR6) is intended to allow dimming not only from 0% to 100% (or 100% to 0%) of currX_current, but also e.g. from 10% to 110% (or 110% to 10%) of currX_current. That means for up dimming the starting current is defined by 0 + currX_adder and the end current is defined by currX_current + currX_adder.
An overflow of the internal bus (8 Bits wide to the IDAC) has to be avoided by the register settings (currX_current + currX_adder must not exceed 255).

If the register subX_en is set, the result from the pwm_modulator is inverted logically. That means for up dimming the starting current is defined by currX_adder - 1 and the end current is defined by currX_adder - currX_current - 1. An overflow of the internal bus (8 Bits wide to the IDAC) has to be avoided by the register settings (currX_adder - currX_current - 1 must not be below zero).
Its purpose is to dim one channel e.g. CURR30 from e.g. 110% to 10% of curr30_current and at the same time dim another channel e.g. CURR31 from 20% to 120% of curr31_current.

Note:

1. The adder logic operates independent of the currX_mode setting, but its main purpose is to work together with the pwm modulator (improved up/down dimming)
2. If the adder logic is not used anymore, set the bit currX_adder to 0. (Setting adder_currentX to 0 is not sufficient)

Figure 24 – PWM Dimming Table

	Decrease by 1/4th every step		Decrease by 1/8th every step		Seconds	Seconds	Seconds	Seconds
Step	%Dimming	PWM	%Dimming	PWM	50msec/ Step	25msec/ Step	5msec/ Step	2,5msec/ Step
1	100,0	255	100,0	255	0,00s	0,00s	0,000s	0,000s
2	75,3	192	87,8	224	0,05s	0,03s	0,005s	0,003s
3	56,5	144	76,9	196	0,10s	0,05s	0,010s	0,005s
4	42,4	108	67,5	172	0,15s	0,08s	0,015s	0,008s
5	31,8	81	59,2	151	0,20s	0,10s	0,020s	0,010s

Figure 24 – PWM Dimming Table

	Decrease by 1/4th every step		Decrease by 1/8th every step		Seconds	Seconds	Seconds	Seconds
Step	%Dimming	PWM	%Dimming	PWM	50msec/ Step	25msec/ Step	5msec/ Step	2,5msec/ Step
6	23,9	61	52,2	133	0,25s	0,13s	0,025s	0,013s
7	18,0	46	45,9	117	0,30s	0,15s	0,030s	0,015s
8	13,7	35	40,4	103	0,35s	0,18s	0,035s	0,018s
9	10,6	27	35,7	91	0,40s	0,20s	0,040s	0,020s
10	8,2	21	31,4	80	0,45s	0,23s	0,045s	0,023s
11	6,3	16	27,5	70	0,50s	0,25s	0,050s	0,025s
12	4,7	12	24,3	62	0,55s	0,28s	0,055s	0,028s
13	3,5	9	21,6	55	0,60s	0,30s	0,060s	0,030s
14	2,7	7	19,2	49	0,65s	0,33s	0,065s	0,033s
15	2,4	6	16,9	43	0,70s	0,35s	0,070s	0,035s
16	2,0	5	14,9	38	0,75s	0,38s	0,075s	0,038s
17	1,6	4	13,3	34	0,80s	0,40s	0,080s	0,040s
18	1,2	3	11,8	30	0,85s	0,43s	0,085s	0,043s
19	0,8	2	10,6	27	0,90s	0,45s	0,090s	0,045s
20	0,4	1	9,4	24	0,95s	0,48s	0,095s	0,048s
21	**0,0**	**0**	8,2	21	**1,00s**	**0,50s**	**0,100s**	**0,050s**
22			7,5	19	1,05s	0,53s	0,105s	0,053s
23			6,7	17	1,10s	0,55s	0,110s	0,055s
24			5,9	15	1,15s	0,58s	0,115s	0,058s
25			5,5	14	1,20s	0,60s	0,120s	0,060s
26			5,1	13	1,25s	0,63s	0,125s	0,063s
27			4,7	12	1,30s	0,65s	0,130s	0,065s
28			4,3	11	1,35s	0,68s	0,135s	0,068s
29			3,9	10	1,40s	0,70s	0,140s	0,070s
30			3,5	9	1,45s	0,73s	0,145s	0,073s
31			3,1	8	1,50s	0,75s	0,150s	0,075s
32			2,7	7	1,55s	0,78s	0,155s	0,078s
33			2,4	6	1,60s	0,80s	0,160s	0,080s
34			2,0	5	1,65s	0,83s	0,165s	0,083s
35			1,6	4	1,70s	0,85s	0,170s	0,085s
36			1,2	3	1,75s	0,88s	0,175s	0,088s
37			0,8	2	1,80s	0,90s	0,180s	0,090s
38			0,4	1	1,85s	0,93s	0,185s	0,093s
39			**0,0**	**0**	**1,90s**	**0,95s**	**0,190s**	**0,095s**

7.3.4.2 PWM Generator Registers

Addr: 16h		**Pwm control**		
		This register controls PWM generator		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2:1	pwm_dim_mode	00b	R/W	Selects the dimming mode 00b = no dimming; actual content of register pwm_code is used for pwm generator 01b = logarithmic up dimming (codes are increased). Start value is actual pwm_code

Addr: 16h		Pwm control This register controls PWM generator		
Bit	**Bit Name**	**Default**	**Access**	**Description**
				10b = logarithmic down dimming (codes are decreased) Start value is actual pwm_code; switch off the dimmed current source after dimming is finished to avoid unnecessary quiescent current 11b = NA
5:3	pwm_dim_speed	000b	R/W	Defines dimming speed by increase/descrease pwm_code … 000b = … by 1/4th every 50 msec (total dim time 1.0s) 001b = … by 1/8th every 50 msec (total dim time 1.9s) 010b = … by 1/4th every 25 msec (total dim time 0.5s) 011b = … by 1/8th every 25 msec (total dim time 0.95s) 100b = … by 1/4th every 5 msec (total dim time 100ms) 101b = … by 1/8th every 5 msec (total dim time 190ms) 110b = … by 1/4th every 2.5 msec (total dim time 50ms) 111b = … by 1/8th every 2.5 msec (total dim time 95ms)

Addr: 17h		Pwm code This register controls the Pwm code.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	pwm_code	00b	R/W	Selects the PWM code 00h = Always 0 ... FFh = Always 1

Addr: 30h		Adder Current 1 This register defines the current which can be added to CURR1, CURR30		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	adder_current1	00b	R/W	Selects the added current value – do not exceed together with currX_current the internal 8 Bit range (see text) 00h = 0 (represents 0mA) ... FFh = 255 (represents 38.25mA)

Addr: 31h		Adder Current 2 This register defines the current which can be added to CURR2, CURR31		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	adder_current2	00b	R/W	Selects the added current value – do not exceed together with currX_current the internal 8 Bit range (see text) 00h = 0 (represents 0mA) ... FFh = 255 (represents 38.25mA)

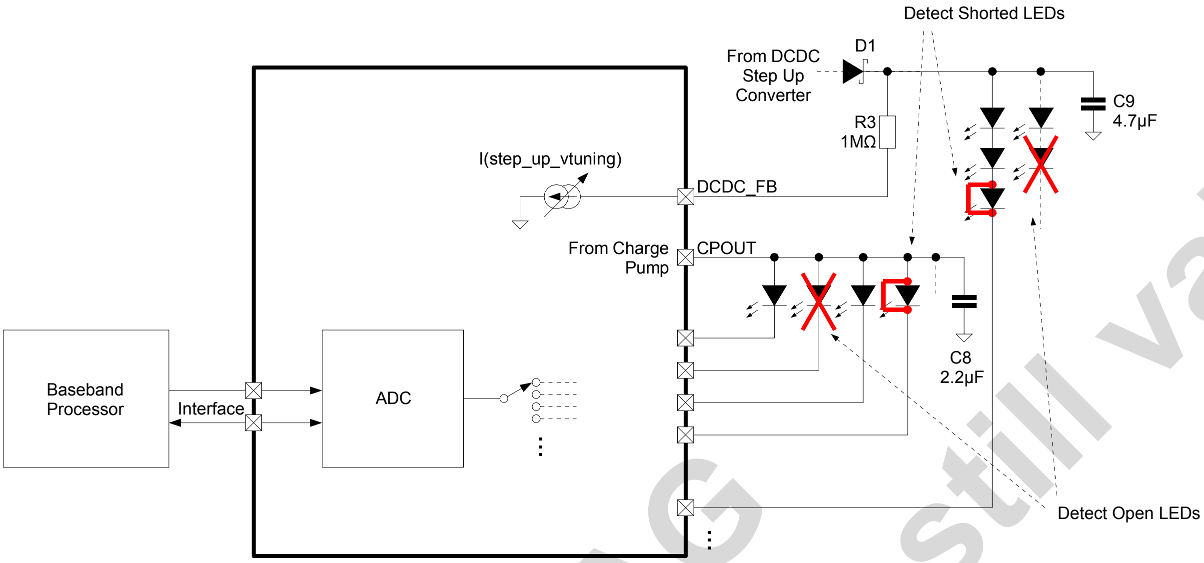
Addr: 32h		Adder Current 3 This register defines the current which can be added to CURR6, CURR32		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	adder_current3	00b	R/W	Selects the added current value – do not exceed together with currX_current the internal 8 Bit range (see text) 00h = 0 (represents 0mA) ... FFh = 255 (represents 38.25mA)

Addr: 34h		Adder Enable 2		
		Enables the adder circuit for the selected current sources		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	curr1_adder	0	R/W	Enables adder circuit for current source CURR1 0 = Normal Operation of the current source 1 = adder_current1 gets added to the current source current
1	curr2_adder	0	R/W	Enables adder circuit for current source CURR2 0 = Normal Operation of the current source 1 = adder_current2 gets added to the current source current
2	curr6_adder	0	R/W	Enables adder circuit for current source CURR6 0 = Normal Operation of the current source 1 = adder_current3 gets added to the current source current
3	curr30_adder	0	R/W	Enables adder circuit for current source CURR30 0 = Normal Operation of the current source 1 = adder_current1 gets added to the current source current
4	curr31_adder	0	R/W	Enables adder circuit for current source CURR31 0 = Normal Operation of the current source 1 = adder_current2 gets added to the current source current
5	curr32_adder	0	R/W	Enables adder circuit for current source CURR32 0 = Normal Operation of the current source 1 = adder_current3 gets added to the current source current

Addr: 35h		Subtract Enable		
		Enable the inversion from the signal from the pwm generator		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	sub_en1	0	R/W	Inverts the signal from the pwm generator 0 = Direct Operation (no inversion) 1 = The signal from the pwm generator for which the adder is enabled (curr1_adder = 1, curr30_adder = 1) is inverted
1	sub_en2	0	R/W	Inverts the signal from the pwm generator 0 = Direct Operation (no inversion) 1 = The signal from the pwm generator for which the adder is enabled (curr2_adder = 1, curr31_adder = 1) is inverted
2	sub_en3	0	R/W	Inverts the signal from the pwm generator 0 = Direct Operation (no inversion) 1 = The signal from the pwm generator for which the adder is enabled (curr6_adder = 1, curr32_adder = 1) is inverted

7.4 LED Test

Figure 25 – LED Function Testing



The AS3687/87XM supports the verification of the functionality of the connected LEDs (open and shorted LEDs can be detected). This feature is especially useful in production test to verify the correct assembly of the LEDs, all its connectors and cables. It can also be used in the field to verify if any of the LEDs is damaged. A damaged LED can then be disabled (to avoid unnecessary currents).
The current sources, charge pump, dcdc converter and the internal ADC are used to verify the forward voltage of the LEDs. If this forward voltage is within the specified limits of the LEDs, the external circuitry is assumed to operate.

7.4.1 Function Testing for single LEDs connected to the Charge Pump

For any current source connected to the charge pump (CURR30-33) where only one LED is connected between the charge pump and the current sink (see Figure 1) use:

Table 11 – Function Testing for LEDs connected to the Charge Pump

Step	Action	Example Code
1.	Switch on the charge pump and set it into manual 1:2 mode (to avoid automatic mode switching during measurements)	Reg 23h <- 14h (cp_mode = 1:2, manual) Reg 00h <- 04h (cp_on = 1)
2.	Switch on the current sink for the LED to be tested	e.g. for register CURR31set to 9mA use Reg 10h <- 0Fh (curr31_other = 9mA) Reg 03h <- 0ch (curr31_mode = curr31_other)
3.	Measure with the ADC the voltage on CP_OUT	Reg 26h <- 95h (adc_select=CP_OUT,start ADC) Fetch the ADC result from Reg 27h and 28h
4.	Measure with the ADC the voltage on the switched on current sink	Reg 26h <- 8bh (adc_select=CURR31,start ADC) Fetch the ADC result from Reg 27h and 28h
5.	Switch off the current sink for the LED to be tested	Reg 03h <- 00h (curr31_mode = off)
6.	Compare the difference between the ADC measurements (which is the actual voltage across the tested LED) against the specification limits of the tested LED	Calculation performed in baseband uProcessor
7.	Do the same procedure for the next LED starting from point 2	Jump to 2. If not all the LEDs have been tested
8.	Switch off the charge pump set chargepump automatic mode	Reg 00h <- 00h (cp_on = 0) Reg 23h <- 00h

7.4.2 Function Testing for LEDs connected to the Step Up DCDC Converter

For LEDs connected to the DCDC converter (usually current sinks CURR1,CURR2 and CURR6) use the following procedure:

Table 12 – Function Testing for LEDs connected to the DCDC converter

Step	Action	Example Code
1.	Switch on the current sink for the LED string to be tested (CURR1,2 or 6)	e.g. Test LEDs on CURR1: Reg 01h <- 01h (curr1_mode=on) Reg 09h <- 3ch (curr1 = 9mA)
2.	Select the feedback path for the LED string to be tested (e.g. step_up_fb = 01 for LED string on CURR1)	Reg 21h <- 02h (feedback=curr1)
3.	Set the current for step_up_vtuning exactly above the maximum forward voltage of the tested LED string + 0.6V (for the current sink) + 0.25V; add 6% margin (accuracy of step_up_vtuning); this sets the maximum output voltage limit for the DCDC converter	e.g. 4 LEDs with UfMAX = 4.1V gives 17.25V +6% = 18.29V; if R3=1MΩ and R4 = open, then select step_up_vtuning = 18 (Reg 21h <- 92h; results in 19.25V overvoltage protection voltage – see table in DCDC section)
4.	Set stepup_prot = 1	Reg 22h <- 04h
5.	Switch on the DCDC converter	Reg 00h <- 08h
6.	Wait 80ms (DCDC_FB settling time)	
7.	Measure the voltage on DCDC_FB (ADC)	Reg 26h <- 96h (adc_select=DCDC_FB, start ADC; Fetch the ADC result from Reg 27h and 28h)
8.	If the voltage on DCDC_FB is above 1.0V, the tested LED string is broken – then skip the following steps	(Code >199h)
9.	Switch off the overvoltage protection (stepup_prot = 0)	Reg 22h <- 00h
10.	Reduce step_up_vtuning step by step until the measured voltage on DCDC_FB (ADC) is above 1.0V. After changing step_up_vtuning always wait 80ms, before AD-conversion	e.g.: Reg 21h <- 62h (step_up_vtuning=12): ADC result=1,602V
11.	Measure voltage on DCDC_FB	e.g. DCDC_FB=1.602V
12.	Switch off the DCDC converter	Reg 00h <- 00h
13.	The voltage on the LED string can be calculated now as follows (R4 = open): $V_{LEDSTRING}$ = V(DCDC_FB) + I(step_up_vtuning) * R3 – 0.5V (current sinks feedback voltage: VFB2). V(DCDC_FB) = ADC Measurement from point 11 I(step_up_vtuing) = last setting used for point 10	e.g.: VLED = (1.602V + 12V – 0.5V) / 4 = 3.276V
14.	Compare the calculated value against the specification limits of the tested LEDs	

With the above described procedures electrically open and shorted LEDs can be automatically detected.

7.5 Analog-To-Digital Converter

The AS3687/87XM has a built-in 10-bit successive approximation analog-to-digital converter (ADC). It is internally supplied by V2_5, which is also the full-scale input range (0V defines the ADC zero-code). For input signal exceeding V2_5 (typ. 2.5V) a resistor divider with a gain of 0.4 ($Ratio_{prescaler}$) is used to scale the input of the ADC converter. Consequently the resolution is:

Table 13 – ADC Input Ranges, Compliances and Resolution

Channels (Pins)	Input Range	V_{LSB}	Note
DCDC_FB	0V-2.5V	2.44mV	V_{LSB}=2.5/1024
ADC_{TEMP_CODE}	-30°C to 125°C	1 / ADC_{TC}	junction temperature

Table 13 – ADC Input Ranges, Compliances and Resolution

Channels (Pins)	Input Range	V_{LSB}	Note
CURR30-33 VBAT, CP_OUT	0V-5.5V	6.1mV	V_{LSB}=2.5/1024 * 1/0.4; internal resistor divider used
CURR1, CURR2, CURR6	0V-1.0V	2.44mV	V_{LSB}=2.5/1024

Table 14 – ADC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
	Resolution	10			Bit	
Vin	Input Voltage Range	VSS		Vsupply	V	Vsupply = V2_5
DNL	Differential Non-Linearity		± 0.25		LSB	
INL	Integral Non-Linearity		± 0.5		LSB	
Vos	Input Offset Voltage		± 0.25		LSB	
Rin	Input Impedance	100			MΩ	
Cin	Input Capacitance			9	pF	
Vsupply (V2_5)	Power Supply Range		2.5		V	± 2%, internally trimmed.
Idd	Power Supply Current		500		µ A	During conversion only.
Idd	Power Down Current		100		nA	
T_{TOL}	Temperature Sensor Accuracy	-10		+10	°C	@ 25 °C
$ADC_{TOFFSET}$	ADC temperature measurement offset value		375		°C	
ADC_{TC}	Code temperature coefficient		1.2939		°C/Code	Temperature change per ADC LSB
$Ratio_{prescaler}$	Ratio of Prescaler		0.4			For all low voltage current sinks, CP_OUT and VBAT
Transient Parameters (2.5V, 25 °C)						
Tc	Conversion Time		27		µs	All signals are internally generated and triggered by start_conversion
fc	Clock Frequency		1.0		MHz	
ts	Settling Time of S&H		16		µs	

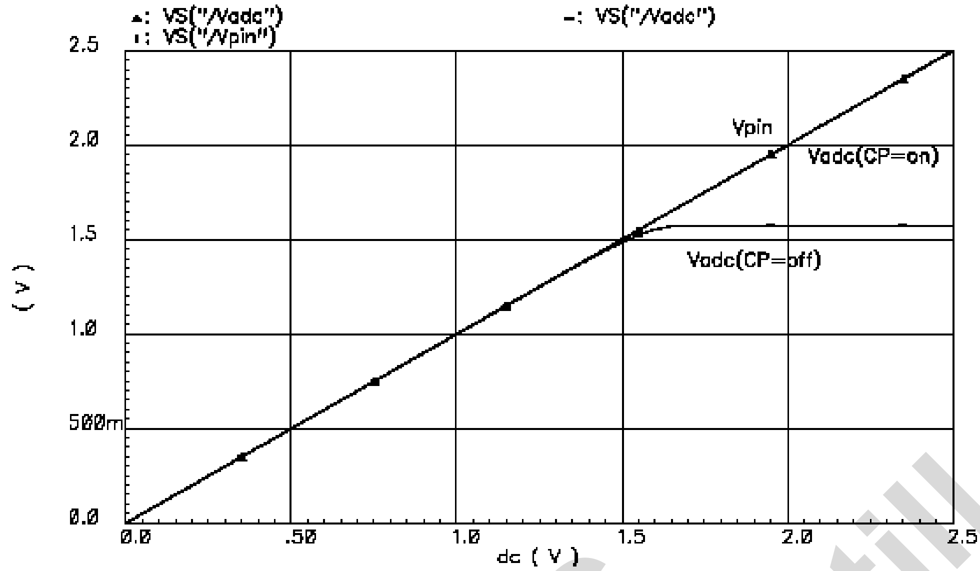
The junction temperature ($T_{JUNCTION}$) can be calculated with the following formula (ADC_{TEMP_CODE} is the adc conversion result for channel 17h selected by register adc_select = 010111b):

$$T_{JUNCTION}\ [°C] = ADC_{TOFFSET} - ADC_{TC} \cdot ADC_{TEMP\_CODE}$$

7.5.1 Application Hint: Extending to ADC input voltage range for CURR1,2,6

Under certain operating conditions, the input voltage range for the ADC input CURR1,2,6 (specified from 0.0V-1.0V for all operating conditions in table “ADC Input Ranges, Compliances and Resolution”) can be extended as follows:

Figure 26 –Internal voltage of the ADC vs. applied voltage on CURR1,2 or CURR6



Operating conditions: VBAT>=3.3V, TJUNC >= -20°C (one curve with charge pump operating in 1:2 mode 'on' and one curve with charge pump in 1:1 mode 'off').
Above curve represent the worst case and therefore are guaranteed by design under the above operating conditions (ADC input range for CURR1,2,6 is between 0V and 1.5V).

7.5.2 ADC Registers

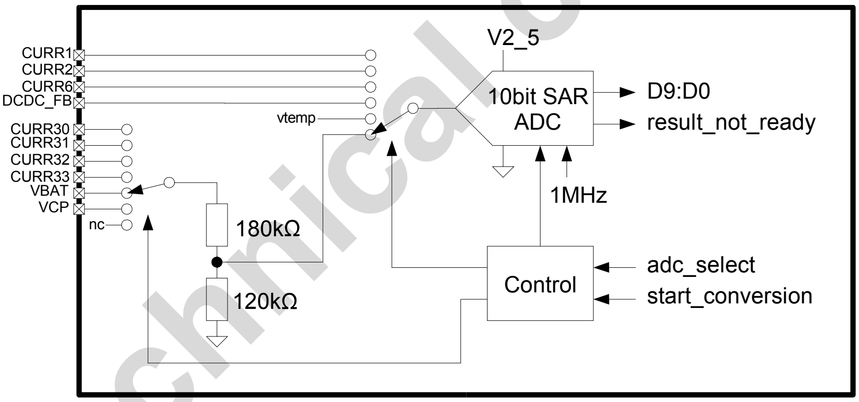
Addr: 27h		**ADC_MSB Result**		
		Together with Register 27h, this register contains the results (MSB) of an ADC cycle.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
6:0	D9:D3	N/A	R	ADC results register.
7	result_not_ready	N/A	R	Indicates end of ADC conversion cycle. 0 = Result is ready. 1 = Conversion is running.

Addr: 28h		**ADC_LSB Result**		
		Together with Register 28h, this register contains the results (LSB) of an ADC cycle		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2:0	D2:D0	N/A	R	ADC result register.

Addr: 26h		ADC_control		
		This register input source selection and initialization of ADC.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
5:0	adc_select[1]	0	R/W	Selects input source as ADC input. 000000 (00h) = reserved 000001 (01h) = reserved 000010 (02h) = reserved 000011 (03h) = reserved 000100 (04h) = reserved 000101 (05h) = reserved 000110 (06h) = reserved 000111 (07h) = reserved 001000 (08h) = CURR1 001001 (09h) = CURR2 001010 (0Ah) = CURR30 001011 (0Bh) = CURR31 001100 (0Ch) = CURR32 001101 (0Dh) = CURR33 001110 (0Eh) = reserved 001111 (0Fh) = reserved 010000 (10h) = reserved 010001 (11h) = reserved 010010 (12h) = reserved 010011 (13h) = CURR6 010100 (14h) = VBAT 010101 (15h) = CP_OUT 010110 (16h) = DCDC_FB 010111 (17h) = ADCTEMP_CODE (junction temperature) 011xxx, 1xxxxx = reserved
6				reserved – don't use; always write 0 to this register
7	start_conversion	N/A	W	Writing a 1 into this bit starts one ADC conversion cycle.

Notes:
1. See Table 'ADC Input Ranges, Compliances and Resolution' for ADC ranges and possible

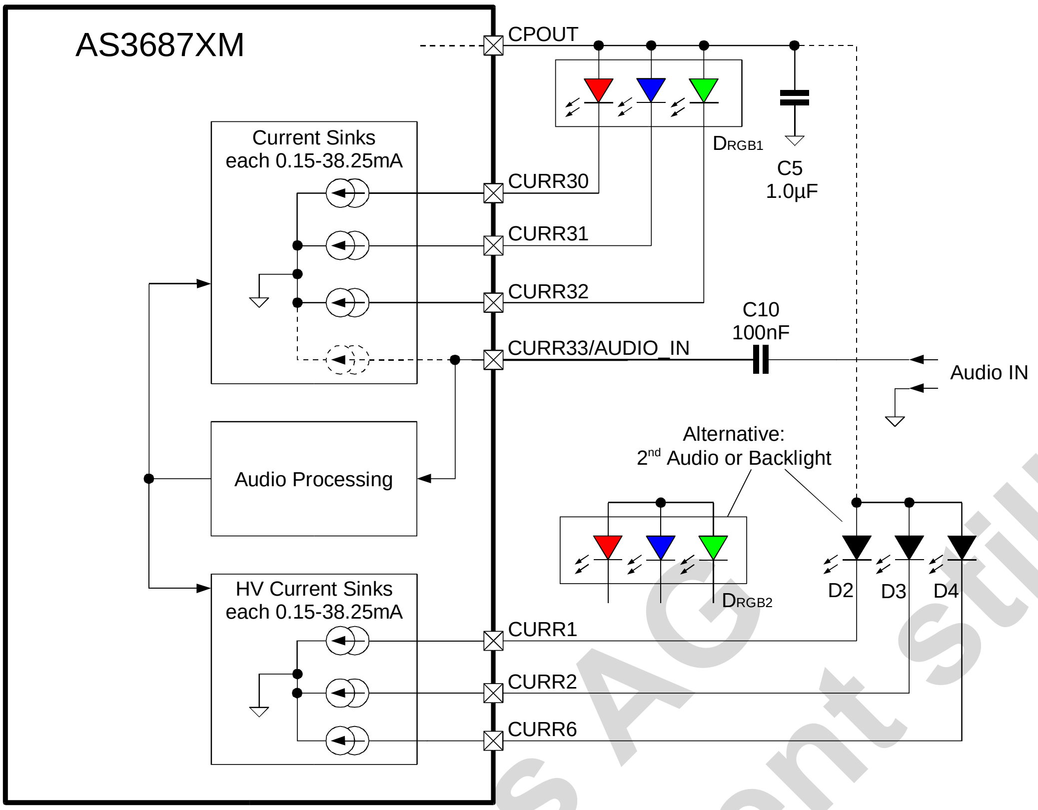
Figure 27 – ADC Circuit



7.6 Audio controlled RGB LEDs (only AS3687XM)

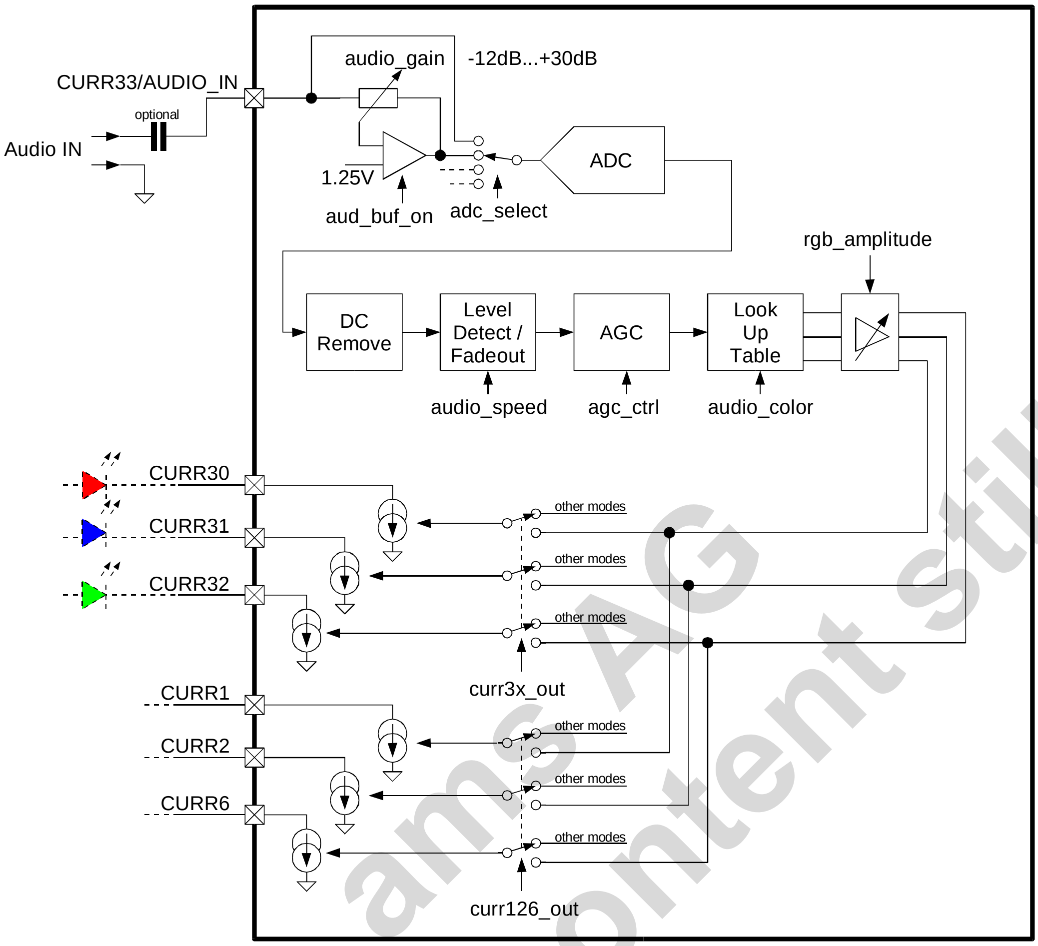
Up to 2 RGB LEDs (connected to the pins CURR30-CURR32 and/or CURR1,2,6) can be controlled by an audio source (connected to pin CURR33/AUDIO_IN). The color of the RGB LED(s) is depending on the input amplitude and it starts from black transitions to blue, green, cyan, yellow, red and for high amplitudes white is used (internal lookup table if audio_color=000b).

Figure 28 – Audio controlled RGB LED application circuit



The internal circuit has the following functions:

Figure 29 – Audio controlled RGB LED internal circuit



The audio controlled LED block is enabled if any of the registers curr3x_out or curr126_out is not zero.
The audio input amplifier (enabled by aud_buf_on=1) is used to allow the attenuation (or amplification of the input signal) and has the following parameters:

Table 15 – Audio input Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
Vin	Input Voltage Range	0		2.5	V	
Rin_min	min. Input Impedance		20		kΩ	at max. input gain (30dB)

When audio control RGB LED is active, the internal ADC is continuously running at a sample frequency of 45.5kHz. In this case the ADC cannot be used for any other purpose.
The input amplitude is mapped into different colors for RGB LED(s) or brightness for single color LED(s). The mapping is controlled by the register audio_color. If audio_color = 000, then the mapping is done as follows: Very low amplitudes are mapped to black, for higher amplitudes, the color smoothly transitions from blue, green, cyan, yellow, red and eventually to white (for high input amplitudes). Otherwise the output is mapped to the brightness of a single color.

7.6.1 AGC

The AGC is used to ‘compress’ the input signal and to attenuate very low input amplitude signals (this is performed to ensure no light output for low signals especially for noisy input signals).
The AGC monitors the input signal amplitude and filters this amplitude with a filter with a short attack time, but a long decay time (decay time depends on the register agc_ctrl). This amplitude measurement (represented by an

integer value from 0 to 15) is then used to amplify or attenuate the input signal with one of the following amplification ratios (output to input ratio) – the curve A, B, or C is selected depending on the register agc_ctrl:

Figure 30 – AGC curve A (x-axis: input amplitude, y-axis: output amplitude; actual value: gain between output to input)

15													1,3	1,2	1,1	1,0
14									1,8	1,6	1,4	1,3				
13					3,3	2,6	2,2	1,9								
12				4,0												
11				4,0												
10				4,0												
9				4,0												
8			4,0													
7			4,0													
6			4,0													
5			4,0													
4		4,0														
3		4,0														
2		4,0														
1		4,0														
0	0,0															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Figure 31 – AGC curve B (x-axis: input amplitude, y-axis: output amplitude; actual value: gain between output to input)

15																1,0
14													1,2	1,1	1,0	
13										1,4	1,3	1,2				
12							2,0	1,7	1,5							
11						2,2										
10					2,5											
9				3,0												
8				3,0												
7				3,0												
6			3,0													
5			3,0													
4			3,0													
3		3,0														
2		3,0														
1		3,0														
0	0,0															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Figure 32 – AGC curve C (x-axis: input amplitude, y-axis: output amplitude; actual value: gain between output to input)

15																1,0
14														1,1	1,0	
13												1,2	1,1			
12										1,3	1,2					
11								1,6	1,4							
10							1,7									
9						1,8										
8					2,0											
7					2,0											
6				2,0												
5				2,0												
4			2,0													
3			2,0													
2		2,0														
1		2,0														
0	0,0															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

7.6.2 Audio Control Registers

Addr: 46h		Audio Control (only AS3687XM) Audio Controlled LED Mode control		
Bit	Bit Name	Default	Access	Description
0	aud_buf_on	0b	R/W	Audio input buffer enable 0 off 1 on
4:2	audio_color	000b	R/W	audio controlled LED color selection 000 color scheme defined by lookup table 001-111 fixed color scheme (b2=R, b1=G, b0=B) – single color only (e.g. Red: 100b)
7:6	audio_speed	00b	R/W	Audio controlled LED persistence time 00 none 01 200ms 10 400ms 11 800ms

Addr: 47h		Audio Input (only AS3687XM) Audio controlled LED input control		
Bit	Bit Name	Default	Access	Description
2:0	audio_gain	000b	R/W	Audio input buffer gain control 000 -12dB 001 -6dB 010 0dB 011 +6dB 100 +12dB 101 +18dB 110 +24dB 111 +30dB
5:3	agc_ctrl	000b	R/W	Audio input buffer AGC function controls AGC transfer function 000 AGC off 001 attenuate low amplitude signals otherwise linear response (to remove e.g. noise) 010 AGC curve A; slow decay of amplitude detection 011 AGC curve A; fast decay of amplitude detection 100 AGC curve B; slow decay of amplitude detection 101 AGC curve B; fast decay of amplitude detection 110 AGC curve C; slow decay of amplitude detection 111 AGC curve C; fast decay of amplitude detection
6	audio_man_start	0b	R/W	Startup Control of audio input buffer (for charging of external AC-coupling capacitor) 0 automatic precharging 300us (if *audio_dis_start* = 0) 1 continuously precharging (if *audio_buf_on* = 1)
7	audio_dis_start	0b	R/W	Disable Startup Control of audio input buffer 0 precharging enabled 1 precharging disabled

Addr: 48h		Audio output (only AS3687XM) Audio controlled LED input control		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2:0	rgb_amplitude	000b	R/W	RGB output amplitude control (in % of selected output current) – master amplitude control 000 6.25% 001 12.5% 010 25% 011 50% 100 75% 101 87.5% 110 93.75% 111 100%
3	curr3x_out	0b	R/W	Audio sync enable for CURR30-CURR32 0 off 1 on, ADC continuously running with f=500kHz
4	curr126_out	0b	R/W	Audio sync enable for CURR1, CURR2, CURR6 0 off 1 on, ADC continuously running with f=500kHz

7.7 Power-On Reset

The internal reset is controlled by two sources:

- VBAT Supply
- Serial interface state (SCL, SDA)

The internal reset is forced if VBAT is low or if both interface pins (SCL, SDA) are low for more than 100ms. The device enters shutdown mode, when SCL and SDA remain low.

The reset levels control the state of all registers. As long as VBAT and SCL/SDA are below their reset thresholds, the register contents are set to default. Access by serial interface is possible once the reset thresholds are exceeded.

Figure 33 – Zero Power Device Wakeup block diagram

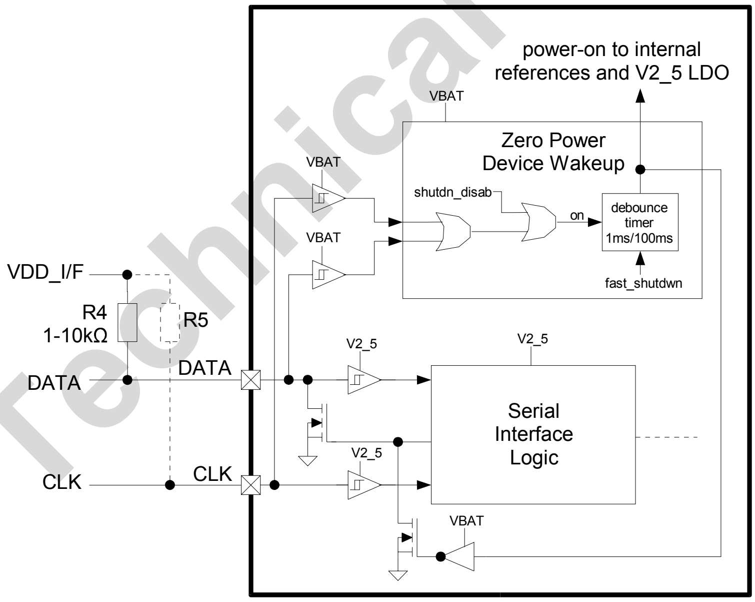


Table 16 – Reset Levels

Symbol	Parameter	Min	Typ	Max	Unit	Note
VPOR_VBAT	Overall Power-On Reset	1.8	2.15	2.4	V	Monitor voltage on V2_5; power-on reset for all internal functions.[2]
VPOR_PERI	Reset Level for pins SCL, SDA	0.29	1.0	1.38	V	Monitor voltage on pins SCL, SDA
tPOR_DEB	Reset debounce time for pins SCL, SDA	80	100	120	ms	
tSTART	Interface Startup Time	4	6	8	ms	

7.7.1 Reset control register

Addr: 29h		Overtemp Control This register reads and resets the overtemperature flag.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
4	shutdwn_enab	0	R/W	Enable Shutdown mode and serial interface reset. 0 Serial Interface reset disabled. Device does not enter Shutdown mode 1 Serial Interface reset enabled, device enters shutdown when SCL and SDA remain low for min. 120ms

7.8 Temperature Supervision

An integrated temperature sensor provides over-temperature protection for the AS3687/87XM. This sensor generates a flag if the device temperature reaches the overtemperature threshold of 140º. The threshold has a hysteresis to prevent oscillation effects.

If the device temperature exceeds the 140º threshold all current sources, the charge pump and the dcdc converter is disabled and the ov_temp flag is set. After decreasing the temperature by 5º (typically) operation is resumed.

The ov_temp flag can only be reset by first writing a 1 and then a 0 to the bit rst_ov_temp.

Bit ov_temp_on = 1 activates temperature supervision.

Table 17 – Overtemperature Detection

Symbol	Parameter	Min	Typ	Max	Unit	Note
T140	ov_temp Rising Threshold		140		° C	
Thyst	ov_temp Hystersis		5		° C	

[2] Guaranteed by design – not production tested.

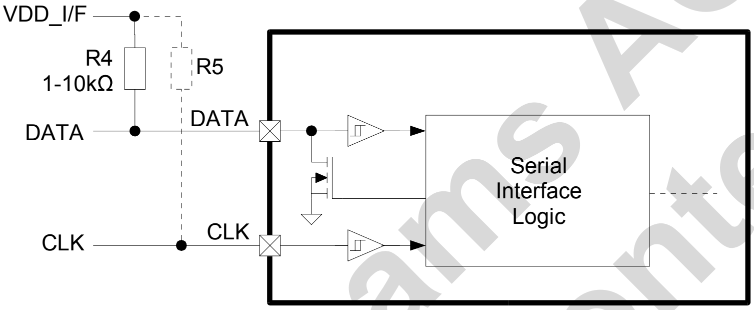
7.8.1 Temperature Supervision Registers

Addr: 29h		Overtemp Control		
		This register reads and resets the overtemperature flag.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	ov_temp_on	1	W	Activates/deactivates device temperature supervision. Default: Off - all other bits are only valid if this bit is set to 1. 0 = Temperature supervision is disabled. No reset will be generated if the device temperature exceeds 140ºC. 1 = Temperature supervision is enabled.
1	ov_temp	N/A	R	1 = Indicates that the overtemperature threshold has been reached; this flag is not cleared by an overtemperature reset. It has to be cleared using bit rst_ov_temp.
2	rst_ov_temp	0	R/W	The ov_temp flag is cleared by first setting this bit to 1, and then setting this bit to 0.

7.9 Serial Interface

The AS3687/87XM is controlled using serial interface pins CLK and DATA:

Figure 35 – Serial interface block diagram



The clock line CLK is never held low by the AS3687/87XM (as the AS3687/87XM does not use clock stretching of the bus).

Table 18 – Serial Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{IHI/F}$	High Level Input voltage	1.38		VBAT	V	Pins DATA and CLK
$V_{ILI/F}$	Low Level Input voltage	0.0		0.52	V	
$V_{HYSTI/F}$	Hysteresis		0.1		V	
t_{RISE}	Rise Time - $V_{ILI/F}$ to $V_{IHI/F}$	0		1000	ns	
t_{FALL}	Fall Time - $V_{IHI/F}$ to $V_{ILI/F}$	0		300	ns	
t_{CLK_FILTER}	Spike Filter on CLK		100		ns	
t_{DATA_FILTER}	Spike Filter on DATA		300		ns	

7.9.1 Serial Interface Features

- Fast Mode Capability (Maximum Clock Frequency is 400 kHz)
- 7-bit Addressing Mode
- Write Formats
  - Single-Byte Write
  - Page-Write

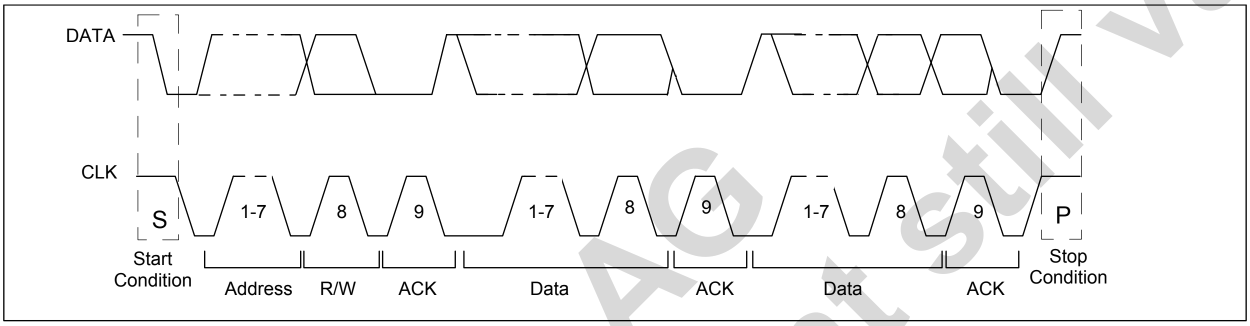
- Read Formats
  - Current-Address Read
  - Random-Read
  - Sequential-Read
- DATA Input Delay and CLK Spike Filtering by Integrated RC Components

7.9.2 Device Address Selection

The serial interface address of the AS3687/87XM has the following address:

- 80h – Write Commands
- 81h – Read Commands

Figure 36 – Complete Serial Data Transfer



7.9.2.1 Serial Data Transfer Formats

Definitions used in the serial data transfer format diagrams are listed in the following table:

Table 19 – Serial Data Transfer Byte Definitions

Symbol	Definition	R/W (AS3687/87XM Slave)	Notes
S	Start Condition after Stop	R	1 bit
Sr	Repeated Start	R	1 bit
DW	Device Address for Write	R	10000000b (80h).
DR	Device Address for Read	R	10000001b (81h)
WA	Word Address	R	8 bits
A	Acknowledge	W	1 bit
N	Not Acknowledge	R	1 bit
reg_data	Register Data/Write	R	8 bits
data (n)	Register Data/read	R	1 bit
P	Stop Condition	R	8 bits
WA++	Increment Word Address Internally	R	During Acknowledge

Figure 37 – Serial Interface Byte Write

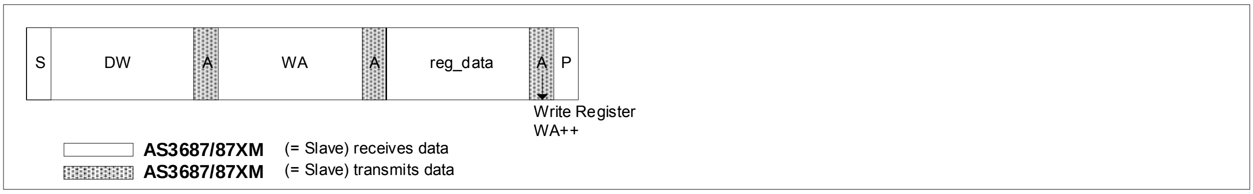
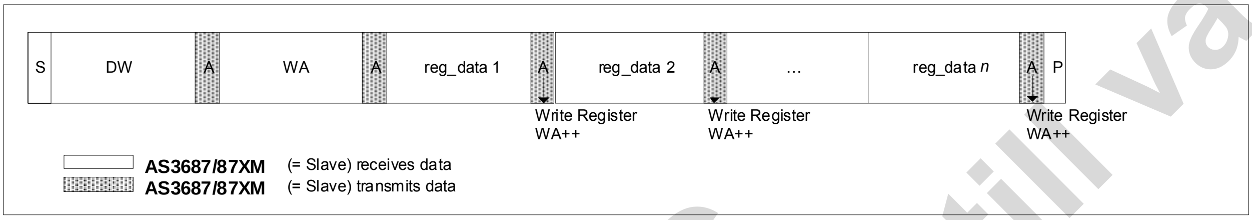


Figure 38 – Serial Interface Page Write



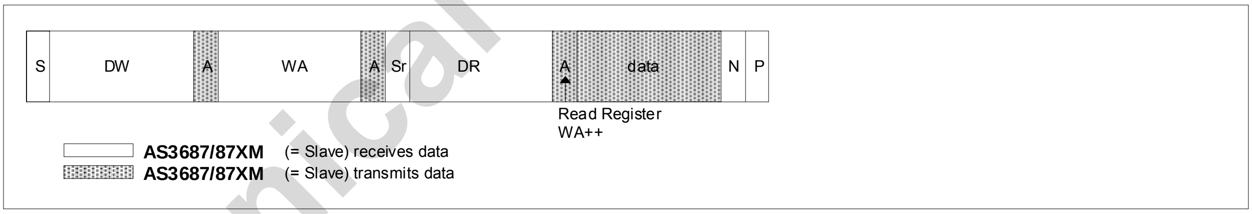
Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

The following diagrams show the serial read formats supported by the AS3687/87XM.

Figure 39 – Serial Interface Random Read

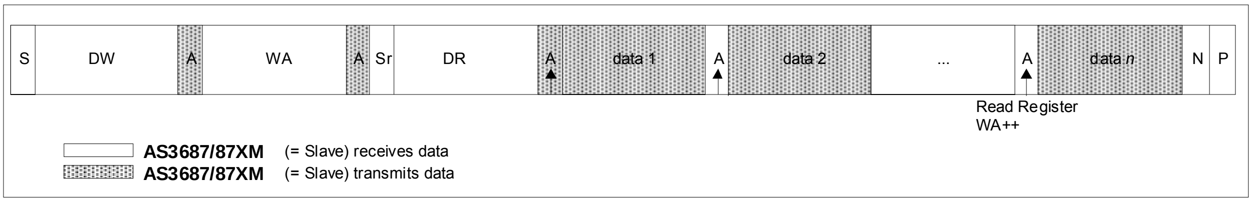


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st CLK pulse after the ACKNOWLEDGE bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a NOT ACKNOWLEDGE, and issues a STOP condition on the bus.

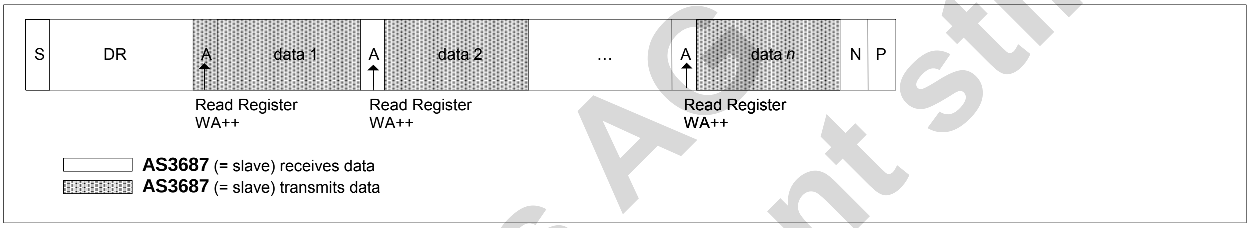
Figure 40 – Serial Interface Sequential Read



Sequential Read is the extended form of Random Read, as multiple register-data bytes are subsequently transferred.

In contrast to the Random Read, in a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a NOT ACKNOWLEDGE following the last data byte and subsequently generate the STOP condition.

Figure 41 – Serial Interface Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address.

Analogous to Random Read, a single byte transfer is terminated with a NOT ACKNOWLEDGE after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes must be responded to with an ACKNOWLEDGE from the master.

For termination of the transmission the master sends a NOT ACKNOWLEDGE following the last data byte and a subsequent STOP condition.

7.10 Operating Modes

If the voltage on SCL and SDA is less than 1V (for > t_{POR_DEB}), the AS3687/87XM is in shutdown mode and its current consumption is minimized (I_{BAT} = $I_{SHUTDOWN}$) and all internal registers are reset to their default values.

If the voltage at SCL or SDA rises above 1V, the AS3687/87XM serial interface is enabled and the AS3687/87XM and the standby mode is selected. The AS3687/87XM is switched automatically from standby mode (I(BAT) = $I_{STANDBY}$) into normal mode (I(BAT) = I_{ACTIVE}) and back, if one of the following blocks are activated:

- Charge pump
- Step up regulator
- Any current sink
- ADC conversion started
- PWM active
- Pattern mode active.

If any of these blocks are already switched on the internal oscillator is running and a write instruction to the registers is directly evaluated within 1 internal CLK Cycle (typ. 1µs)

If all these blocks are disabled, a write instruction to enable these blocks is delayed by 64 CLK cycles (oscillator will startup, within max 200µs).

8 Register Map

Table 20 – Registermap

Register Definition	Addr.	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Reg. control	00h	00					step_up_on	cp_on		
curr12 control	01h	00h					curr2_mode		curr1_mode	
curr rgb control	02h	00h	curr6_mode							
curr3 control1	03h	00h	curr33_mode		curr32_mode		curr31_mode		curr30_mode	
Curr1 current	09h	00h	curr1_current							
Curr2 current	0Ah	00h	curr2_current							
Curr3x strobe	0Eh	00h			curr3x_strobe					
Curr3x preview	0Fh	00h			curr3x_preview					
Curr3x other	10h	00h			curr3x_other					
Curr3 strobe control	11h	00h	strobe_timing				strobe_mode		strobe_ctrl	
Curr3 control2	12h	00h			curr3x_strobe_high			preview_ctrl		preview_off_after strobe
Pwm control	16h	00h		pwm_dim_speed				pwm_dim_mode		
pwm code	17h	00h	pwm_code							
Pattern control	18h	00h	curr33_pattern	curr32_pattern	curr31_pattern	curr30_pattern	softdim_pattern	pattern_delay		pattern_color
Pattern data0	19h	00h	pattern_data[7:0]							
Pattern data1	1Ah	00h	pattern_data[15:8]							
Pattern data2	1Bh	00h	pattern_data[23:16]							
Pattern data3	1Ch	00h	pattern_data[31:24]							
DCDC control1	21h	00h	step_up_vtuning					step_up_fb		step_up_frequ
DCDC control2	22h	04h	step_up_fb_auto	curr6_prot_on	curr2_prot_on	curr1_prot_on	step_up_lowcur	step_up_prot	skip_fast	step_up_res
CP control	23h	00h		cp_auto_on	cp_start_debounce	cp_mode_switching		cp_mode		cp_clk
CP mode Switch1	24h	00h					curr33_on_cp	curr32_on_cp	curr31_on_cp	curr30_on_cp
CP mode Switch2	25h	00h	curr6_on_cp						curr2_on_cp	curr1_on_cp
ADC_control	26h	00h	start_conversion	adc_on	adc_select					
ADC_MSB result	27h	NA	result_not_ready	D9	D8	D7	D6	D5	D4	D3
ADC_LSB result	28h	NA						D2	D1	D0

Table 20 – Registermap

Register Definition	Addr.	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Overtemp control	29h	01h				shutdwn_enab		rst_ov_temp	ov_temp	ov_temp_on
Curr low voltage status1	2Ah	NA	curr6_low_v				curr33_low_v	curr32_low_v	curr31_low_v	curr30_low_v
Curr low voltage status2	2Bh	NA							curr2_low_v	curr1_low_v
gpio current	2Ch	00h		pattern_slow		pattern_delay2				
curr6 current	2Fh	00h	curr6_current							
Adder Current 1	30h	00h	adder_current1 (can be enabled for CURR30, CURR1)							
Adder Current 2	31h	00h	adder_current2 (can be enabled for CURR31, CURR2)							
Adder Current 3	32h	00h	adder_current3 (can be enabled for CURR32, CURR6)							
Adder Enable 2	34h	00h			curr32_adder	curr31_adder	curr30_adder	curr6_adder	curr2_adder	curr1_adder
Subtract Enable	35h	00h						sub_en 3	sub_en 2	sub_en 1
ASIC ID1	3Eh	CAh	1	1	0	0	1	0	1	0
ASIC ID2	3Fh	50h	0	1	0	1	revision			
Curr30 current	40h	00h	curr30_current							
Curr31 current	41h	00h	curr31_current							
Curr32 current	42h	00h	curr32_current							
Curr33 current	43h	00h	curr33_current							
Audio Control (only AS3687XM)	46h	00h	audio_speed			audio_color				aud_buf_on
Audio input (only AS3687XM)	47h	00h	audio_dis_start	audio_man_start	agc_ctrl			audio_gain		
Audio output (only AS3687XM)	48h	00h				curr126_out	curr3x_out	rgb_amplitude		

Note: If writing to register, write 0 to unused bits
Note: Write to read only bits will be ignored
Note: yellow color = read only

9 External Components

Table 21 – External Components List

Part Number	Value min	Value typ	Value max	Tol (min)	Rating (max)	Notes	Package (min)
C1		1µF		+/-20%	6.3V	Ceramic, X5R (V2_5 output) (e.g. Taiyo Yuden JMK105BJ105KV-F)	0402
C2		1µF		+/-20%	6.3V	Ceramic, X5R (VBAT) (e.g. Taiyo Yuden JMK107BJ225MA-T)	0402
C3		500nF		+/-20%	6.3V	Ceramic, X5R (Charge Pump) (e.g. Taiyo Yuden JMK107BJ225MA-T)	0402
C4		500nF		+/-20%	6.3V	Ceramic, X5R (Charge Pump) (e.g. Taiyo Yuden JMK107BJ225MA-T)	0402
C5		1µF		+/-20%	6.3V	Ceramic, X5R (Charge Pump Output) (e.g. Taiyo Yuden JMK107BJ225MA-T)	0403
C6		1µF		+/-20%	6.3V	Ceramic, X5R (Step Up DCDC input) (e.g. Taiyo Yuden JMK107BJ225MA-T)	0402
C7		1.5nF		+/-20%	25V	Ceramic, X5R (Step Up DCDC Feedback, 150pF for overvoltage protection)	0402
C8		15nF		+/-20%	6.3V	Ceramic, X5R (Step Up DCDC Feedback, 1.5nF for overvoltage protection)	0402
C9		4.7µF		+/-20%	25V	Ceramic, X5R, X7R (Step Up DCDC output) (e.g. Taiyo Yuden TMK316BJ475KG)	1206 (0805)
C10		100nF		+/-20%	6.3V	Ceramic, X5R, X7R (Audio DC Block capacitor) – only for AS3687XM	0402
R1		100mΩ		+/-5%		Shunt Resistor	0603
R2		1MΩ		+/-1%		Step Up DC/DC Converter Voltage Feedback	0201
R3		100kΩ		+/-1%		Step Up DC/DC Converter Voltage Feedback - not required for overvoltage protection	0201
R4		1-10kΩ		+/-1%		I2C Bus DATA Pullup resistor – usually already inside I2C master	0201
R5						I2C Bus CLK Pullup resistor – usually already inside I2C master	0201
L1		10µH		+/-20%		Panasonic ELLSFG100MA or TDK VLF3012A or LQH3NPN100NJ0	
Q1 (+ D1)		FDFMA3N109				Integrated NMOS and Schottky diode	MicroFET 2x2mm
D2:D14		LED				As required by application	

10 Pinout and Packaging

10.1 Pin Description

Table 22 – Pinlist WL-CSP 4x5 balls

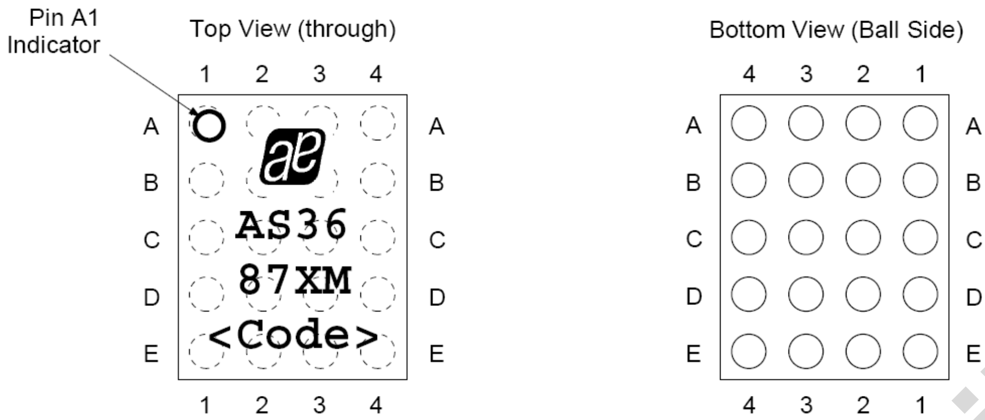
Bmp	Name	Type	Description
A1	C2_N	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 500nF to this pin.
A2	C1_P	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 500nF to this pin.
A3	CP_OUT	AO	Output voltage of the Charge Pump; connect a ceramic capacitor of 1µF (±20%).
A4	DATA	DIO	Serial interface data input/output.
B1	C1_N	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 500nF to this pin.
B2	C2_P	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 500nF to this pin.
B3	DCDC_GATE	AO	DCDC gate driver.
B4	CLK	DI	Clock input for serial interface.
C1	VSS	GND	Ground pad
C2	VBAT	S	Supply pad. Connect to battery.
C3	CURR30	AI	Analog current sink input, intended for activity icon LED
C4	DCDC_SNS	AI	Sense input of shunt resistor for Step Up DC/DC Converter.
D1	CURR33	AI	AS3687: Analog current sink input, intended for activity icon LED
	CURR33 /AUDIO_IN		AS3687XM: Analog current sink input, intended for activity icon LED or audio signal input
D2	CURR31	AI	Analog current sink input, intended for activity icon LED
D3	CURR2	AI_HV	Analog current sink input (intended for Keyboard backlight)
D4	DCDC_FB	AI	DCDC feedback. Connect to resistor string.
E1	CURR32	AI	Analog current sink input, intended for activity icon LED
E2	CURR6	AI_HV	Analog current sink input (intended for Keyboard backlight)
E3	CURR1	AI_HV	Analog current sink input (intended for Keyboard backlight)
E4	V2_5	AO3	Output voltage of the Low-Power LDO; always connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%). Do not load this pin during device startup.

Table 23 – Pin Type Definitions

Type	Description
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
AIO	Analog Pad
AI	Analog Input
AI_HV	High-Voltage (15V) Pin
AO3	Analog Output (3.3V)
S	Supply Pad
GND	Ground Pad

10.2 Package Drawings and Markings

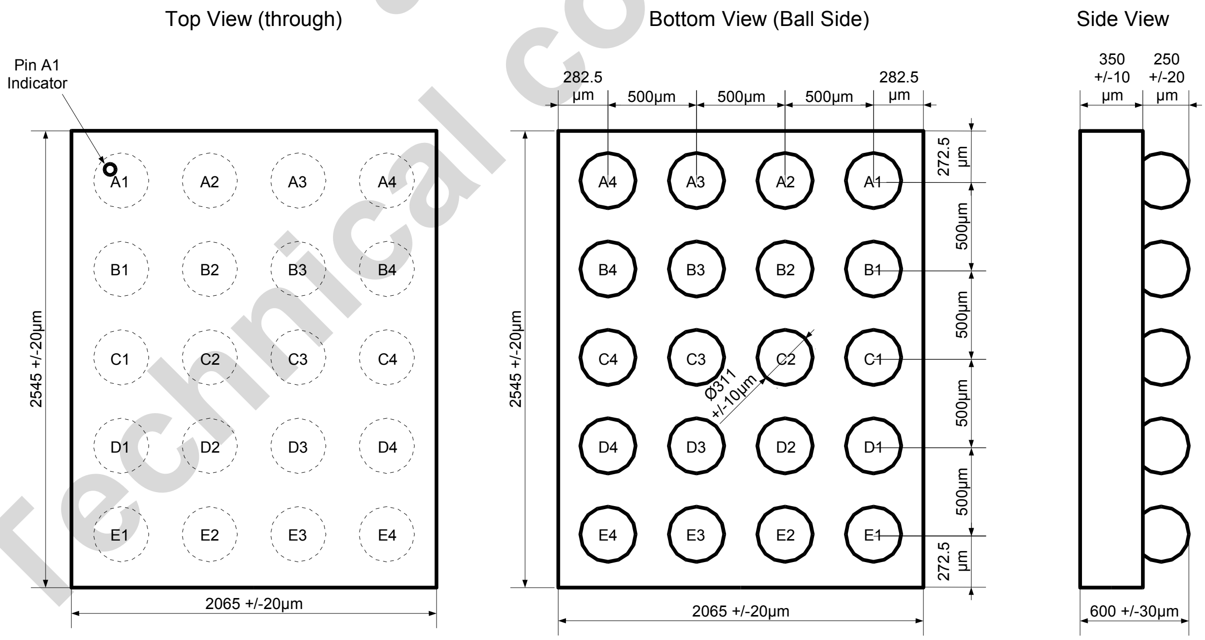
Figure 42 – WL-CSP 4x5 Balls Package Drawing



Marking:

Line 1: austriamicrosystems logo
Line 2: AS36
Line 3: 87 (for AS3687)
87XM (for AS3687XM)
Line 4: <Code>
4 Letter Encoded Datecode

Figure 43 – WL-CSP 4x5 Balls Detail Dimensions



The coplanarity of the balls is 40µm.

11 Ordering Information

Table 24 – Delivery Information

Part Number	Marking	Package Type	Delivery Form	Description
AS3687-ZWLT[1]	AS3687	WL-CSP 4x5 balls	Tape&Reel	AS3687 Wafer Level Chip Scale Package, Size 4x5 balls, 0.5mm pitch, RoHS compliant, Pb-Free
AS3687XM-ZWLT	AS3687XM	WL-CSP 4x5 balls	Tape&Reel	AS3687XM Wafer Level Chip Scale Package, Size 4x5 balls, 0.5mm pitch, RoHS compliant, Pb-Free

[1] **Do not use AS3687 for new designs – use AS3687XM (drop in pin to pin compatible replacement for AS3687) instead.**

Description:

AS3687-ZWLT

AS3687 AS3687XM		AS3687 Lighting Management Unit AS3687XM Lighting Management Unit (including audio controlled light)
-		
Z	…	Temperature range: Z = -30°C – 85°C
WL	…	Package: WL = Wafer Level Chip Scale Package
T	…	Delivery Form: T = Tape&Reel

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