SPP1305

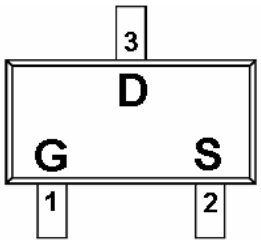
The SPP1305 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

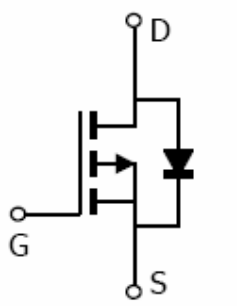
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

FEATURES

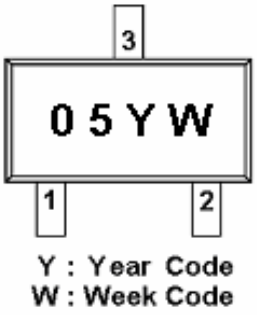
- -20V/-0.95A,$R_{DS(ON)}$= 280mΩ@V_{GS}=-4.5V
- -20V/-0.80A,$R_{DS(ON)}$= 380mΩ@V_{GS}=-2.5V
- -20V/-0.70A,$R_{DS(ON)}$= 530mΩ@V_{GS}=-1.8V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- SOT-323 (SC–70) package design

PIN CONFIGURATION (SOT-323 ; SC-70)





PART MARKING



SPP1305

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP1305S32RG	SOT-323	05YW

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
※ SPP1305S32RG : Tape Reel ; Pb – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate –Source Voltage		V_{GSS}	±12	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	-1.0	A
	T_A=70℃		-0.7	
Pulsed Drain Current		I_{DM}	-3	A
Continuous Source Current(Diode Conduction)		I_S	-0.28	A
Power Dissipation	T_A=25℃	P_D	0.33	W
	T_A=70℃		0.21	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	105	℃/W

SPP1305

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-0.5		-1.2	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V			-1	uA
		V_{DS}=-20V,V_{GS}=0V T_J=55℃			-5	
On-State Drain Current	$I_{D(on)}$	V_{DS}≦-5V,V_{GS}=-4.5V	-6			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-4.5V,I_D=-0.95A		0.22	0.28	Ω
		V_{GS}=-2.5V,I_D=-0.80A		0.30	0.38	
		V_{GS}=-1.8V,I_D=-0.70A		0.42	0.53	
Forward Transconductance	gfs	V_{DS}=-5V,I_D=-1.0A		3.5		S
Diode Forward Voltage	V_{SD}	I_S=-0.5A,V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-4V,V_{GS}=-4.5V I_D≡-1.0A		3.0	4.2	nC
Gate-Source Charge	Q_{gs}			0.6		
Gate-Drain Charge	Q_{gd}			0.5		
Input Capacitance	C_{iss}	V_{DS}=-4V,V_{GS}=0V f=1MHz		320		pF
Output Capacitance	C_{oss}			55		
Reverse Transfer Capacitance	C_{rss}			25		
Turn-On Time	$t_{d(on)}$	V_{DD}=-4V,R_L=4Ω I_D≡-1.0A,V_{GEN}=-4.5V R_G=6Ω		10	16	ns
	t_r			40	60	
Turn-Off Time	$t_{d(off)}$			18	25	
	t_f			15	20	