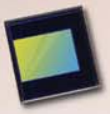
OmniVision



datasheet

PRODUCT SPECIFICATION

1/3.2" color CMOS 8 megapixel (3264 x 2448) image sensor
with OmniBSI+™ technology

OV8825

color CMOS 8 megapixel (3264 x 2448) image sensor with OmniBSI+™ technology

datasheet (COB)
PRODUCT SPECIFICATION

version 2.0
may 2012

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular phones
- digital still cameras (DSC)
- digital video camcorders (DVC)

ordering information

- **OV08825-G04A** (color, chip probing, 200 µm backgrinding, reconstructed wafer)**OV08825-E68A** (color, lead-free)
  68-pin CSP4

features

- automatic black level calibration (ABLC)
- programmable controls for frame rate, mirror and flip, cropping, windowing, and scaling
- image quality controls: lens correction and defective pixel canceling
- support for output formats: 10-bit RAW RGB (MIPI)
- support for horizontal and vertical subsampling
- support for images sizes: 8 Mpixel, EIS1080p, 1080p, EIS720p, EISQ 1080p, Q1080p, EISVGA, VGA, QVGA, etc.
- support 2x2 binning
- standard serial SCCB interface
- MIPI serial output interface
- 256 bytes embedded one-time programmable (OTP) memory for part identification, etc.
- on-chip phase lock loop (PLL)
- programmable I/O drive capability
- built-in 1.5V regulator for core

key specifications (typical)

- **active array size:** 3296 x 2460
- **power supply:**
  core: 1.5VDC ± 5% (internal regulator optional)
  analog: 2.6 ~ 3.0V
  I/O: 1.7 ~ 3.0V
- **power requirements:**
  active: 160mA (358 mW)
  standby: 30µA
- **temperature range:**
  operating: -30°C to 70°C junction temperature (see **table 8-2**)
  stable image: 0°C to 50°C junction temperature (see **table 8-2**)
- **output formats:** 10-bit RGB RAW
- **lens size:** 1/3.2"
- **lens chief ray angle:** 27° non-linear
- **input clock frequency:** 6~27 MHz
- **max S/N ratio:** 35.7 dB
- **dynamic range:** 70.45 dB @ 8x gain
- **maximum image transfer rate:**
  8Mpixel: 24 fps (see **table 2-1**)
  EIS1080p: 30 fps (see **table 2-1**)
  EIS720p: 60 fps (see **table 2-1**)
- **sensitivity:** 725 mV/Lux-sec
- **scan mode:** progressive
- **maximum exposure interval:** 2480 x t_{ROW}
- **pixel size:** 1.4 µm x 1.4 µm
- **dark current:** 8 mV/s @ 50°C junction temperature
- **image area:** 4614 µm x 3444 µm
- **packagedie dimensions:** 6350 µm x 6750 µm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pad numbers for the OV8825 image sensor. The die information is shown in section 9.

table 1-1 signal descriptions (sheet 1 of 3)

pad number	signal name	pad type	description	default I/O status
01	SIOD	I/O	SCCB data	
02	VSYNC	I/O	VSYNC output	
03	FREX	I/O	frame exposure input / mechanical shutter output	
04	SHUTTER	I/O	illumination control output	
05	AVDD	power	power for analog circuit	
06	AGND	ground	ground for analog circuit	
07	STROBE	I/O	strobe output	
08	RESETB	input	reset (active low with internal pull up transistors) Depending on process condition and DOVDD voltage, the pull up resistance ranges from 1MΩ ~ 7MΩ when it is low and ranges from 200KΩ to 1MΩ when it is high	
09	PWDNB	input	power down (active low with internal pull up resistor) Depending on process condition, the pull up resistance is 700KΩ ~ 1.3MΩ	
10	TM	input	test mode (active high with internal pull down resistor) Tie to ground although it is pulled to ground internally	
11	SGND	ground	ground for array	
12	DVDD	power	power for digital circuit	
13	DGND	ground	ground for digital circuit	
14	AVDD	power	power for analog circuit	
15	AGND	ground	ground for analog circuit	
16	AGND	ground	ground for analog circuit	
17	AVDD	power	power for analog circuit	
18	DGND	ground	ground for digital circuit	
19	DVDD	power	power for digital circuit	
20	EGND	ground	ground for MIPI TX circuit	
21	PVDD	power	power for PLL circuit	
22	XVCLK	input	system input clock	

table 1-1 signal descriptions (sheet 2 of 3)

pad number	signal name	pad type	description	default I/O status
23	DOVDD	power	power for I/O circuit	
24	MDP2	I/O	MIPI TX third data lane positive output	
25	MDN2	I/O	MIPI TX third data lane negative output	
26	MDP0	I/O	MIPI TX first data lane positive output	
27	MDN0	I/O	MIPI TX first data lane negative output	
28	MCP	I/O	MIPI TX clock lane positive output	
29	MCN	I/O	MIPI TX clock lane negative output	
30	EGND	ground	ground for MIPI TX circuit	
31	EVDD	power	power for MIPI TX circuit	
32	MDP1	I/O	MIPI TX second data lane positive output	
33	MDN1	I/O	MIPI TX second data lane negative output	
34	MDP3	I/O	MIPI TX fourth data lane positive output	
35	MDN3	I/O	MIPI TX fourth data lane negative output	
36	DVDD	power	power for digital circuit	
37	DGND	ground	ground for digital circuit	
38	AVDD	power	power for analog circuit	
39	AGND	ground	ground for analog circuit	
40	VSNK	analog I/O	VCM driver current sink input	
41	VSNK	analog I/O	VCM driver current sink input	
42	VGND	ground	ground for VCM driver	
43	VGND	ground	ground for VCM driver	
44	DVDD	power	power for digital circuit	
45	DGND	ground	ground for digital circuit	
46	DGND	ground	ground for digital circuit	
47	DVDD	power	power for digital circuit	
48	DOVDD	power	power for I/O circuit	
49	DVDD	power	power for digital circuit	
50	DOVDD	power	power for I/O circuit	
51	DVDD	power	power for digital circuit	
52	DOVDD	power	power for I/O circuit	

table 1-1 signal descriptions (sheet 3 of 3)

pad number	signal name	pad type	description	default I/O status
53	AGND	ground	ground for analog circuit	
54	AVDD	power	power for analog circuit	
55	DOGND	ground	ground for I/O circuit	
56	VH	reference	internal analog reference	
57	VNH	reference	internal analog reference	
58	VNL	reference	internal analog reference	
59	AGND	ground	ground for analog circuit	
60	**SIOC**	input	SCCB input clock	

table 1-2 configuration under various conditions (sheet 1 of 2)

pad	signal name	RESET	after RESET release	software standby	hardware standby (PWDNB = 0)
01	SIOD	open drain	I/O	I/O	open drain
02	VSYNC	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
03	FREX	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
04	SHUTTER	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
07	STROBE	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
08	RESETB	input	input	input	input
09	PWDNB	input	input	input	input
10	TM	input	input	input	input
22	XVCLK	input	input	input	high-z
24	MDP2	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
25	MDN2	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
26	MDP0	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)

table 1-2 configuration under various conditions (sheet 2 of 2)

pad	signal name	RESET	after RESET release	software standby	hardware standby (PWDNB = 0)
27	MDN0	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
28	MCP	zero	zero	zero by default (configurable)	zero by default (configurable)
29	MCN	zero	zero	zero by default (configurable)	zero by default (configurable)
32	MDP1	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
33	MDN1	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
34	MDP3	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
35	MDN3	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
40	VSNK	high-z	open drain	open drain	high-z
41	VSNK	high-z	open drain	open drain	high-z
60	SIOC	input	input	input	high-z

figure 1-1 pad diagram

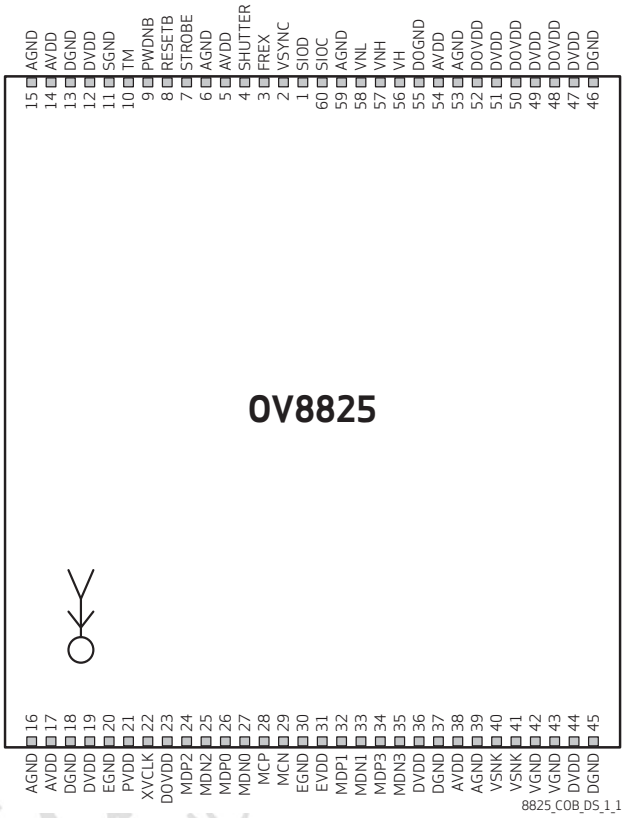


table 1-3 pad symbol and equivalent circuit (sheet 1 of 2)

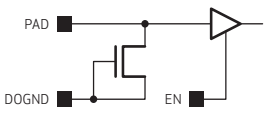
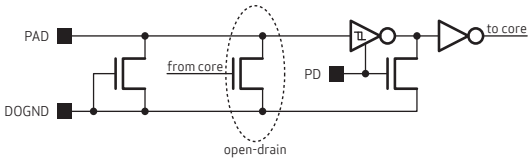
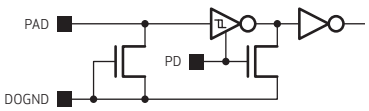
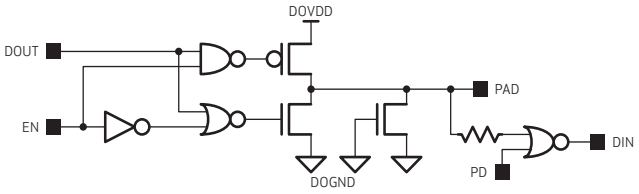
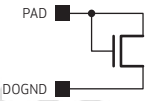
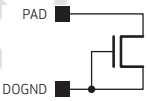
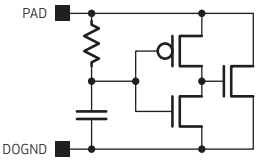
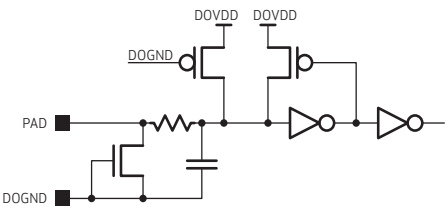
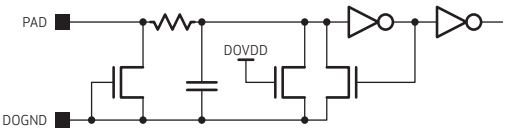
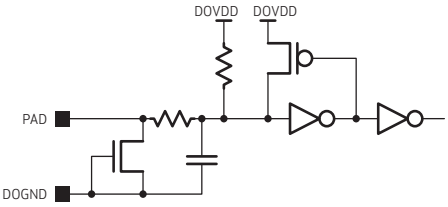
symbol	equivalent circuit
XVCLK	
SIOD	
SIOC	

table 1-3 pad symbol and equivalent circuit (sheet 2 of 2)

symbol	equivalent circuit
VSYNC, STROBE, SHUTTER, FREX	
VNH, VNL, VH	
MDP3, MDP2, MDP1, MDP0, MDN3, MDN2, MDN1, MDN0, MCP, MCN, VSNK, VGND, SGND, EGND, AGND, DOGND, DGND	
AVDD, EVDD, DVDD, DOVDD, PVDD	
RESETB	
TM	
PWDNB	

2 system level description

2.1 overview

The OV8825 color image sensor is a low voltage, high performance 1/3.2-inch 8 megapixel CMOS image sensor that provides the functionality of a single 8 megapixel (3264x2448) camera using OmniBSI+™ technology. It provides full-frame, sub-sampled, windowed 10-bit MIPI images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV8825 has an image array capable of operating at up to 24 frames per second (fps) in 10-bit 8 megapixel resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, white balance, defective pixel canceling, etc., are programmable through the SCCB interface.

In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

For customized information purposes, the OV8825 includes a one-time programmable (OTP) memory. The OV8825 has up to four lanes of MIPI interface.

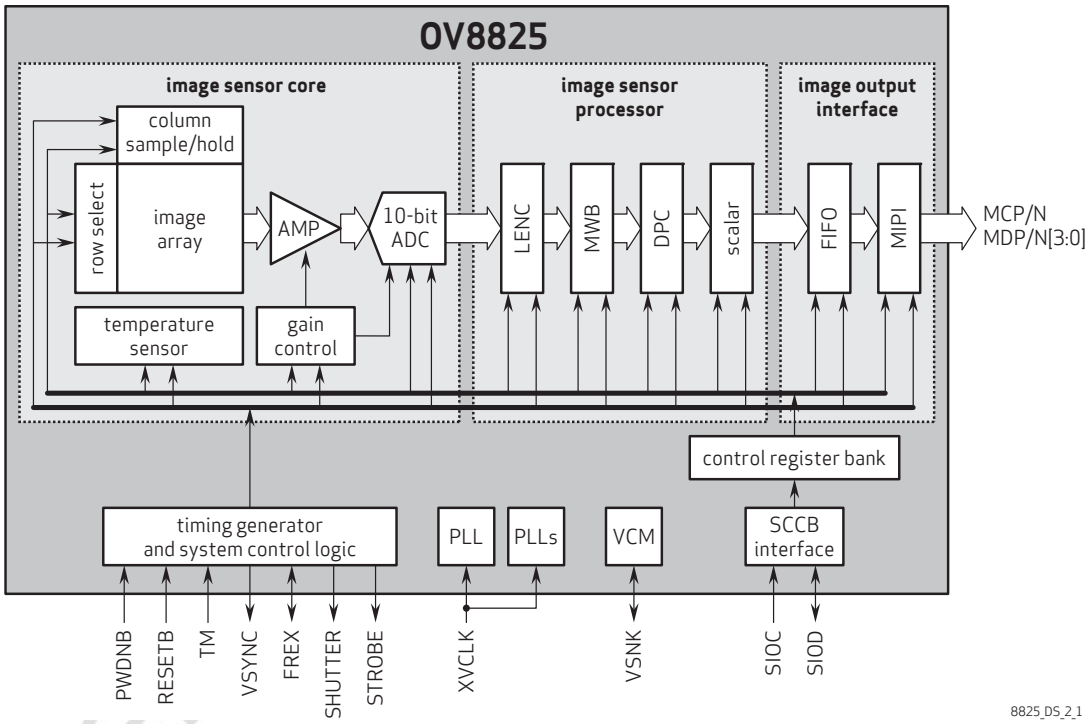
2.2 architecture

The OV8825 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OV8825 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, precharging and sampling the rows of array sequentially. In the time between precharging and sampling a row, the charge in the pixels decrease with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV8825 block diagram



2.3 format and frame

The OV8825 supports RAW RGB output with a one, two, or four lane MIPI interface.

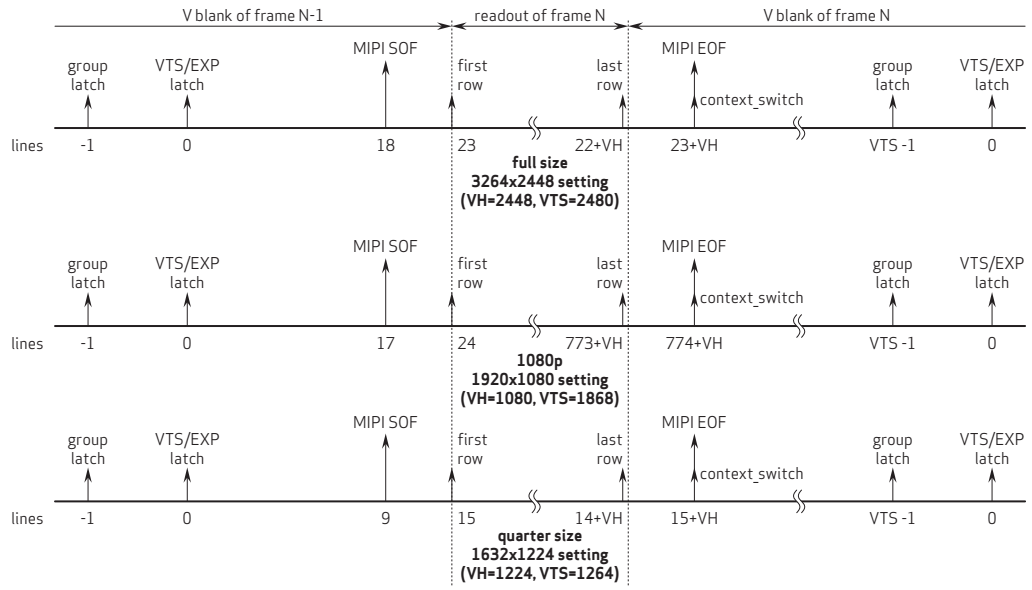
table 2-1 MIPI supported frame and frame rate (using 4 lanes, 700 Mbps max data rate)

format	resolution	maximum frame rate with MIPI	methodology
full resolution (see **figure 2-2** and **table 2-4**)	3264x2448	24 fps	full
EIS1080p (see **figure 2-3** and **table 2-4**)	2112x1188	30 fps	crop+scale 1.5 (3168x1782)
1080p (see **figure 2-2** and **table 2-4**)	1920x1080	30 fps	crop+scale 1.7 (3264x1836)
quartersize (see **figure 2-2** and **table 2-4**)	1632x1224	30 fps	binning+scale (3264x2448)
EIS720p (see **figure 2-3** and **table 2-4**)	1408x792	30 fps / 60 fps	crop+binningx2+scale 2.3 (3138x1822) HB2/VB2
720p (see **figure 2-3** and **table 2-4**)	1280x720	30 fps / 60 fps	crop+binningx2+scale 2.5 (3200x1800) HB2/VB2
EISQ1080p	1056x594	30 fps / 60 fps	crop+binningx2+scale 3.0 (3168x1782) HB2/VB2
Q1080p	960x540	30 fps / 60 fps	crop+binningx2+scale 3.4 (3264x1836) HB2/VB2
EISVGA	704x528	90 fps / 120 fps	crop+skip+scale
VGA (see **figure 2-4** and **table 2-4**)	640x480	90 fps / 120 fps	crop+skip+scale
QVGA	320x240	200 fps	crop+skip

table 2-2 MIPI supported format and frame rate (using 2 lanes, 800 Mbps max data rate)

resolution	frame rate	description
4:3 full resolution (8 megapixel)	15 fps	full frame
16:9 full resolution (cropped)	30 fps	crop (3264x1838)
16:9 1080p using scalar	30 fps	crop+scale (3264x1836)
16:9 720p using scalar	30 fps	crop+scale (3200x1800)

figure 2-2 exposure/gain latch points for full resolution, 1080p, and quarter size

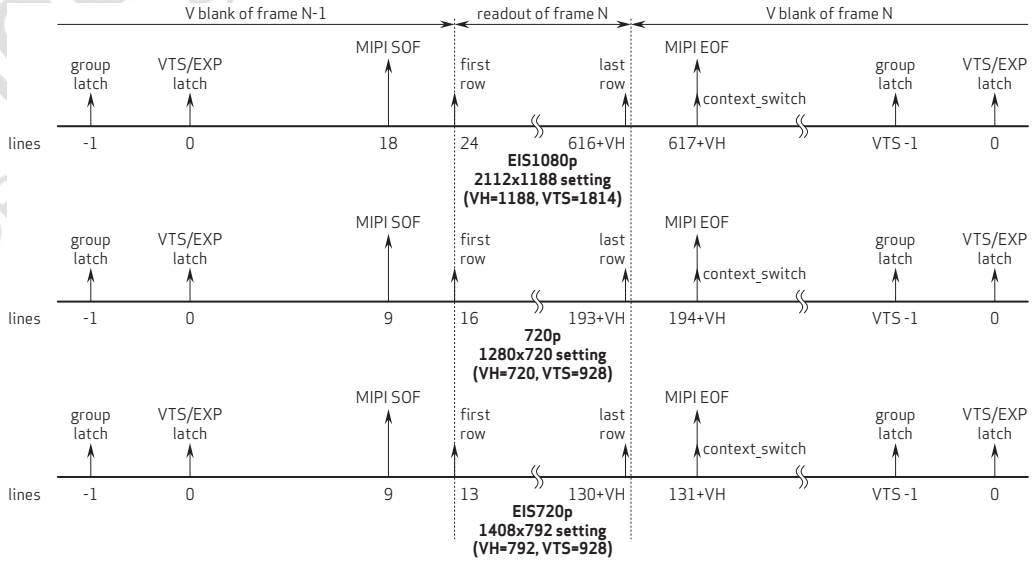


note 1 VTS = total vertical size in units of lines (refer to registers 0x380E, 0x380F)

note 2 VH = vertical endpoint (refer to registers 0x3806, 0x3807)

8825_DS_2_2

figure 2-3 exposure/gain latch points for EIS1080p, EIS720p, and 720p



note 1 VTS = total vertical size in units of lines (refer to registers 0x380E, 0x380F)

note 2 VH = vertical endpoint (refer to registers 0x3806, 0x3807)

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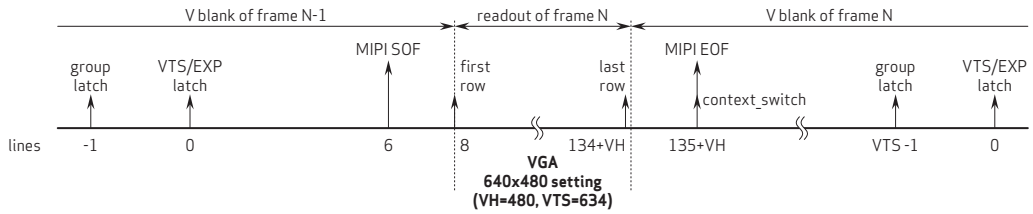
figure 2-4 exposure/gain latch points for VGA



note 1 VTS = total vertical size in units of lines (refer to registers 0x380E, 0x380F)

note 2 VH = vertical endpoint (refer to registers 0x3806, 0x3807)

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2.4 I/O control

table 2-3 I/O control registers (sheet 1 of 2)

function	register	description
output drive capability control	0x3612	Bit[6:5]: pad I/O drive capability 00: 1x 01: 2x 10: 3x 11: 4x
VSYNC I/O control	0x3000	Bit[1]: input/output control for VSYNC pad 0: input 1: output
VSYNC output select	0x3010	Bit[1]: output selection for VSYNC pad 0: normal data path (vertical sync signal) 1: register control value
VSYNC output value	0x300D	Bit[1]: output value
SHUTTER I/O control	0x3000	Bit[0]: input/output control for SHUTTER pad 0: input 1: output
SHUTTER output select	0x3010	Bit[0]: output selection for SHUTTER pad 0: normal data path (illumination control signal) 1: register control value
SHUTTER output value	0x300D	Bit[0]: output value
FREX I/O control	0x3000	Bit[2]: input/output control for FREX pad 0: input 1: output
FREX output select	0x3010	Bit[2]: output selection for FREX pad 0: normal data path 1: register control value

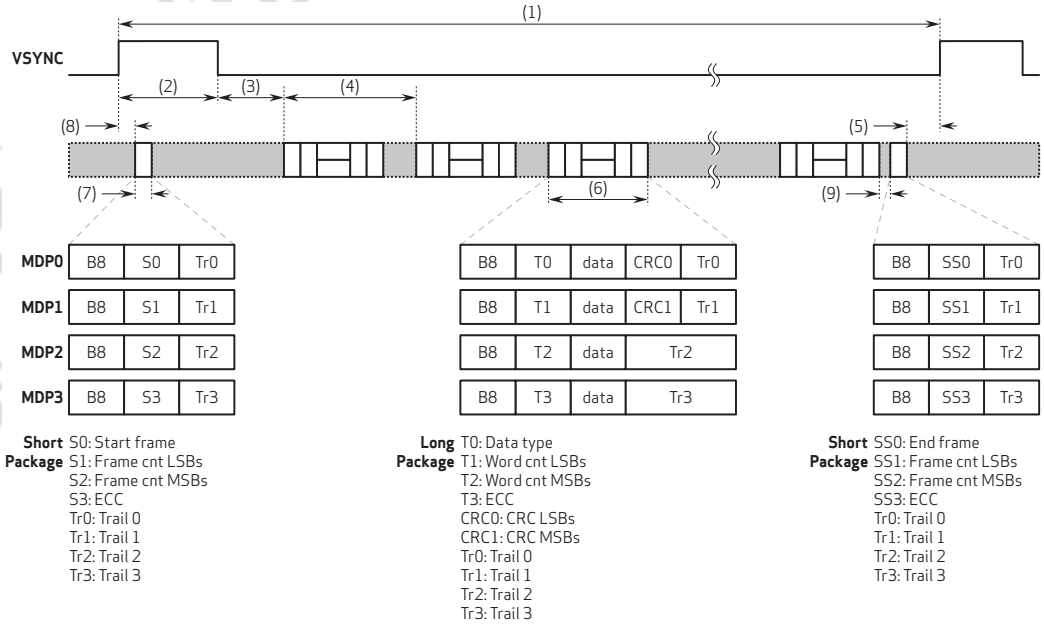
table 2-3 I/O control registers (sheet 2 of 2)

function	register	description
FREX output value	0x300D	Bit[2]: output value
STROBE I/O control	0x3000	Bit[4]: output selection for STROBE pad 0: normal data path 1: register control value
STROBE output select	0x3010	Bit[4]: input/output control for STROBE pad 0: input 1: output
STROBE output value	0x300D	Bit[4]: output value

2.5 MIPI interface

The OV8825 supports one, two, and four lane MIPI transmitter interfaces with up to 800 Mbps per lane.

figure 2-5 MIPI timing



Short Package S0: Start frame
S1: Frame cnt LSBs
S2: Frame cnt MSBs
S3: ECC
Tr0: Trail 0
Tr1: Trail 1
Tr2: Trail 2
Tr3: Trail 3

Long Package T0: Data type
T1: Word cnt LSBs
T2: Word cnt MSBs
T3: ECC
CRC0: CRC LSBs
CRC1: CRC MSBs
Tr0: Trail 0
Tr1: Trail 1
Tr2: Trail 2
Tr3: Trail 3

Short Package SS0: End frame
SS1: Frame cnt LSBs
SS2: Frame cnt MSBs
SS3: ECC
Tr0: Trail 0
Tr1: Trail 1
Tr2: Trail 2
Tr3: Trail 3

note 1 input clock is 24 MHz

note 2 in 8 megapixel and VGA formats, MIPI 4-lane mode, MIPI data rate is 528.5 Mbps/lane; tp is one sclk, which in this case is 100 MHz

note 3 in 1080p, EIS1080p, 720p, EIS720p, and quartersize formats, MIPI 4-lane mode, MIPI data rate is 407.8 Mbps/lane; tp is one sclk, which in this case is 100 MHz

note 4 1080p, EIS1080p, 720p, EIS720p, and VGA are generated using raw scale function, in which value (4) will vary

8825_DS_2_5

table 2-4 MIPI timing specifications (sheet 1 of 2)

mode	timing
8 Megapixel 3264x2448 24 fps	(1) 11,010,571 tp (2) 8,879 tp (3) 89,057 tp (4) 4,440 tp (5) 44,375 tp (6) 4,107 tp (7) 19 tp (8) 75,709 tp (9) 70 tp where tp = 1 sclk
1080p 3264x1836 => 1920x1080 (scale) 30 fps	(1) 6,795,497 tp (2) 7,276 tp (3) 79,272 tp (4) 7,272 or 3,640 tp (5) 52,821 tp (6) 2,246 tp (7) 19 tp (8) 51,192 tp (9) 61 tp where tp = 1 sclk
EIS1080p 3168x1782 => 2112x1188 (scale) 30 fps	(1) 6,791,403 tp (2) 7,488 tp (3) 80,234 tp (4) 3,744 or 7,488 tp (5) 36,822 tp (6) 2,666 tp (7) 19 tp (8) 63,906 tp (9) 61 tp where tp = 1 sclk
720p 3200x1800 => 1280x720 (binning + scale) 30 fps	(1) 6,795,367 tp (2) 14,645 tp (3) 96,384 tp (4) 7,320 or 14,648 tp (5) 106,952 tp (6) 1,623 tp (7) 19 tp (8) 58,781 tp (9) 61 tp where tp = 1 sclk

table 2-4 MIPI timing specifications (sheet 2 of 2)

mode	timing
EIS720p 2816x1584 => 1408x792 (binning + scale) 30 fps	(1) 6,795,367 tp (2) 14,645 tp (3) 74,432 tp (4) 7,320 or 14,648 tp (5) 48,192 tp (6) 1,782 tp (7) 14 tp (8) 58,781 tp (9) 61 tp where tp = 1 sclk
quartersize 3264x2448 => 1632x1224 (binning + scale) 30 fps	(1) 6,796,835 tp (2) 10,754 tp (3) 64,983 tp (4) 5,376 tp (5) 142,591 tp (6) 2,063 tp (7) 19 tp (8) 43,217 tp (9) 61 tp where tp = 1 sclk
VGA 1280x960 => 640x480 (skip + scale) 90 fps	(1) 2,935,433 tp (2) 9,260 tp (3) 23,646 tp (4) 4,632 or 9,256 tp (5) 95,820 tp (6) 827 tp (7) 19 tp (8) 23,382 tp (9) 68 tp where tp = 1 sclk

2.6 VSYNC timing

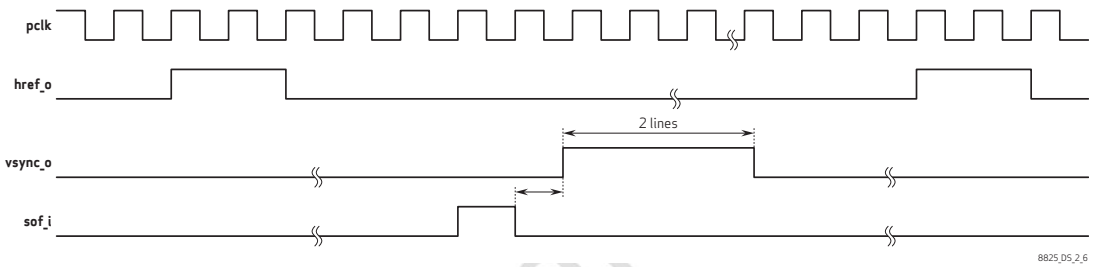
The width of VSYNC is two lines. Register bit 0x4309[0] is used to control VSYNC mode.

2.6.1 VSYNC modes

2.6.1.1 VSYNC mode 1

VSYNC mode 1 is generated by internal start of frame (sof_i) signal sof (see **figure 2-6**).

figure 2-6 VSYNC mode 1 timing



2.6.1.2 VSYNC mode 2

VSYNC mode 2 is generated by internal end of frame (eof: last href_o) (see **figure 2-7**).

figure 2-7 VSYNC mode 2 timing

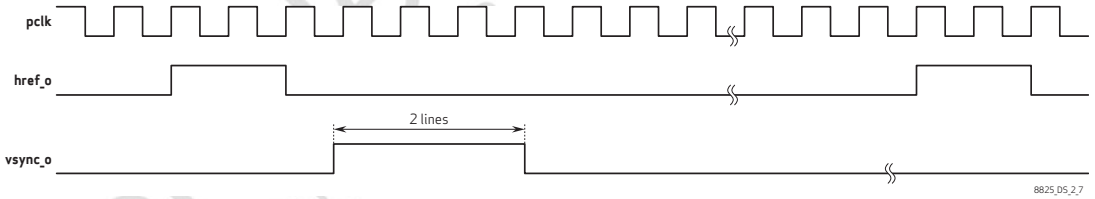


table 2-5 VSYNC control registers

address	register name	default value	R/W	description
0x4309	VSYNC MODE	1'b0	RW	Bit[0]: vsync_mode 0: Mode 1 1: Mode 2
0x361E	VSYNC POLARITY	1'b0	RW	Bit[0]: vsync_polarity 0: VSYNC output is low in active pixel period 1: VSYNC output is high in active pixel period

2.7 external interface

2.7.1 external components

Image sensor power is provided from a 2.8V (typical) system power supply. An internal regulator provides 1.5V for core logic with I/O power (DOVDD). Typical I/O pad power is 1.8V.

2.8 power up sequence

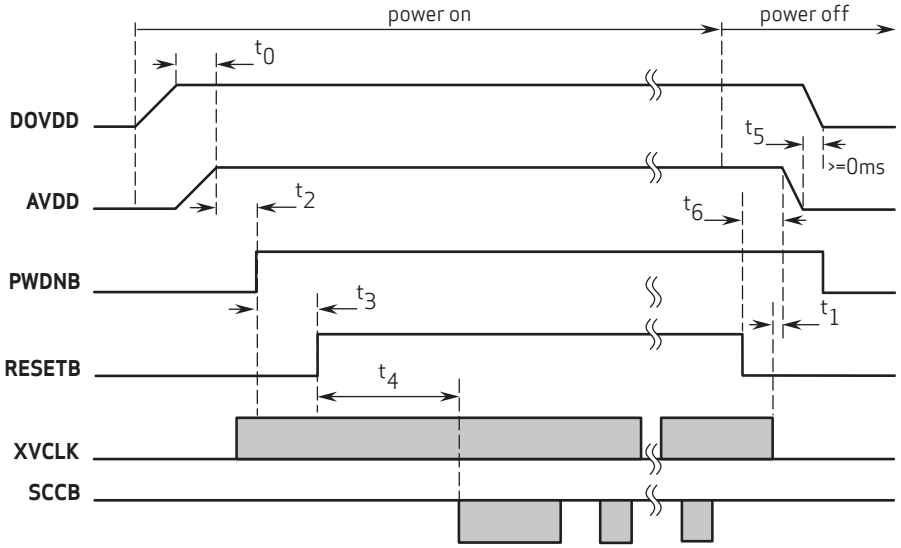
Based on the system power configuration (1.8V or 2.8V for I/O power) using external DVDD or internal DVDD, the power up sequence will differ. If 1.8V is used for I/O power, using the internal DVDD is preferred. If 2.8V is used for I/O power, due to a high voltage drop at the internal DVDD regulator, there is a potential heat issue. Hence, for a 2.8V power system, OmniVision recommends using an external DVDD source. Due to the higher power down current when using an external DVDD source, OmniVision strongly recommends cutting off all power supplies, including the external DVDD, when the sensor is not in use in the case of 2.8V I/O and external DVDD.

2.8.1 power up with internal DVDD

For powering up with the internal DVDD and SCCB access during the power ON period, the following conditions must occur:

1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
2. PWDNB is active low with an asynchronized design (does not need clock)
3. PWDNB must be low during the power on period
4. for PWDNB to go high, power must first become stable (AVDD to PWDNB ≥ 5 ms)
5. RESETB is active low with an asynchronized design
6. state of RESETB does not matter during power on period once DOVDD is up
7. master clock XVCLK should be provided at least 2 ms before host accesses the sensor's registers
8. host can access SCCB bus (if shared) during entire period. 20 ms after PWDNB goes high or 20 ms after RESETB goes high if reset is inserted after PWDNB goes high, host can access the sensor's registers to initialize sensor

figure 2-8 power up timing with internal DVDD



note $t_0 \geq 0$ms, delay from DOVDD stable to AVDD stable, it is recommended to power up AVDD shortly after DOVDD has been powered up

$t_1 \geq 0$ms, delay from XVCLK off to AVDD off

$t_2 \geq 5$ms, delay from AVDD stable to sensor power up stable, PWDNB can be pulled high after this point, XVCLK can be turned on after power on

$t_3 \geq 1$ms, delay from sensor power up stable to RESETB pull up

$t_4 \geq 20$ms, delay from RESETB pull high to SCCB initialization

$t_5 \geq 0$ms, delay from AVDD off to DOVDD off

$t_6 \geq 0$ms, delay from RESETB pull low to AVDD off

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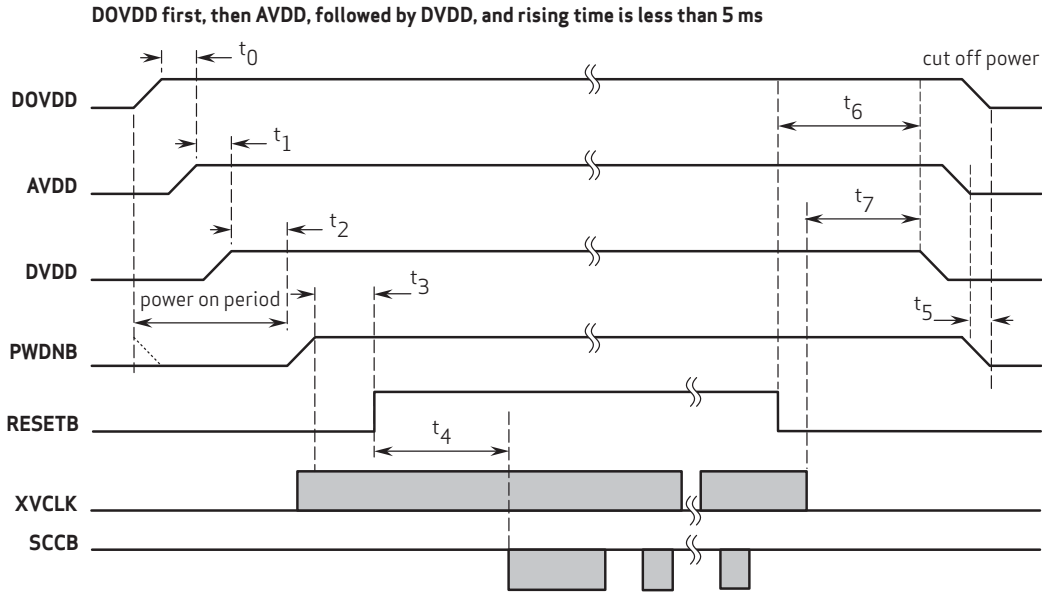
2.8.2 power up with external DVDD source

For powering up with an external DVDD source and SCCB access during the power ON period, the following conditions must occur:

1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
2. when AVDD and DVDD are turned ON, make sure AVDD becomes stable before DVDD becomes stable
3. PWDNB is active low with an asynchronized design (does not need clock)
4. for PWDNB to go high, power must first become stable (DVDD to PWDNB ≥ 5 ms)
5. all power supplies are cut off when the camera is not in use (power down mode is not recommended
6. RESETB is active low with an asynchronized design
7. state of RESETB does not matter during power on period once DOVDD is up
8. master clock XVCLK should be provided at least 2 ms before host accesses the sensor's registers
9. host can access SCCB bus (if shared) during entire period. 20 ms after PWDNB goes high or 20 ms after RESETB goes high if reset is inserted after PWDNB goes low, host can access the sensor's registers to initialize sensor

figure 2-9 power up timing with external DVDD source



note $t_0 \geq 0$ ms: delay from DOVDD stable to AVDD stable, it is recommended to power up AVDD shortly after DOVDD has been powered up
$t_1 \geq 0$ ms: delay from AVDD stable to DVDD stable
$t_2 \geq 5$ ms: delay from DVDD stable to sensor power up stable
$t_3 \geq 1$ ms, delay from sensor power up stable to RESETB pull up
$t_4 \geq 20$ms, delay from RESETB pull high to SCCB initialization
$t_5 \geq 0$ms, delay from AVDD off to DOVDD off
$t_6 \geq 0$ms, delay from RESETB pull low to DVDD off
$t_7 \geq 0$ms, delay from XVCLK off to DVDD off

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2.9 power management

During power down, all registers keep their values. So, when power is resumed all the registers are restored to their previous values.

In power down mode, the clock input of each block is turned off even when the external clock source is still clocking.

2.10 reset

The OV8825 sensor includes a **RESETB** pad (pad **08**) that forces a complete hardware reset when it is pulled low (GND). The OV8825 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register **0x0103**[0] to high. Reset requires ~2ms settling time.

2.10.1 power ON reset generation

The power on reset can be controlled from external pin. However, inside this chip, a power on reset is generated after core power becomes stable.

2.11 hardware and software standby

Two suspend modes are available for the OV8825:

- **hardware standby**
- **software standby**

2.11.1 hardware standby

To initiate a hardware standby, the **PWDNB** pad (pad **09**) must be tied to low. When this occurs, the OV8825 internal device clock is halted and all internal counters are reset and registers are maintained. Majority of the digital circuitry will remain in the power-cut state.

2.11.2 software standby

Executing a software standby through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

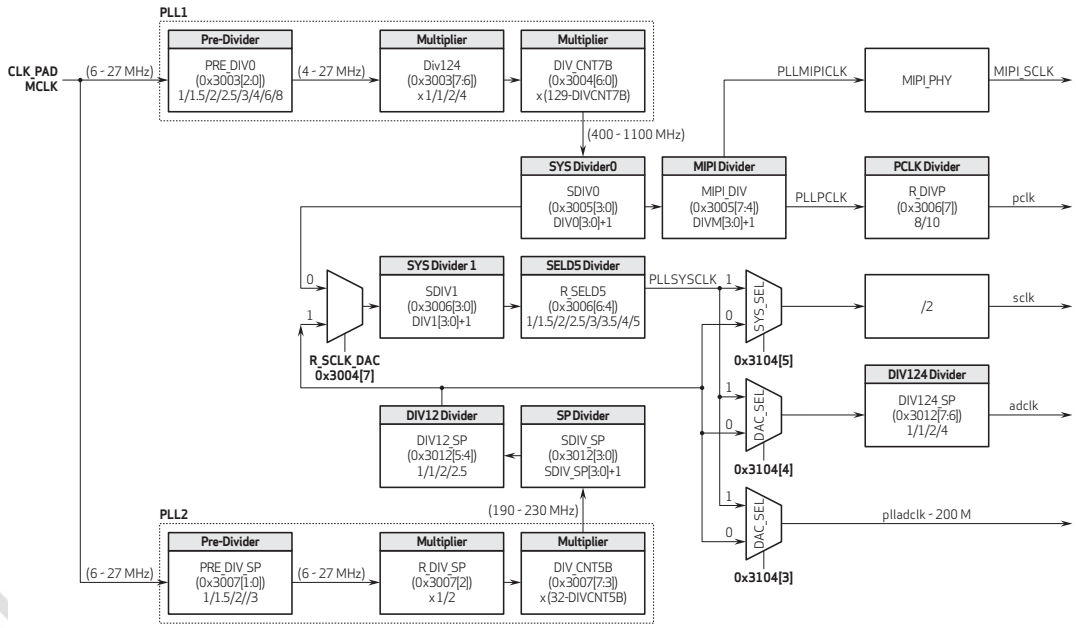
2.12 system clock control

The OV8825 has an on-chip PLL which generates the system clock from a 6~27 MHz input clock. A programmable clock divider is provided to generate different frequencies for the system.

2.12.1 PLL configuration

note
Contact your local OmniVision FAE for additional assistance on PLL configuration.

figure 2-10 OV8825 PLL clock diagram



note 1 input clock (XCLK) range is 6 - 27 MHz

note 2 clock after predivider for PLL1 is 4 - 27 MHz, for PLL2 is 6 -27 MHz

note 3 PLL1 output clock range 400 - 1100 MHz

note 4 PLL2 output clock range 190 - 230 MHz

note 5 to run full size full speed, adclck >= 200 MHz, sclk, adclk >= 100 MHz

note 6 exposure unit Line_Period = HTS/(sclk*2), where HTS = 0x380C/0x380D

note 7 frame time is Line_Period * VTS, where VTS = 0x380E/0x380F

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table 2-6 PLL configurations

configuration	register 0x3003	register 0x3004	register 0x3005	register 0x3006	register 0x3007	register 0x3012	register 0x3104
default	0x8E	0x04	0x10	0x70	0x3B	0x80	0x20
(sample 1)[a]	0xCE	0xBF	0x10	0x00	0x3B	0x80	0x20

a. Sample setting is for 24 MHz MCLK, sensor output of 8 megapixel at 24 fps with MIPI clock of 264 MHz and 4-lane MIPI output.

2.13 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

2.13.1 data transfer protocol

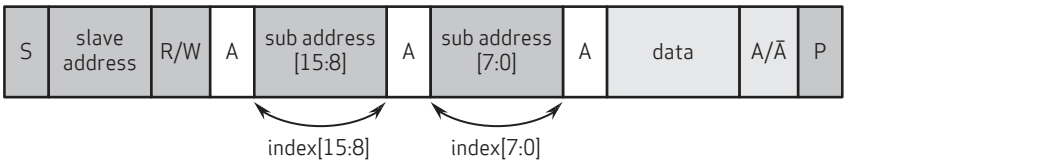
The data transfer of the OV8825 follows the SCCB protocol.

2.13.2 message format

The OV8825 supports the message format shown in **figure 2-11**. The 7-bit address of the OV8825 is 0x36 by default but can be programmed using register 0x3002[7:1]. The repeated START (Sr) condition is not shown in **figure 2-12**, but is shown in **figure 2-13** and **figure 2-14**.

figure 2-11 message type

message type: 16-bit sub-address, 8-bit data, and 7-bit slave address



from slave to master	S	START condition	A	acknowledge	
from master to slave	P	STOP condition	Ā	negative acknowledge	
direction depends on operation	Sr	repeated START condition			8825_DS_2_11

2.13.3 read / write operation

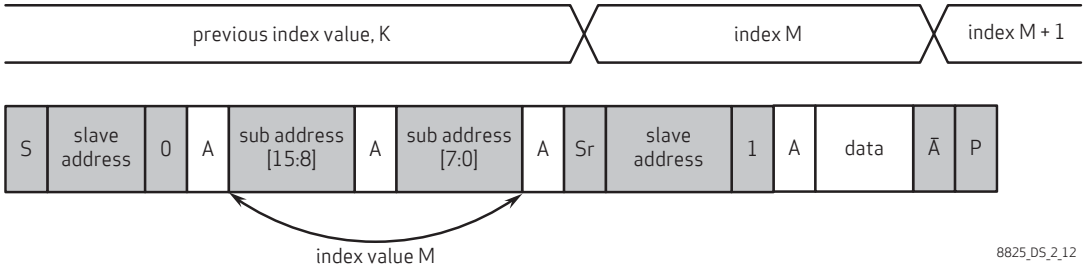
The OV8825 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

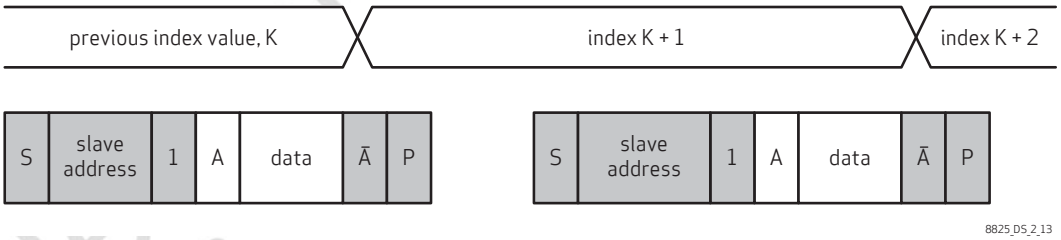
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 2-12**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-12 SCCB single read from random location



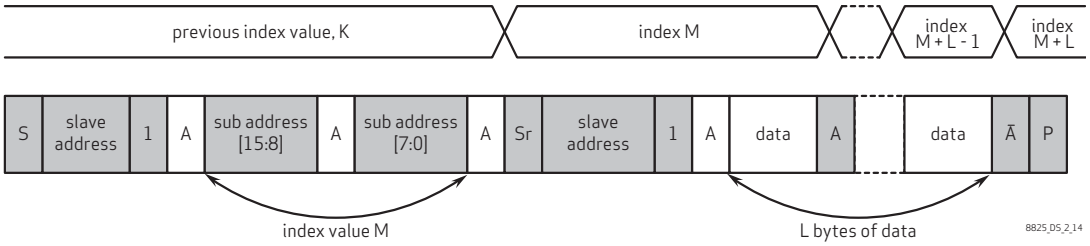
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 2-13**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-13 SCCB single read from current location



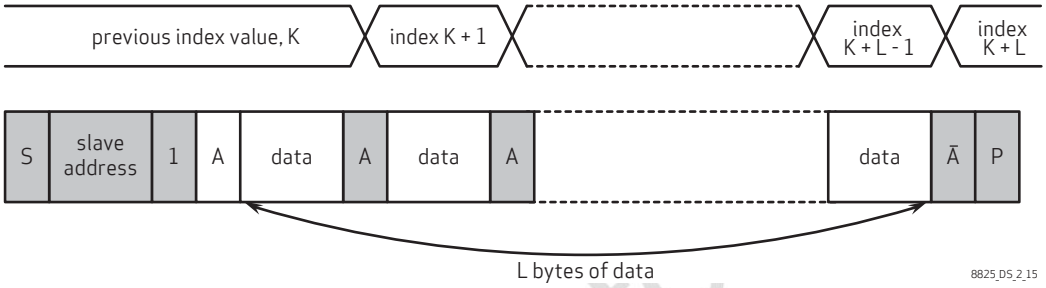
The sequential read from a random location is illustrated in **figure 2-14**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 2-14 SCCB sequential read from random location



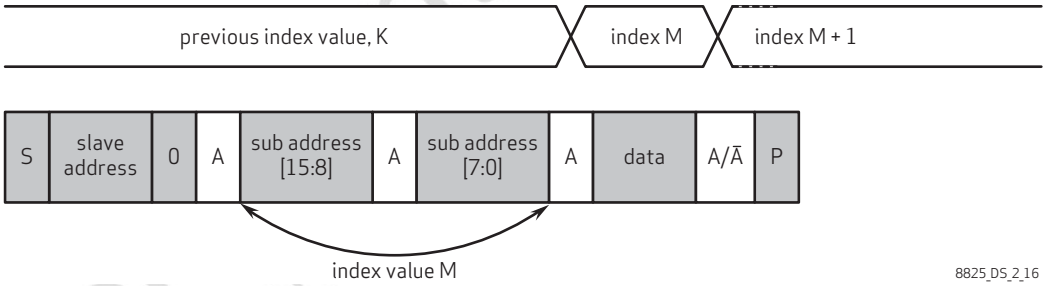
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation. as shown in **figure 2-15**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-15 SCCB sequential read from current location



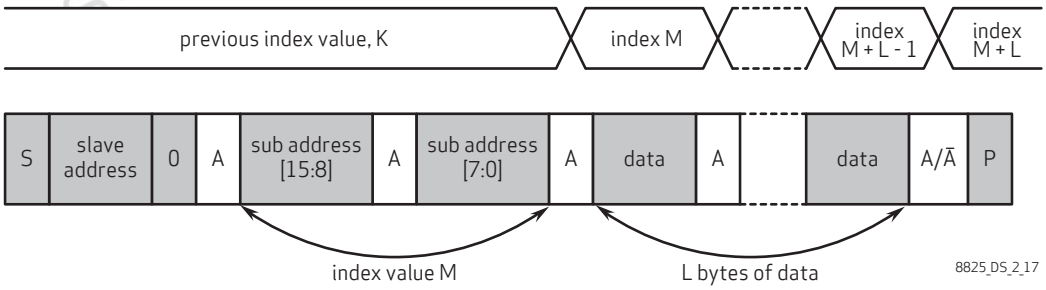
The write operation to a random location is illustrated in **figure 2-16**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 2-16 SCCB single write to random location



The sequential write is illustrated in **figure 2-17**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 2-17 SCCB sequential write to random location



2.13.4 SCCB timing

figure 2-18 SCCB interface timing

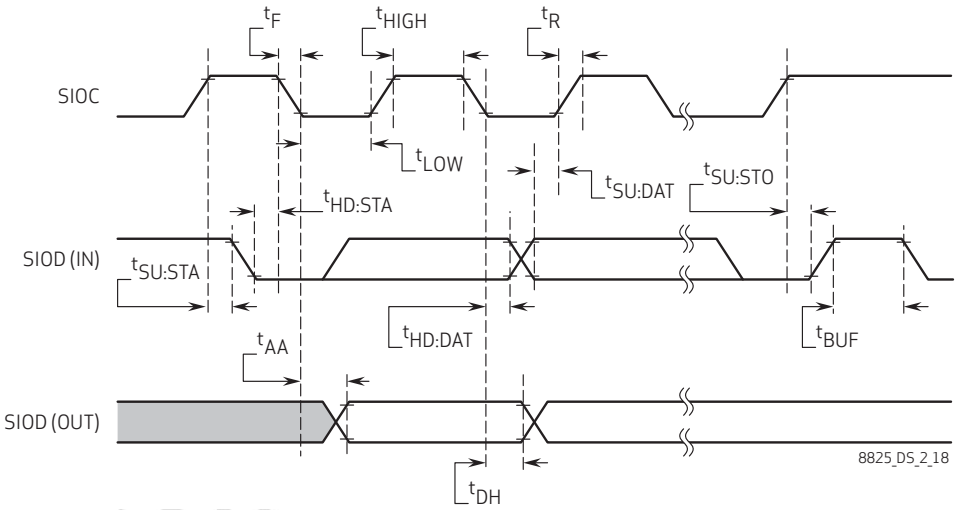


table 2-7 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SIOC}	clock frequency			400	KHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SIOC low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400KHz mode

b. timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 10%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge or/and of the falling edge signifies 90%

2.13.5 group write

Group write is supported in order to update a group of registers in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary.

The OV8825 supports up to four groups. These groups share 512 byte RAM and the size of each group is programmable by adjusting the start address.

In the OV8825, the SCCB ID is 0x6C.

table 2-8 SCCB interface register

address	register name	default value	R/W	description
0x3104	SCCB_PLL	0x20	RW	Bit[7]: Not used Bit[6]: sda_vblank Bit[5]: r_sys_sel (sclk) 0: pll2_daclk 1: pll1_sclk Bit[4]: r_dac_sel (sen_clk) 0: pll2_daclk 1: pll1_sclk Bit[3]: r_daclk (dacclk) 0: pll2_daclk 1: pll1_sclk Bit[2:0]: Debug mode

table 2-9 context switching control (sheet 1 of 2)

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Group Access Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch others: Reserved Bit[3:0]: group_id 0000: Group bank 0, default start from address 0x00 0001: Group bank 1, default start from address 0x40 0010: Group bank 2, default start from address 0x80 0011: Group bank 3, default start from address 0xB0 others: Reserved
0x3209	GRP0_PERIOD	0x00	RW	Frames For Staying in Group 0

table 2-9 context switching control (sheet 2 of 2)

address	register name	default value	R/W	description
0x320A	GRP1_PERIOD	0x00	RW	Frames For Staying in Group 1
0x320B	GRP_SWCTRL	0x01	RW	Bit[3]: group_switch_repeat Bit[2]: context_en Bit[1:0]: Second group selection
0x320D	GRP_ACT	–	R	Indicates Which Group is Active
0x320E	FRAME_CNT_GRP0	–	R	frame_cnt_grp0
0x320F	FRAME_CNT_GRP1	–	R	frame_cnt_grp1

3 block level description

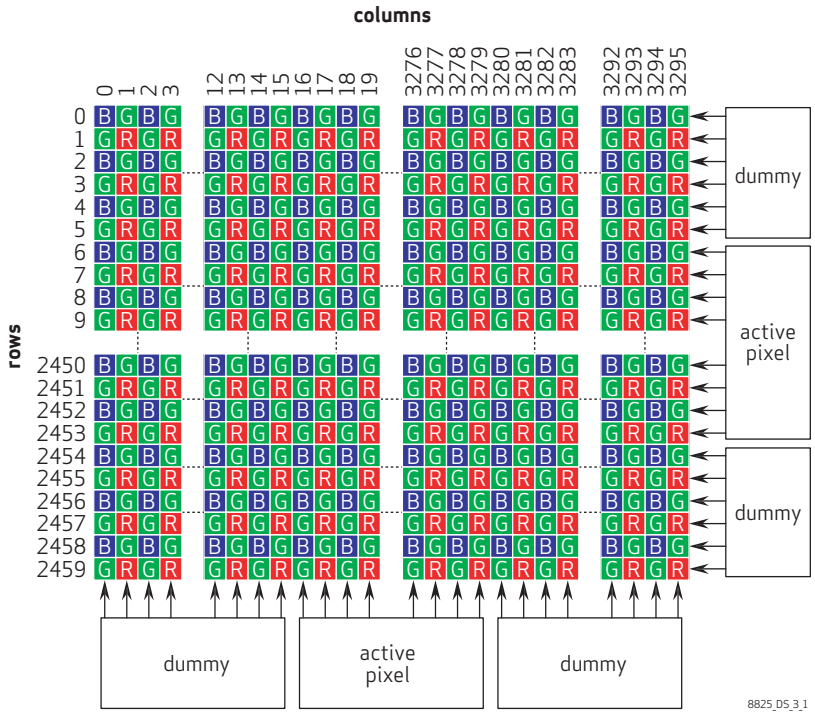
3.1 pixel array structure

The OV8825 sensor has an image array of 3296 columns by 2460 rows (8,108,160 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 8,108,160 pixels, 7,990,272 (3264x2448) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

figure 3-1 sensor array region color filter layout



3.2 subsampling

There are two subsampling modes in the OV8825: binning and skipping. Both are acceptable methods of reducing output resolution while maintaining the field of view. Binning is usually preferred as it increases the pixel's signal-to-noise ratio. When the binning function is ON, voltage levels of adjacent pixels are averaged. In skipping mode (binning function is OFF), alternate pixels, which are not output, are merely skipped. The OV8825 supports 2x2 binning. **figure 3-2** illustrates 2x2 binning, where the voltage levels of two horizontal (2x1) adjacent same-color pixels are averaged before entering the ADC. See **table 3-1** for horizontal and vertical binning registers.

figure 3-2 example of 2x2 binning

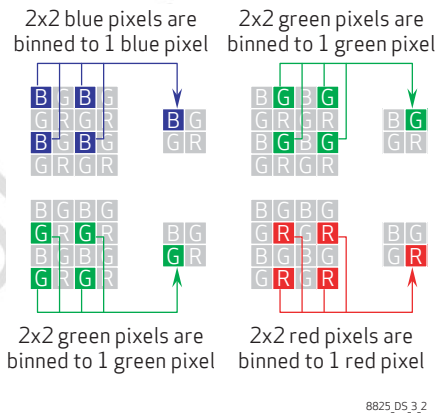


table 3-1 binning-related registers

binning/skip mode	0x370E[3]	0x3820[0]	0x3821[0]	0x6901[0]
V binning at array (avg), H binning at digital (sum)	1	0	x	0
V binning at array (avg), H binning at digital (avg)	1	0	x	1
V binning at digital (avg), H binning at array (avg)	0	1	x	0
V binning at digital (sum), H binning at array (avg)	0	1	x	1
V skip at array, H skip at array	0	0	0	x

table 3-2 binning-related registers when not in sub-sampling mode

mode[a]	0x370E[3]	0x3820[0]	0x3821[0]	0x6901[0]
full/crop mode	0	0	0	x

a. registers 0x3814=0x11 and 0x3815=0x11

4 image sensor core digital functions

4.1 mirror and flip

The OV8825 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

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table 4-1 mirror and flip registers

address	register name	default value	R/W	description
0x3820	TIMING REG20	0x00	RW	Timing Control Register Bit[2:1]: Vertical flip enable 00: Normal 11: Vertical flip
0x3821	TIMING REG21	0x00	RW	Timing Control Register Bit[2:1]: Horizontal mirror enable 00: Normal 11: Horizontal mirror

4.2 image windowing

An image windowing area is defined by four parameters, horizontal start (HS), horizontal end (HE), vertical start (VS), and vertical end (VE). By properly setting the parameters, any portion within the sensor array size can output as a visible area. Windowing is achieved by simply masking off the pixels outside of the window; thus, the original timing is not affected.

figure 4-2 image windowing

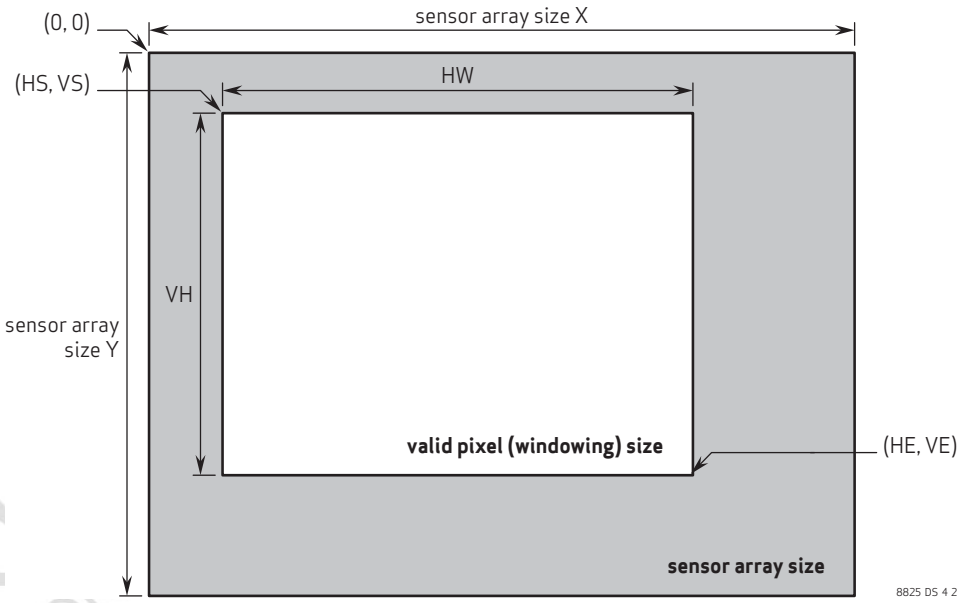


table 4-2 image windowing control functions

function	register	R/W	description
horizontal start	{0x3800, 0x3801}	RW	HS[12:8] = 0x3800 HS[7:0] = 0x3801
vertical start	{0x3802, 0x3803}	RW	VS[11:8] = 0x3802 VS[7:0] = 0x3803
horizontal end	{0x3804, 0x3805}	RW	HW[12:8] = 0x3804 HW[7:0] = 0x3805
vertical end	{0x3806, 0x3807}	RW	VH[11:8] = 0x3806 VH[7:0] = 0x3807

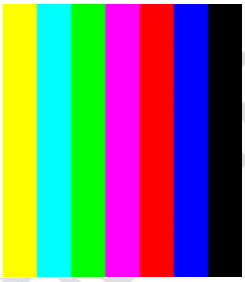
4.3 test pattern

For testing purposes, the OV8825 offers five types of test patterns:

- **general color bar**
- **test pattern I and II (16 bar)**
- **test pattern III and IV (horizontal fading)**

4.3.1 general color bar

figure 4-3 test pattern



color bar

table 4-3 general color bar selection control

function	register	default value	R/W	description
color bar	0x5E00	0x00	RW	Bit[7]: color bar enable 0: color bar OFF 1: color bar enable Bit[3:2]: color bar pattern select 00: normal color bar pattern 01: color bar pattern with vertical fading 10: color bar pattern with horizontal fading 11: color bar pattern with horizontal and vertical fading

4.3.2 test pattern I and II (16 bar)

table 4-4 test pattern I and II selection control

function	register	default value	R/W	description
test pattern I & & II	0x4303	0x00	RW	Bit[4]: 16 color bar inverse 0: normal 1: inverse Bit[3]: 16 color bar enable 0: 16 color bar OFF 1: 16 color bar enable

4.3.3 test pattern III and IV (horizontal fading)

table 4-5 test pattern III and IV selection control

function	register	default value	R/W	description
test pattern III & & IV	0x4303	0x00	RW	Bit[7]: fading enable 0: disable 1: enable Bit[6]: horizontal fading inverse 0: normal 1: inverse

4.4 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration.

Black level adjustments can be made with registers 0x4000, 0x4002, 0x4008, and 0x4009.

table 4-6 BLC control functions

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x29	RW	Bit[7]: BLC bypass enable 0: Disable bypass (BLC enabled) 1: Enable BLC bypass (no BLC)
0x4002	BLC CTRL02	0x45	RW	Bit[7]: Format change enable BLC will redo after format change Bit[6]: BLC auto enable 0: BLC offset from manual register 1: BLC offset from auto statistics Bit[5:0]: Reset frame number[5:0]
0x4008	BLC TARGET	0x00	RW	Bit[1:0]: Black level target[9:8]
0x4009	BLC CTRL09	0x10	RW	Bit[7:0]: Black target level[7:0]

4.5 one time programmable (OTP) memory

The OV8825 has a total of 2048 bits (256 bytes) of embedded one time programmable (OTP) memory. The 256 bytes of OTP memory is divided into 8 banks, each bank has 32 bytes of memory. Register 0x3D84[2:0] is a bank setting register. After setting the banks and sending a load request (register 0x3D81), the data can be loaded from registers 0x3D00~0x3D1F through the SCCB interface. The first 5 bytes of bank 0 are reserved for OmniVision FAE use and the remaining bytes of bank 0 and the reset of the banks can be used by the customer.

The OTP can be programmed through a regular SCCB write and can be read back through a regular SCCB read. For OTP write, it requires AVDD to be 2.5V±5% and for OTP read, there is no such restriction.

table 4-7 OTP control functions

function	register	description
OTP program	0x3D80	Bit[0]: program OTP
OTP load / dump	0x3D81	Bit[0]: load / dump OTP
OTP bank select	0x3D84	Bit[3]: bank mode enable Bit[2:0]: bank index
dump / program data n	0x3D00 ~ 0x3D1F	Bit[7:0]: data dumped or data to be programmed for bits[8*(n+1)-1:8*n]

The following sections provide instructions on how to program the OTP (can only be done once) and how to read back the OTP (can be done multiple times). Before read/write, make sure all sensor powers are properly provided and the sensor is up and running. The OTP module is at default enabled state, 0x301C[4] is 1 and 0x301C[0] is 0.

4.5.1 OTP program

An example of programming OTP addresses 0x3D1C~0x3D1F is shown below. If the whole bank is not being programmed, make sure non-programmable addresses 0x3D00~0x3D1B are at default value of 0 to avoid accidental programming to other OTP addresses.

```
6C 3D80 00
6C 3D84 09 ; set bank 1
6C 3D1C 1C
6C 3D1D 1E
6C 3D1E 1F
6C 3D1F 20
;//PROGRAM to bank 1 OTP
6C 3D80 01
;
#delay 25ms
6C 3D80 00
```

4.5.2 OTP read

After programming and at any time after the sensor is powered on, use the procedure shown below to read back the OTP values. Before each read, the user can clear 0x3D00~0x3D1F registers first if just finished write.

```
6C 3D84 09 ; set bank 1
6C 3D81 01 ; OTP read enable
#delay 3ms
6C 3D1C ; read bank 1 data 29
6C 3D1D ; read bank 1 data 30
6C 3D1E ; read bank 1 data 31
6C 3D1F ; read bank 1 data 32
```

4.6 temperature sensor

The OV8825 supports an on-chip temperature sensor that covers 0~80°C with an error range of 5°C. It can be controlled through the SCCB interface (see **table 4-8**). When the temperature is lower than 0°C, the reading will stop at 0°C. Before reading the temperature, the temperature sensor should be triggered by a 0 to 1 transition of register bit 0x670B[7].

This module needs a 1-3MHz clock divided from XVCLK. If XVCLK is 24MHz, 0x6706[3:0] must be set to 4'b1000.

table 4-8 temperature sensor functions

function	register	R/W	description
temp clock divisor	0x6706	RW	Bit[3:0]: Temp clock divisor Sample clock = XVCLK/clock divisor Divisor = 1 if bit[3:0] = 0 Sample clock must be around 3MHz
TPM trigger / read	0x670B	RW	Bit[7]: temperature sensor trigger Bit[6:0]: measured temperature

4.7 context switching

The OV8825 supports a shadowing of registers that enable the pre-loading of two different configurations of window, subsampling, scaling, integration time, and gain. With one register controlling which bank is the active settings, the OV8825 supports switching from context A to context B in X frames where X frames is up to 255 frames. The OV8825 supports staying at context B for a programmable number of frames from 1 to 255 frames where a value of 0 is to stay at context B until changed. This sync should also be coordinated with strobe control.

4.7.1 context switching time

For any case where the context switching starts off as electronic rolling shutter and ends with electronic rolling shutter, the changes will take effect in the second frame. This mode is inclusive of auto exposure where there is a change to integration time but the context is not actually changed.

For any case where the context starts off as one mode and switches to the other mode, this change will happen in the next frame. If the switch is received while a frame is being read out, then that frame will continue to be read out until complete and the next frame will be the new mode. If the command is issued while a frame is not being read out (i.e., the last row of frame n-1 is completed and the first row of frame n has not started to be read yet), then the current rows being exposed are abandoned and the mode is changed immediately.

Both of these statements are inclusive of changes to binning, integration time, resolution, and resizing. There are three possible changes that can happen:

- a change that does not result in a sensor mode change
- a sensor mode change from electronic rolling shutter to global shutter
- a sensor mode change from global shutter to electronic rolling shutter

table 4-9 context switching latency

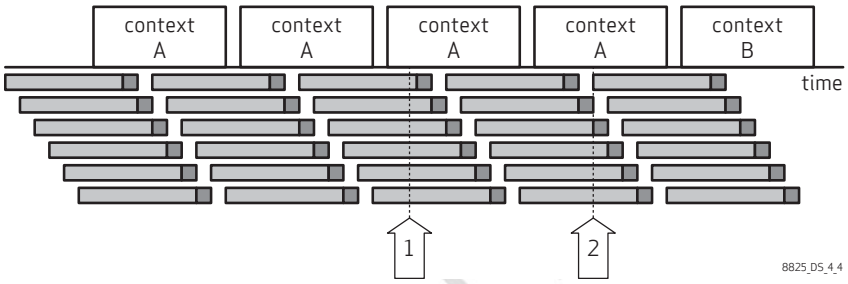
mode change	latency[a]
context change with no mode change	1 frame
electronic rolling shutter to global shutter	<5 µs
global shutter to electronic rolling shutter	<1 ms

a. where latency is from the last row read out in the current mode to when integration of the next mode starts

4.7.1.1 example 1

In example 1, we issue a change from context A to context B where both context A and context B is electronic rolling shutter. The change is issued at node 1. The next frame is unchanged and the following frame changes to context B. Although this change is shown as a change from context A to context B, it is also represented by a change to exposure within context A.

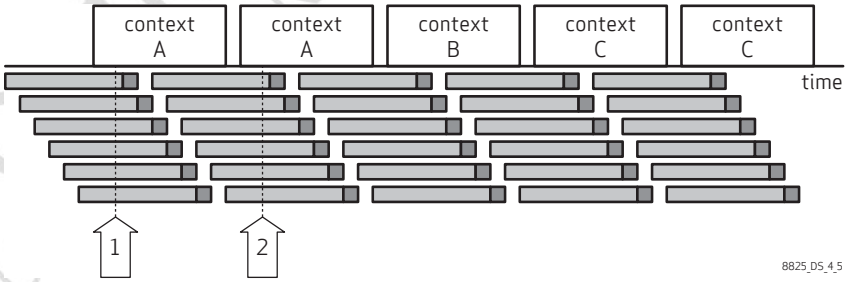
figure 4-4 context switching without sensor mode change



4.7.1.2 example 2

Example 2 illustrates a multiple consecutive context switch. In this example, we issue a change from context A to context B to context C in three consecutive frames where context A, context B, and context C are electronic rolling shutter and can have different integration times. The change is issued at node 1. The next frame is unchanged and the following frame changes to context B. Context B to context C changes are issued at node 2. The frame after context B will be changed to context C.

figure 4-5 multiple consecutive context switching



4.7.1.3 example 3

Context A is full resolution with 2x2 binning at 15 fps with electronic rolling shutter with duration of 0. Context B is full resolution at 15 fps with global reset and mechanical shutter with duration of 1 frame. The system stays at context A until told to change because duration is set to 0. At node 1, the command is sent to change to context B. The sensor finishes sending the data for the current frame. The rows currently integrating for the next frame are lost. The shutter is intended to close at 3, however, because of the programmed delay, the signal is sent at node 2 to overcome system latency. At node 5, the system switches back to context A with electronic rolling shutter.

figure 4-6 electronic rolling shutter to global reset context switching example

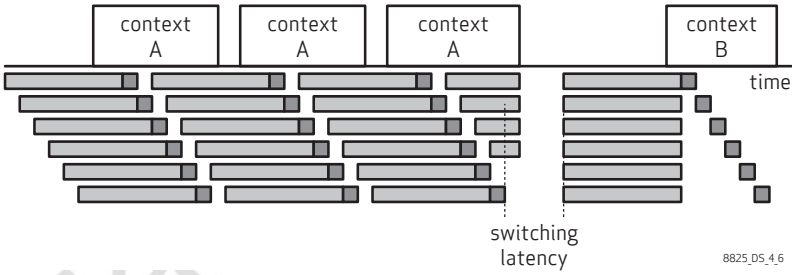
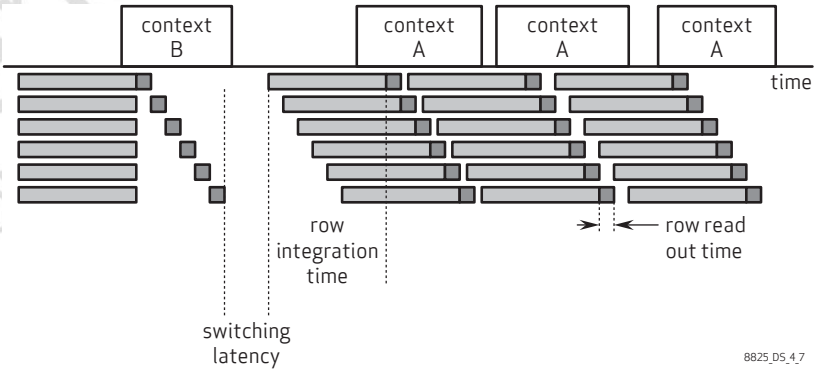
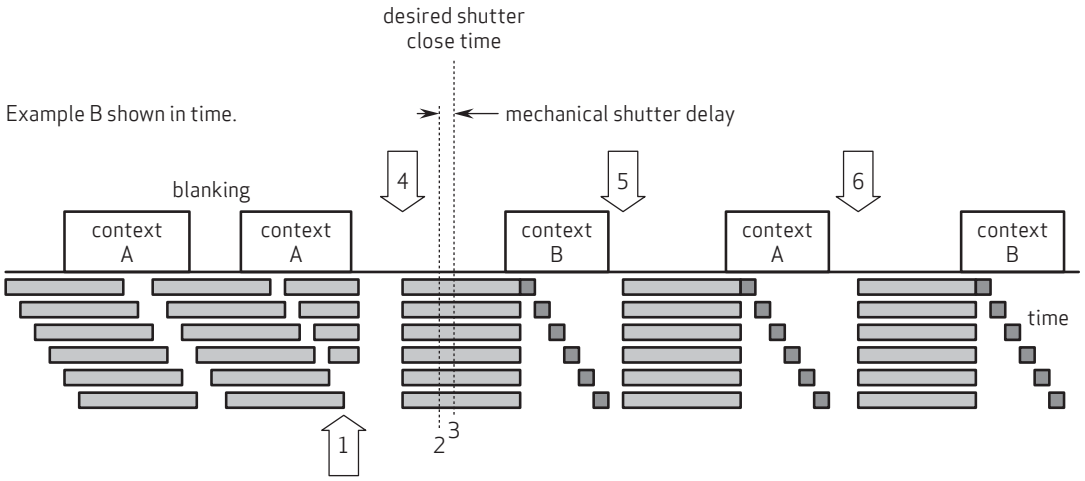


figure 4-7 context change for global reset to electronic rolling shutter



4.7.1.4 bracketed exposure example

figure 4-8 bracketed exposure context example



Where 4 has an EV of -1, 5 has an EV of 0 and 6 has an EV of +1.
This would require each context to be set to duration of 1 frame,
and the integration time would need to be reprogramed while other context is active.

Context A: Full res, 2x2 binning, 15 fps, ERS, indefinite.
Context B: Full res, 15 fps 1 frame mechanical shutter with global reset.

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4.7.2 context switching control

The OV8825 supports switching between two different groups of sensor configuration. It can be controlled through the SCCB interface (see **table 4-10**). Each group can define up to 84 registers. Switching point and length are defined based on concept of number of frames, which can be up to 255 frames.

table 4-10 context switching control functions

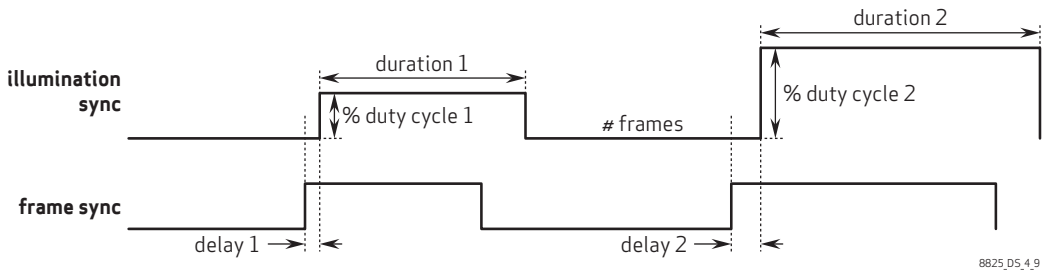
function	register	description
group access	0x3208	Bit[7:4]: group_ctrl 0000: group hold start 0001: group hold end 1010: group launch others: reserved Bit[3:0]: group_id 0000: group bank 0 (default start from address 0x00) 0001: group bank 1 (default start from address 0x40) 0010: group bank 2 (default start from address 0x80) 0011: group bank 3 (default start from address 0xB0) others: reserved
grp0_period	0x3209	frames for staying in grp0
grp1_period	0x320A	frames for staying in grp1
grp_swctrl	0x320B	Bit[3]: group_switch_repeat Bit[2]: context_en Bit[1:0]: second group selection

4.8 illumination control

The OV8825 supports illumination control. It can be controlled through the SCCB interface (see **table 4-11**). The PWM duration and duty cycle are programmable.

The PWM is programmed such that a frame is divided into 32 time slots. Each frame is PWM cycle.

figure 4-9 illumination diagram 1



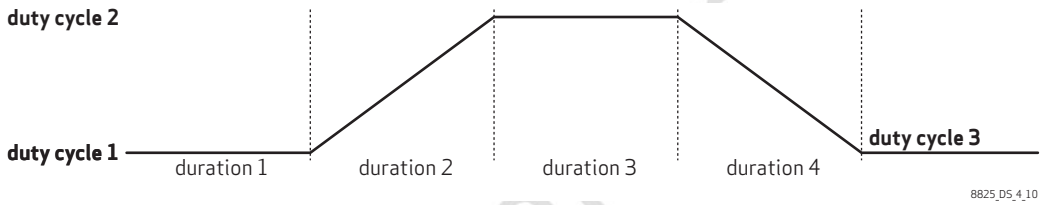
Delays are from -0.5 of a frame to 0.5 of frame with 5-bit resolution, where 16 is equal to zero delay. The step is a time slot. Zero delay is the default value.

The gap between the two PWMs is number of frames, which can be programmable from 0 to 255, with zero as the default.

Duration is programmable from 0 to 16 frames with 4-bit resolution. Each step is a frame.

In the case where the delay + duration results in the illumination ending prior to the end of a frame, the number of frames starts at the next full frame.

figure 4-10 illumination diagram 2



In this case, the PWM duration 1 and duration 3 have the same control as the Illumination case 1. For Duration 2 and Duration 4, the ramps can be smoothed out. Both the duty cycle step for each frame increase and the frame number, which repeats the same duty cycle, can be set by registers.

If the repeat bit is set, the waveform will repeat until cleared. After clearing the repeat bit, the waveform will finish one full cycle before taking effect. This means that Duration 4 should be completed in its entirety before the cycle is ended.

table 4-11 illumination control functions (sheet 1 of 2)

function	register	description
PWM 1 delay	0x6600	Bit[4:0]: PWM1 delay 0~31 0x00: -0.5 frame 0x31: 0.5 frame
PWM 2 delay	0x6601	Bit[4:0]: PWM2 delay 0~31 0x00: -0.5 frame 0x31: 0.5 frame
PWM 3 delay	0x6602	Bit[4:0]: PWM3 delay 0~31 0x00: -0.5 frame 0x31: 0.5 frame
PWM 4 delay	0x6603	Bit[4:0]: PWM4 delay 0~31 0x00: -0.5 frame 0x31: 0.5 frame
duration control 0	0x6604	Bit[7:4]: PWM2 duration width (0~15 frames) Bit[3:0]: PWM1 duration width (0~15 frames)

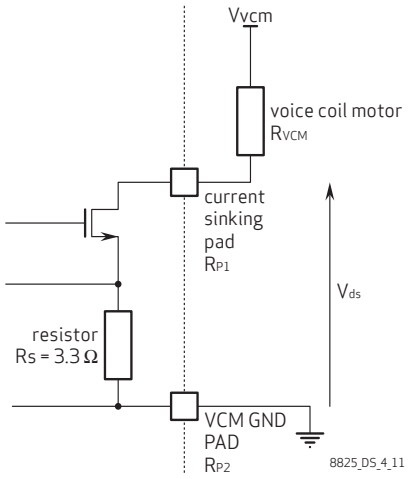
table 4-11 illumination control functions (sheet 2 of 2)

function	register	description
duration control 1	0x6605	Bit[7:4]: PWM4 duration width (0~15 frames) Bit[3:0]: PWM3 duration width (0~15 frames)
PWM 1 duty cycle control	0x6606	Bit[4:0]: PWM1 duty cycle 0~31
PWM 2 duty cycle control	0x6607	Bit[4:0]: PWM2 duty cycle increase step 0~31
PWM 3 duty cycle control	0x6608	Bit[4:0]: PWM3 duty cycle 0~31
PWM 4 duty cycle control	0x6609	Bit[4:0]: PWM4 duty cycle decrease step 0~31
gap1 control	0x660A	Bit[7:0]: gap between PWM1 and PWM2
gap2 control	0x660B	Bit[7:0]: gap between PWM2 and PWM3
gap3 control	0x660C	Bit[7:0]: gap between PWM3 and PWM4
gap4 control	0x660D	Bit[7:0]: gap between PWM4 and PWM1 when repeat is ON
illum_ctrl	0x660E	Bit[7]: pwm_request Bit[5]: illum_sel Bit[0]: repeat_en

4.9 VCM driver

The OV8825 supports VCM control. It can be controlled through the SCCB interface (see **table 4-12**). Different target, slew, and step can be controlled.

figure 4-11 VCM block diagram



The maximum SINK current can be estimated as:

- ISINK = (Vvcm - Vds) / (Rs + Rvcm + Rp1 + Rp2)
- Vds is the transistor headroom
- Rp1 and Rp2 are the resistance in the current path
- RVCM is the resistance of the voice coil motor.

The OV8825 VCM driver is a single 10-bit DAC with 100 mA output current sink capability. It is designed for linear control of the VCM. The DAC is controlled via the SCCB interface. The OV8825 VCM driver provides three types of output current control modes that allow users to adjust transient response of the sinking current.

4.9.1 output current mode

The OV8825 VCM driver uses four bits (S3, S2, S1, and S0) to control the output current response.

- S[3:0] = X000: Directly jump mode: code directly jumps to target code (see **figure 4-12**). Output current transient response time is shown in **table 8-5**.
- S[3:0] = 0001 to 0111: Single step mode: code increases/decreases by a single step. Single step time durations are 50µs, 100µs, 200µs, 400µs, 800µs, 1600µs, and 3200µs, which are controlled by S2, S1, and S0 (see **table 4-13**).
- S[3:0] = 1001 to 1111: Multi-code steps mode: Code increases/decreases in multi-code steps. If the target code and the current code have a difference larger than 128, the 64-code step is applied first. When the difference in between target and current codes is no more than 128 but larger than 16, the 16-code step is used. When the difference is less than 16, it will directly jump to the target code. Single step time options are 50µs, 100µs, 200µs, 400µs, 800µs, 1600µs, and 3200µs, which are controlled by S2, S1, and S0 (see **table 4-14**).

table 4-12 VCM control functions (sheet 1 of 2)

function	register	description
A_VCM_LOW	0x3618	Bit[7:4]: din[3:0] Bit[3]: s3 Bit[2:0]: s[2:0]
A_VCM_MID0	0x3619	Bit[7]: pdin Bit[6]: rv14 Bit[5:0]: din[9:4]
A_VCM_MID1	0x361A	Bit[7:0]: rdiv[7:0]
A_VCM_MID2	0x361B	Bit[7]: rmsb_inv 0: Normal 1: Switch **A_VCM_LOW** and **A_VCM_MID0** Bit[6]: rs14 Bit[5]: rs13 Bit[4]: vcm_rih_o Bit[3:0]: rdiv[11:8]

table 4-12 VCM control functions (sheet 2 of 2)

function	register	description
A_VCM_HIGH	0x361C	Bit[7:3]: Not used Bit[2:0]: VCM output current control 000: 0.71 * Id 001: 0.77 * Id 010: 0.83 * Id 011: 0.91 * Id 100: 1.00 * Id 101: 1.11 * Id 110: 1.25 * Id 111: 1.43 * Id

table 4-13 single step mode

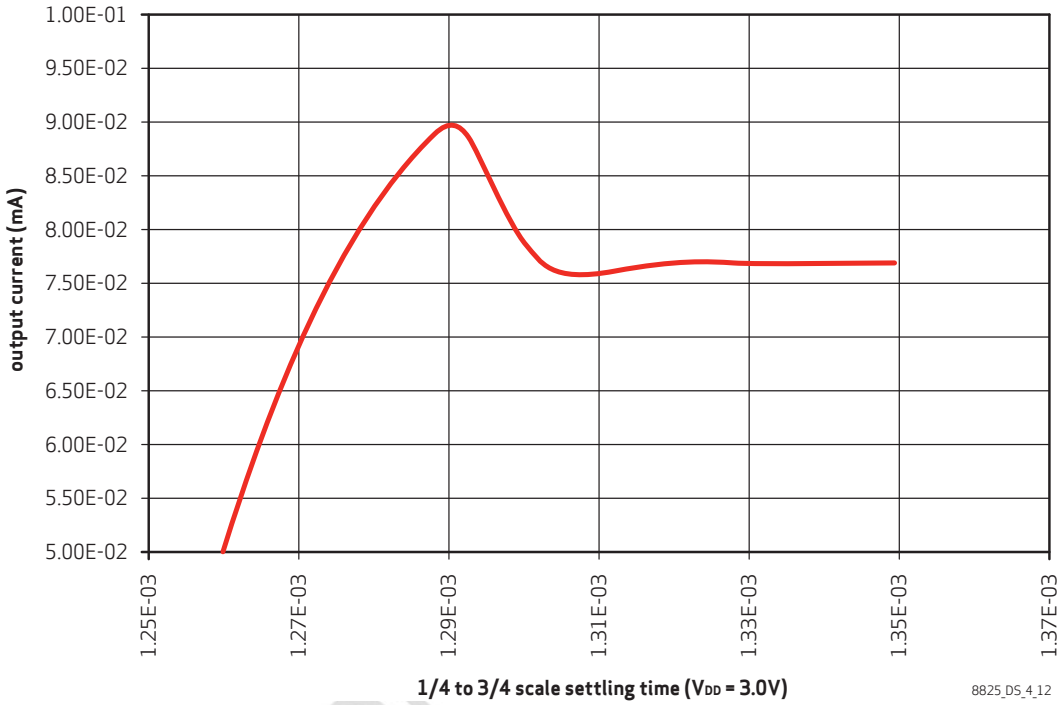
mode	S3	S2	S1	S0	single step transition time	full scale transition time (1023 steps)
single step mode	0	0	0	1	50µs	51.15ms
	0	0	1	0	100µs	102.3ms
	0	0	1	1	200µs	204.6ms
	0	1	0	0	400µs	409.2ms
	0	1	0	1	800µs	818.4ms
	0	1	1	0	1600µs	1.637s
	0	1	1	1	3200µs	3.274s

table 4-14 multi-code step mode

mode	S3	S2	S1	S0	single step transition time	full scale transition time (22 steps)[a]
single step mode	1	0	0	1	50µs	1.1ms
	1	0	1	0	100µs	2.2ms
	1	0	1	1	200µs	4.4ms
	1	1	0	0	400µs	8.8ms
	1	1	0	1	800µs	17.6ms
	1	1	1	0	1600µs	35.2ms
	1	1	1	1	3200µs	70.4ms

a. a full scale transition includes fourteen 64-code steps, seven 16-code steps and one directly jump step.

figure 4-12 1/4 to 3/4 scale settling time (directly jump mode, VDD = 3.0V)



4.10 strobe flash and frame exposure

4.10.1 strobe flash control

The strobe signal is programmable. It supports both LED and Xenon modes. The polarity of the pulse can be changed. The strobe signal is enabled (turned high/low depending on the pulse's polarity) by requesting the signal via the SCCB interface. Flash modules are triggered by the rising edge by default or by the falling edge if the signal polarity is changed. The OV8825 supports the following flashlight modes (see **table 4-15**).

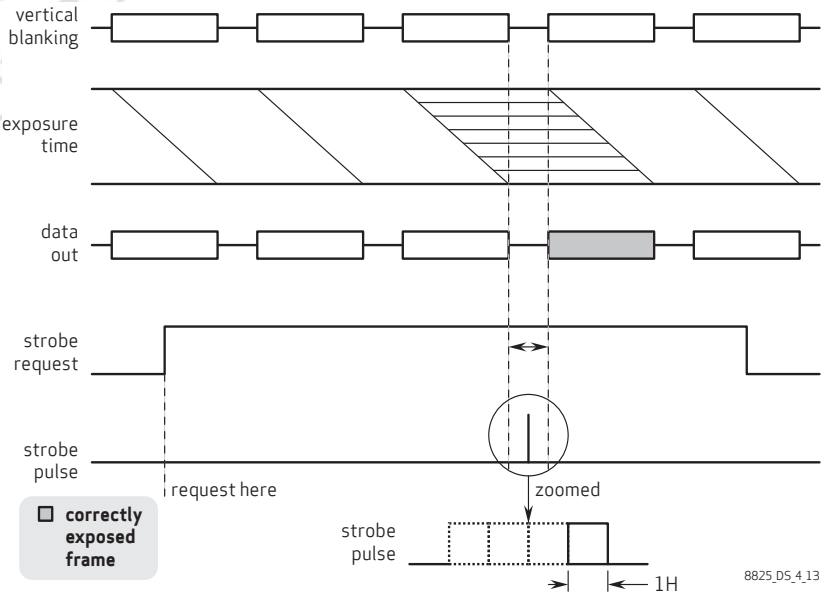
table 4-15 flashlight modes

mode	output	AEC / AGC	AWB
xenon	one-pulse	no	no
LED 1	continuous	yes	yes
LED 2	one-pulse	yes	yes

4.10.1.1 xenon flash control

After a strobe request is submitted, the strobe pulse will be activated at the beginning of the third frame (see **figure 4-13**). The third frame will be correctly exposed. The pulse width can be changed in Xenon mode between 1H and 4H, depending on register 0x3B00[5:4], where H is one row period.

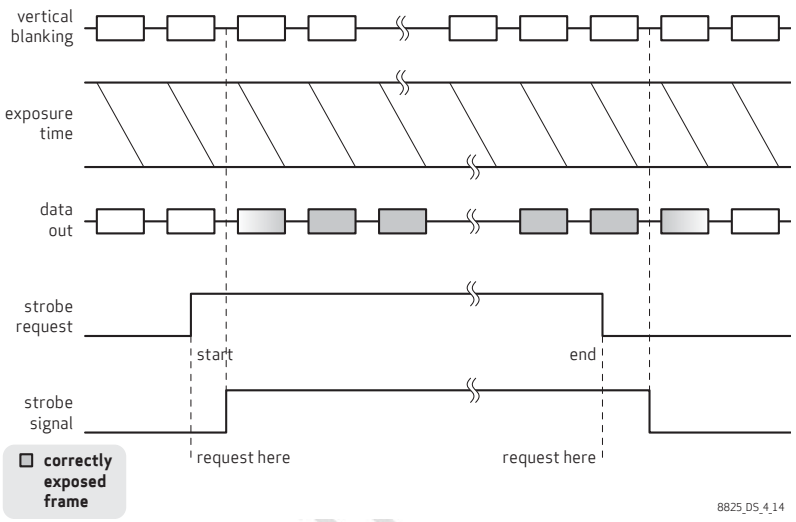
figure 4-13 xenon flash mode



4.10.1.2 LED 1 mode

In LED 1 mode, the strobe signal stays active until the strobe end request is sent (see **figure 4-14**).

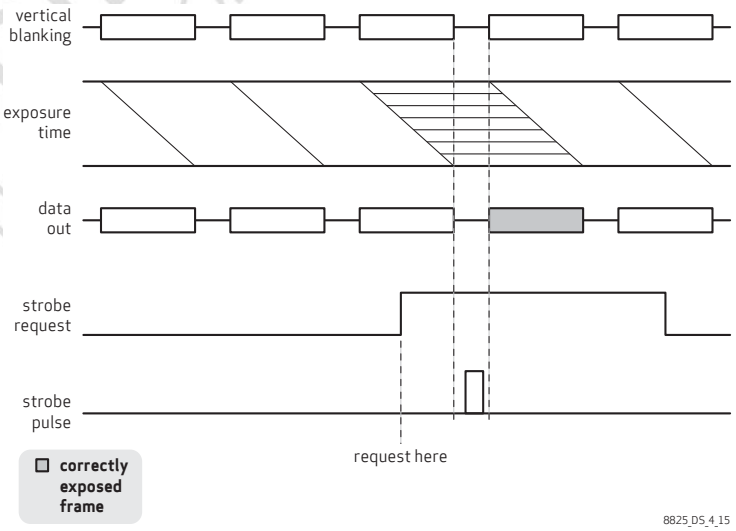
figure 4-14 LED 1 mode



4.10.1.3 LED 2 mode

In LED 2 mode, the strobe signal width is controlled by register 0x3B02 (see **figure 4-15**). Strobe width = 128 × (2**0x3B02[1:0]) × (0x3B02[7:2] + 1) × sclk_period. The maximum value of 0x3B02[7:2] is 6'b111110.

figure 4-15 LED 2 mode



4.10.2 frame exposure (FREX) mode

In FREX mode, all pixels in the frame start integration at the same time, rather than integrating row by row. After a user-defined exposure time, the mechanical shutter should be closed, preventing further integration and the image begins to read out. After the readout finishes, the shutter opens again and the sensor resumes normal mode, waiting for the next FREX request.

The OV8825 supports two modes of FREX (see **figure 4-16** and **figure 4-17**):

figure 4-16 FREX mode 1

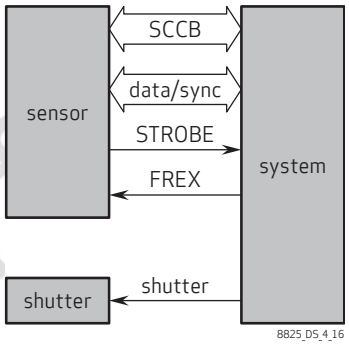
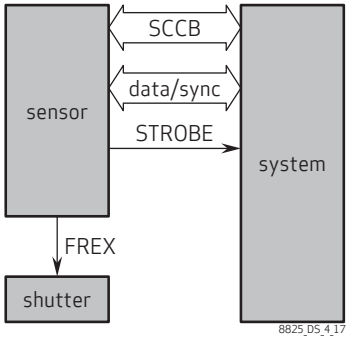


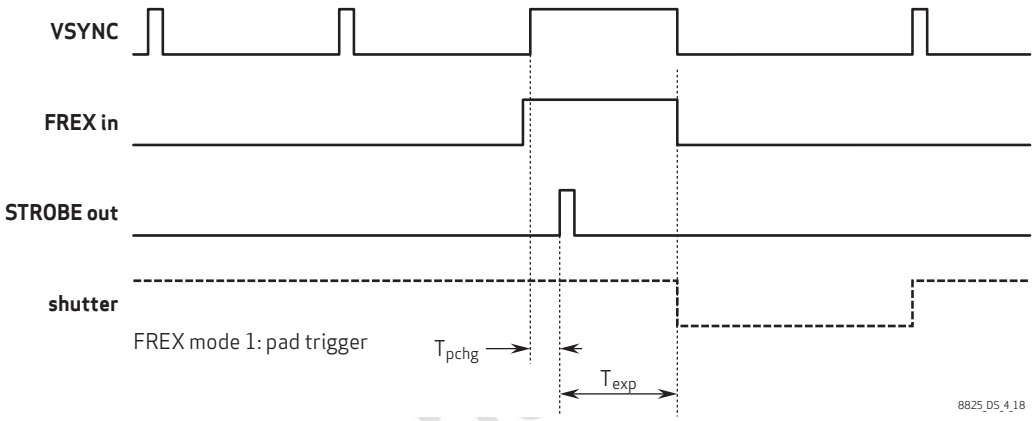
figure 4-17 FREX mode 2



In mode 1, the FREX pin is configured as an input while it is configured as an output in mode 2. In both mode 1 and mode 2, the strobe output is irrelevant with the rolling strobe function. When in rolling shutter mode, the strobe function and this FREX/shutter control function do not work at the same time.

The timing diagram for mode 1 is shown in **figure 4-18**.

figure 4-18 FREX mode 1 timing diagram



In mode 1, the host asserts FREX at any time in preview mode (mechanical shutter is open at this time). The sensor will trigger STROBE to indicate the start of exposure time. Exposure time is calculated from the STROBE rising edge to when the mechanical shutter closes. The host will control when to close the mechanical shutter (shutter delay is handled by the host). The host can re-open the shutter after receiving the entire image data or the next VSYNC signal.

The timing diagrams for mode 2 are shown in **figure 4-19** and **figure 4-20**.

figure 4-19 FREX mode 2 (shutter delay = 0) timing diagram

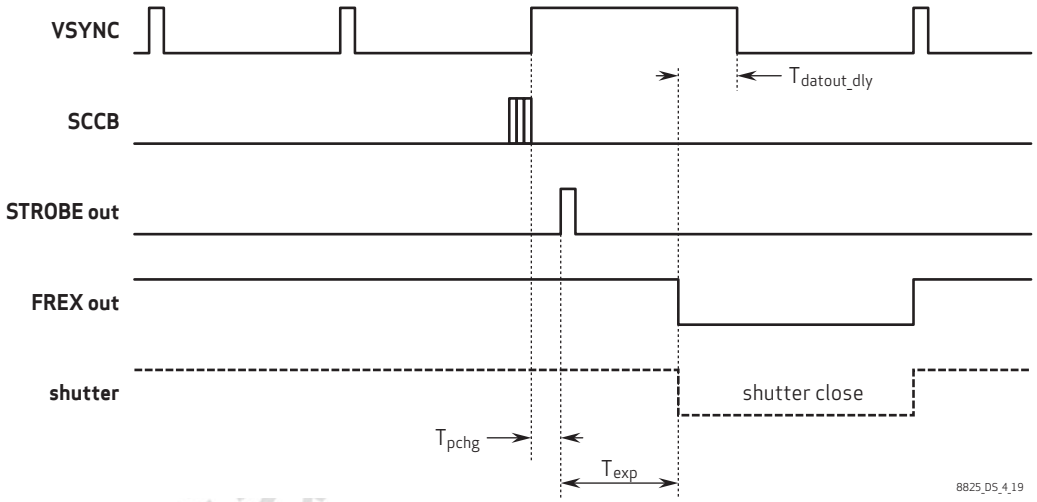
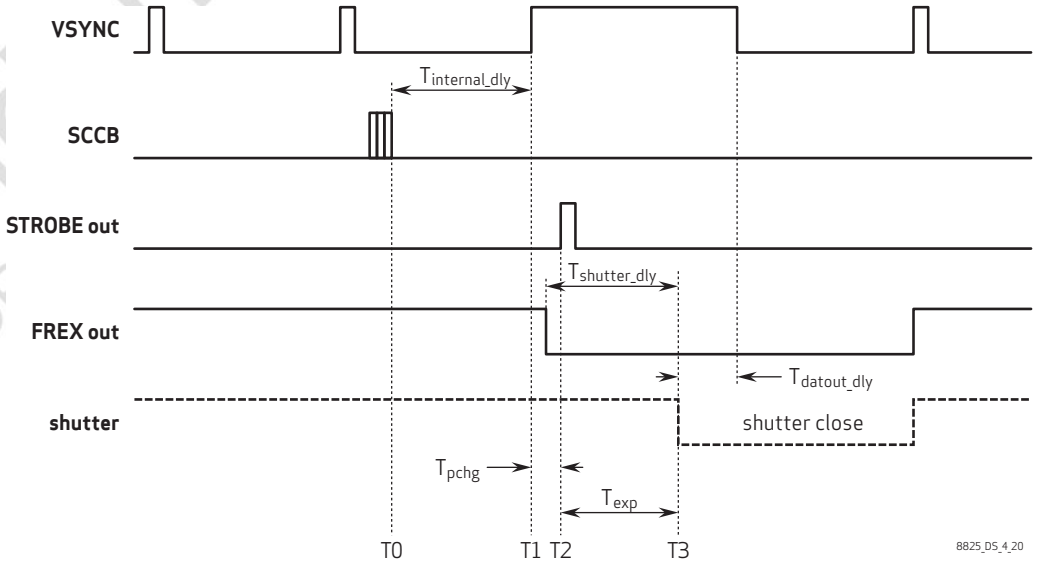


figure 4-20 FREX mode 2 (shutter delay > 0) timing diagram



Before using mode 2, the host needs to program exposure time at (frex_exp), shutter delay (registers **0x3B0C**, **0x3B0D**), strobe width, and data output delay. The host triggers this mode by SCCB at any time in preview mode (mechanical shutter is open at this time). The sensor can either start frame exposure right away (since the current data packet is broken, the receiver may get a packet error) or wait for the current frame to finish (controlled by register). The sensor will

trigger STROBE to indicate the start of exposure time. Exposure time is calculated from STROBE rising edge to when the mechanical shutter closes. The host can control the sensor to start sending image data after a certain delay (registers **0x3B10**, **0x3B11**) after FREX goes low. The host can re-open the shutter after receiving the entire image data or the next VSYNC signal.

See **table 4-16** for FREX strobe control functions.

table 4-16 FREX strobe control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B00	STROBE CTRL00	0x00	RW	Bit[7]: Strobe request ON/OFF Bit[6]: Strobe polarity 0: Active high 1: Active low Bit[5:4]: Pulse width in xenon mode Bit[2:0]: Strobe mode select 000: Xenon 011: LED1 100: LED2
0x3B01	STROBE CTRL01	0x00	RW	Bit[3]: start_point_sel Bit[2]: Strobe repeat enable Bit[1:0]: Strobe latency 00: Strobe generated at next frame 01: Delay one frame, strobe generated 2 frames later 10: Delay one frame, strobe generated 3 frames later 11: Delay one frame, strobe generated 4 frames later
0x3B02	STROBE CTRL02	0x00	RW	Bit[7:2]: Strobe pulse width step Bit[1:0]: Strobe pulse width gain Strobe pulse width = 128 × (2**gain) × (step+1) × sclk_period
0x3B05	FREX CTRL 00	0x00	RW	Bit[7:0]: frex_exp[23:16] MSB of frame exposure time in mode 2. Exposure time is in units of 128 x (2**gain) x (step+1) x sclk_period. See **0x3B06** and **0x3B07**.
0x3B06	FREX CTRL 01	0x00	RW	Bit[7:0]: frex_exp[15:8] Middle byte of frame exposure time in mode 2. See **0x3B05** and **0x3B07**.
0x3B07	FREX CTRL 02	0x00	RW	Bit[7:0]: frex_exp[7:0] LSB of frame exposure time in mode 2. See **0x3B05** and **0x3B06**.
0x3B09	FREX CTRL 04	0x00	RW	Bit[3:0]: strobe_width[19:16] MSB of strobe width in mode 2. Strobe width is in units of 1 clock cycle. See registers **0x3B0A** and **0x3B0B**.

table 4-16 FREX strobe control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B0A	FREX CTRL 05	0x00	RW	Bit[7:0]: strobe_width[15:8] Middle byte of strobe width in mode 2. See registers **0x3B09** and **0x3B0B**.
0x3B0B	FREX CTRL 06	0x00	RW	Bit[7:0]: strobe_width[7:0] LSB of strobe width in mode 2. See registers **0x3B09** and **0x3B0A**.
0x3B0C	FREX CTRL 07	0x00	RW	Bit[4:0]: shutter_dly[12:8] MSB of shutter delay in mode 2. Shutter delay is in units of 128 clock cycles. See register **0x3B0D**.
0x3B0D	FREX CTRL 08	0x00	RW	Bit[7:0]: shutter_dly[7:0] LSB of shutter delay in mode 2. Shutter delay is in units of 128 clock cycles. See register **0x3B0C**.
0x3B0E	FREX CTRL 09	0x01	RW	Bit[7:0]: frex_pchg_width[15:8] MSB of sensor precharge in mode 2. Sensor precharge is in units of 1 system clock cycle (see **section 2.12.1**). See register **0x3B0F**.
0x3B0F	FREX CTRL 0A	0x00	RW	Bit[7:0]: frex_pchg_width[7:0] LSB of sensor precharge in mode 2. Sensor precharge is in units of 1 system clock cycle (see **section 2.12.1**). See register **0x3B0E**.
0x3B10	FREX CTRL 0B	0x00	RW	Bit[7:0]: datout_dly[15:8] MSB of readout delay time in mode 2. Readout delay time is in units of 128 clock cycles. See register **0x3B11**.
0x3B11	FREX CTRL 0C	0x00	RW	Bit[7:0]: datout_dly[7:0] LSB of readout delay time in mode 2. Readout delay time is in units of 128 clock cycles. See register **0x3B10**.
0x3B1F	FREX CTRL 0D	0x04	RW	Bit[6]: frex_sccb_req_repeat Bit[5]: frex_strobe_out_sel Bit[4]: frex_nopchg Bit[3]: frex_strobe_pol 0: Active high 1: Active low Bit[2]: frex_shutter_pol Bit[1]: frex_sel 0: Internal FREX 1: External FREX Bit[0]: no_latch
0x3B20	FREX CTRL 0E	0x00	RW	Bit[0]: frex_repeat_trig

4.10.2.1 exposure time control

Registers: r_frame_exp = {0x3B05, 0x3B06, 0x3B07}, 24 bits, 1 step = 128 clock cycles.

Minimum exposure time: 0x3B05 = 0x00, 0x3B06 = 0x00, 0x3B07 = 0x00.
If OV8825 works at 96 MHz, the minimum exposure time is 0 and minimum step is 1.33 s.

Maximum exposure time: 0x3B05 = 0xFF, 0x3B06 = 0xFF, 0x3B07 = 0xFF.
If OV8825 works at 96 MHz, the maximum exposure time is 22.37 sec.

4.10.2.2 shutter delay control

Registers: r_shutter_dly = {0x3B0C[4:0], 0x3B0D[7:0]}, 13 bits, 1 step = 128 clock cycles.

Minimum shutter delay time: 0x3B0C = 0x00, 0x3B0D = 0x00.

Minimum step is 1.33 µs.

Maximum shutter delay time: 0x3B0C = 0x1F, 0x3B0D = 0xFF.
If OV8825 works at 96 MHz, the maximum shutter delay time is 10.92 ms.

4.10.2.3 sensor precharge control

Registers: r_frex_pchg = {0x3B0E[7:0], 0x3B0F[7:0]}, 16 bits, 1 step = 1 system clock cycle (refer to PLL section).

These registers affect sensor performance. It is for internal use and not recommended for customer to change. Time requirement? 10 µs, for example.

4.10.2.4 strobe control

Registers: r_strobe_width = {0x3B09[3:0], 0x3B0A[7:0], 0x3B0B[7:0]}, 20 bits, 1 step = 1 clock cycle.

These registers control the strobe signal output width.

5 image sensor processor digital functions

5.1 ISP general controls

The ISP module provides image processor functions, including lens correction and defect pixel cancellation. These functions are enabled by registers 0x5000, 0x5001, 0x5003, 0x5005, 0x501F, 0x5025, and 0x5041.

table 5-1 ISP general control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x86	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable
0x5001	MWB_GAIN_ CLOCK_ENABLE	0x01	RW	Bit[0]: MWB gain clock enable 0: Disable clock 1: Enable clock
0x5002	NOT USED	–	–	Not Used
0x5003	ISP CTRL03	0x20	RW	Bit[5]: Buffer control enable Must be enabled if DPC or binning filter is used. 0: Disable 1: Enable
0x5005	ISP CTRL05	0xDC	RW	Bit[7:5]: Not used Bit[4]: MWB bias ON 0: Disable 1: Enable Bit[3]: LENC bias plus 0: Disable 1: Enable Bit[2]: LENC bias ON 0: Disable 1: Enable Bit[1:0]: Not used
0x501F	ISP CTRL1F	0x00	RW	Bit[7:6]: Not used Bit[5]: Bypass ISP 0: Disable 1: Enable Bit[4:0]: Debug mode

table 5-1 ISP general control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5025	ISP CTRL 25	0x10	RW	Bit[1:0]: avg_sel 00: raw_i 01: LENC 10: mwb_gain
0x503D	ISP CTRL 3D	0x08	RW	Bit[7:0]: Debug mode
0x503E	ISP CTRL 3E	0x00	RW	Bit[7:0]: Debug mode
0x503F	ISP CTRL 3F	0x20	RW	Bit[7:0]: Debug mode
0x5041	ISP CTRL 41	0x0C	RW	Bit[7]: Manual scaling select 0: Disable 1: Enable Bit[6]: Not used Bit[5]: Scaling enable 0: Disable 1: Enable Bit[4]: Post binning filter enable 0: Disable 1: Enable Bit[3]: Not used Bit[2]: Average enable 0: Disable 1: Enable Bit[1:0]: Not used
0x5042	NOT USED	–	–	Not Used
0x5043	ISP CTRL 43	0x08	RW	Bit[7:0]: Debug mode
0x5044	ISP CTRL 44	0x00	RW	Bit[7:0]: Debug mode
0x5045	ISP CTRL45	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Not used
0x5046	ISP CTRL46	0x00	RW	Bit[7:0]: Debug mode
0x5047	ISP CTRL47	0x00	RW	Bit[7:0]: Debug mode
0x5048	ISP CTRL48	0x10	RW	Bit[7:0]: Debug mode
0x5049	ISP CTRL49	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Debug mode
0x504A	ISP CTRL 4A	0x00	RW	Bit[7:0]: Debug mode
0x504B	ISP CTRL 4B	0x00	RW	Bit[7:0]: Debug mode
0x504C	ISP CTRL 4C	0x00	RW	Bit[7:0]: Debug mode
0x504D	ISP CTRL 4D	0x00	RW	Bit[7:0]: Debug mode

5.2 LENC

The lens correction (LENC) algorithm compensates for the illumination drop off in the corners due to the lens. Based on the radius of each pixel to the lens, the algorithm calculates a gain for each pixel and then corrects each pixel with the calculated gain to compensate for the light distribution due to the lens curvature. Additionally, LENC supports subsampling in both the horizontal and vertical directions. LENC is performed in the RGB domain.

Luminance channel consists of 36 control points while each color channel consists of 25 control points.

figure 5-1 control points of luminance and color channels

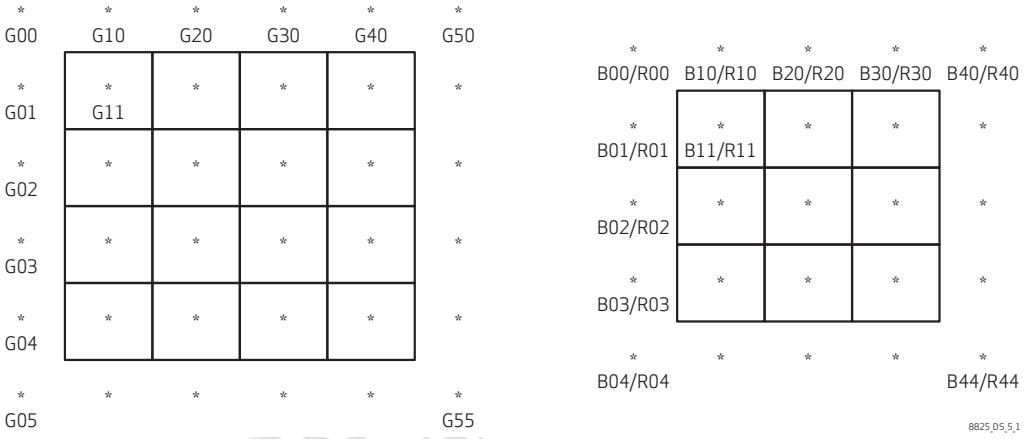
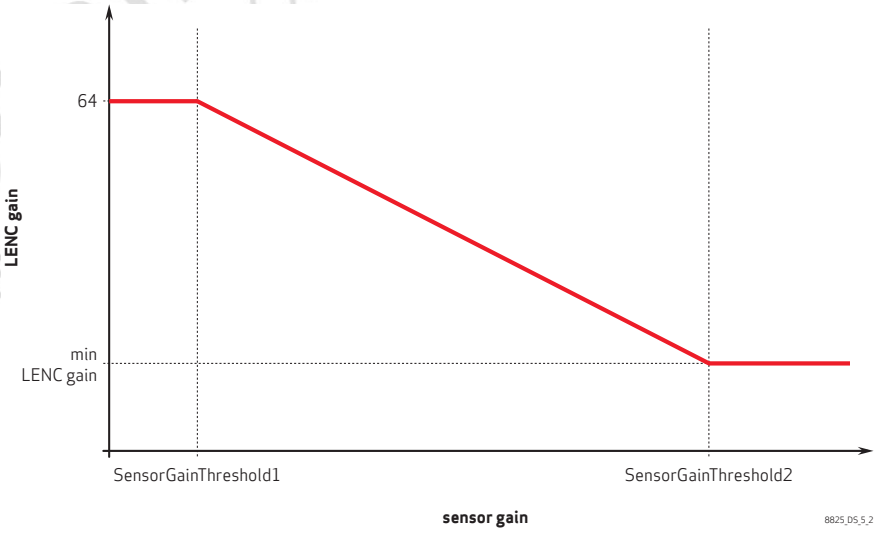


figure 5-2 luminance compensation level calculation



note
There is a lens calibration tool that can be used for calibrating these settings required for a specific module. Contact your local OmniVision FAE for generating these settings.

table 5-2 LENC control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x86	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable
0x5800	LENC G00	0x00	RW	Bit[5:0]: Control point G00 for luminance compensation
0x5801	LENC G01	0x00	RW	Bit[5:0]: Control point G01 for luminance compensation
0x5802	LENC G02	0x00	RW	Bit[5:0]: Control point G02 for luminance compensation
0x5803	LENC G03	0x00	RW	Bit[5:0]: Control point G03 for luminance compensation
0x5804	LENC G04	0x00	RW	Bit[5:0]: Control point G04 for luminance compensation
0x5805	LENC G05	0x00	RW	Bit[5:0]: Control point G05 for luminance compensation
0x5806	LENC G10	0x00	RW	Bit[5:0]: Control point G10 for luminance compensation
0x5807	LENC G11	0x00	RW	Bit[5:0]: Control point G11 for luminance compensation
0x5808	LENC G12	0x00	RW	Bit[5:0]: Control point G12 for luminance compensation
0x5809~ 0x5822	LENC G13~ LENC G54	0x00	RW	Bit[5:0]: Control point G13~G54 for luminance compensation
0x5823	LENC G55	0x00	RW	Bit[5:0]: Control point G55 for luminance compensation
0x5824	LENC BR00	0x00	RW	Bit[7:4]: Control point B00 for blue channel compensation Bit[3:0]: Control point R00 for red channel compensation
0x5825	LENC BR01	0x00	RW	Bit[7:4]: Control point B01 for blue channel compensation Bit[3:0]: Control point R01 for red channel compensation
0x5826	LENC BR02	0x00	RW	Bit[7:4]: Control point B02 for blue channel compensation Bit[3:0]: Control point R02 for red channel compensation

table 5-2 LENC control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5827	LENC BR03	0x00	RW	Bit[7:4]: Control point B03 for blue channel compensation Bit[3:0]: Control point R03 for red channel compensation
0x5828	LENC BR04	0x00	RW	Bit[7:4]: Control point B04 for blue channel compensation Bit[3:0]: Control point R04 for red channel compensation
0x5829~ 0x583C	LENC BR10~ LENC BR44	0x00	RW	Bit[7:4]: Control point B10~B44 for blue channels compensation Bit[3:0]: Control point R10~R44 for red channels compensation
0x583D	LENC BROFFSET	0x88	RW	Bit[7:4]: Base value for all blue channel control points Bit[3:0]: Base value for all red channel control points
0x583E	LENC SENSORGAIN THRESHOLD1	0x40	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will be the minimum value (min LENC gain). Register value is 16 times sensor gain.
0x583F	LENC SENSORGAIN THRESHOLD2	0x20	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will start to decrease; otherwise, the amplitude will not change. Register value is 16 times sensor gain.
0x5840	MIN LENC GAIN	0x18	RW	Bit[6:0]: This value indicates the minimum amplitude which luminance channel compensates when AutoLensSwitchEnable is true. Value should be in the range [0~64]

table 5-2 LENC control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5841	LENC CTRL	0x00	RW	Bit[3]: Add BLC target 0: Do not add BLC target after applying compensation 1: Add BLC target after applying compensation Bit[2]: Subtract BLC target 0: Do not subtract BLC target after applying compensation 1: Subtract BLC target after applying compensation Bit[1]: Reserved Bit[0]: AutoLensSwitchEnable 0: Luminance compensation amplitude does not change with sensor gain 1: Luminance compensation amplitude changes with sensor gain
0x5842	LENC BRHSCALE	0x00	RW	For horizontal color gain calculation, this value indicates the step between two connected horizontal pixels. BRHScale = 3145728 / ImageWidth Bit[2:0]: br_Hscale[10:8]
0x5843	LENC BRHSCALE	0x00	RW	Bit[7:0]: br_Hscale[7:0]
0x5844	LENC BRVSCALE	0x00	RW	For vertical color gain calculation, this value indicates the step between two connected vertical pixels. BRVScale = 3145728 / ImageHeight Bit[2:0]: br_Vscale[10:8]
0x5845	LENC BRVSCALE	0x00	RW	Bit[7:0]: br_Vscale[7:0]
0x5846	LENC GHSCALE	0x00	RW	For horizontal luminance gain calculation, this value indicates the step between two connected horizontal pixels. GHScale = 4194304 / ImageWidth Bit[2:0]: g_Hscale[10:8]
0x5847	LENC GHSCALE	0x00	RW	Bit[7:0]: g_Hscale[7:0]
0x5848	LENC GVSCALE	0x00	RW	For vertical luminance gain calculation, this value indicates the step between two connected horizontal pixels. GVScale = 4194304 / ImageHeight Bit[2:0]: g_Vscale[10:8]
0x5849	LENC GVSCALE	0x00	RW	Bit[7:0]: g_Vscale[7:0]

5.3 defect pixel cancellation (DPC)

Primarily due to process anomalies, pixel defects in the sensor array will occur, generating incorrect pixel levels and color values. The purpose of defect pixel cancellation (DPC) is to remove the effects caused by defective pixels. To correctly remove defective pixels the proper threshold should first be determined.

Defective pixels usually exhibit an abrupt change compared to normal pixels to which the human eye is sensitive. The DPC algorithm is designed to recover these white or black pixels while maintaining image quality. As the position of these defective pixels is not registered, the DPC algorithm may remove some of the image details.

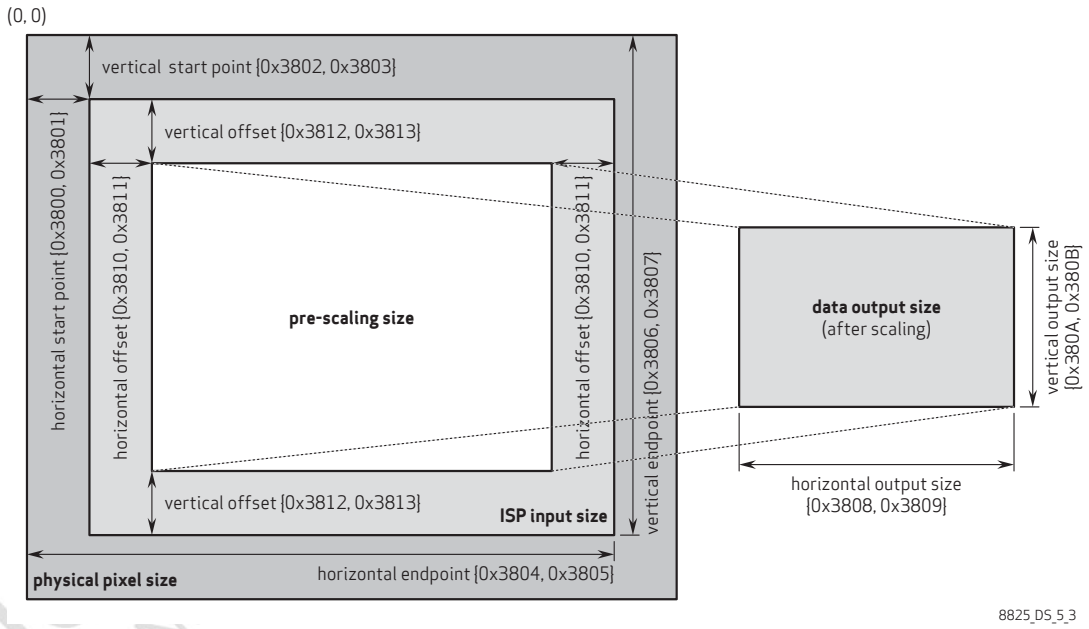
table 5-3 DPC register

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x86	RW	Bit[2]: Remove black defect pixel 0: Disable 1: Enable Bit[1]: Remove white defect pixel 0: Disable 1: Enable

5.4 scalar

The OV8825 includes a scalar function that allows the user to arbitrarily set an output image size (width and height) that is smaller than the designated array size. The scalar module outputs the specified image size and maintains the field-of-view as the input image to the scalar. Note that the frame rate will not change in scaling mode.

figure 5-3 scaling function



1. The scaling function is automatic enable and disable. The user only needs to set the image input size, output size and offset. If the output size < (input size – 2 × offset), scaling is enabled; otherwise, scaling is disabled. To disable the scaling function manually, set register 0x5041[7] to 0.

   Horizontal output size: {0x3808, 0x3809}

   Vertical output size: {0x380A, 0x380B}

   Horizontal offset: {0x3810, 0x3811}

   Vertical offset: {0x3812, 0x3813}

   Horizontal input size: Horizontal endpoint {0x3804, 0x3805} – Horizontal start point {0x3800, 0x3801}

   Vertical input size: Vertical endpoint {0x3806, 0x3807} – Vertical start point {0x3802, 0x3803}

2. Calculate the scaling factor ((input_size – 2 × offset) / output_size) × 128

   Based on the scaling factor, get hscale_ctrl and vscale_ctrl from **table 5-4** using the following criteria:

   If scale_factor is located in column factor 1, hscale_ctrl[7:6] or vscale[7:6] = 2'b01.

   If scale_factor is located in column factor 2, hscale_ctrl[7:6] or vscale[7:6] = 2'b01.

   If scale_factor is located in column factor 3, hscale_ctrl[7:6] or vscale[7:6] = 2'b01.

If both hscale_factor and vscale_factor are the same, hscale_ctrl[4:0] = scale_ctrl0 and vscale_ctrl[4:0] = scale_ctrl1.
If hscale_factor and vscale_factor are different, use column scale_ctrl1.

For example, hscale_factor = 400, vscale_factor = 400
hscale_ctrl[7:6] = 2'b01, hscale_ctrl[4:0] = 0x14
vscale_ctrl[7:6] = 2'b01, vscale_ctrl[4:0] = 0x15

table 5-4 scalar factor calculation matrix (sheet 1 of 2)

factor1	factor2	factor3	scale_ctrl0	scale_ctrl1
129-134	265-268	529-537	0x1F	0x1F
135-136	269-273	538-546	0x1E	0x1F
137-139	274-277	547-555	0x1E	0x1E
140-141	278-282	556-565	0x1D	0x1E
142-143	283-287	566-574	0x1D	0x1D
144-146	288-292	575-585	0x1C	0x1D
147-149	293-298	586-596	0x1C	0x1C
150-151	299-303	597-606	0x1B	0x1C
152-154	304-309	607-618	0x1B	0x1B
155-157	310-315	619-630	0x1A	0x1B
158-160	316-321	631-642	0x1A	0x1A
161-163	322-327	643-655	0x19	0x1A
164-167	328-334	656-669	0x19	0x19
168-170	335-341	670-682	0x18	0x19
171-174	342-348	683-697	0x18	0x18
175-178	349-356	698-712	0x17	0x18
179-182	357-364	713-728	0x17	0x17
183-186	365-372	729-744	0x16	0x17
187-190	373-381	745-762	0x16	0x16
191-195	382-390	763-780	0x15	0x16
196-199	391-399	781-799	0x15	0x15
200-204	400-409	800-819	0x14	0x15
205-210	410-420	820-840	0x14	0x14
211-215	421-431	841-862	0x13	0x14
216-221	432-443	863-885	0x13	0x13

table 5-4 scalar factor calculation matrix (sheet 2 of 2)

factor1	factor2	factor3	scale_ctrl0	scale_ctrl1
222-227	444-455	886-910	0x12	0x13
228-234	456-468	911-935	0x12	0x12
235-240	469-481	936-963	0x11	0x12
241-248	482-496	964-992	0x11	0x11
249-255	497-511	993-1023	0x10	0x11
256-263	512-528	1024	0x10	0x10

table 5-5 scalar control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5041	ISP CTRL41	0x04	RW	Bit[7]: Manual scaling select 0: Disable, scaling is auto enabled when the output size is less than the input size 1: Enable, scaling is manually enabled or disabled depending on register 0x5041[5] Bit[5]: Manual scaling enable 0: Scaling disable 1: Scaling enable
0x5068	HSCALE_CTRL	0x00	RW	Bit[7:6]: Horizontal scaling control (see formula) Bit[5]: Not used Bit[4:0]: scale_ctrl0
0x506A	VSCALE_CTRL	0x00	RW	Bit[7:0]: Vertical scaling control (see formula) Bit[5]: Not used Bit[4:0]: scale_ctrl1
0x3800	TIMING HS	0x00	RW	Bit[7:4]: Not used Bit[3:0]: HREF horizontal start point[11:8]
0x3801	TIMING HS	0x00	RW	Bit[7:0]: HREF horizontal start point[7:0]
0x3802	TIMING VS	0x00	RW	Bit[7:4]: Not used Bit[3:0]: HREF vertical start point[11:8]
0x3803	TIMING VS	0x00	RW	Bit[7:0]: HREF vertical start point[7:0]
0x3804	TIMING HW	0x00	RW	Bit[7:4]: Not used Bit[3:0]: HREF horizontal endpoint[11:8]
0x3805	TIMING HW	0xDF	RW	Bit[7:0]: HREF horizontal endpoint[7:0]
0x3806	TIMING VH	0x00	RW	Bit[7:4]: Not used Bit[3:0]: HREF vertical endpoint[11:8]

table 5-5 scalar control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3807	TIMING VH	0x9B	RW	Bit[7:0]: HREF vertical endpoint[7:0]
0x3808	TIMING ISPHO	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ISP output horizontal width[11:8]
0x3809	TIMING ISPHO	0xC0	RW	Bit[7:0]: ISP output horizontal width[7:0]
0x380A	TIMING ISPVO	0x00	RW	Bit[7:4]: Not used Bit[3:0]: ISP output vertical width[11:8]
0x380B	TIMING ISPVO	0x90	RW	Bit[7:0]: ISP output vertical width[7:0]
0x3810	TIMING HOFFS HIGH	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Horizontal offset[11:8]
0x3811	TIMING HOFFS LOW	0x10	RW	Bit[7:0]: Horizontal offset[7:0]
0x3812	TIMING VOFFS HIGH	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Vertical offset[11:8]
0x3813	TIMING VOFFS LOW	0x10	RW	Bit[7:0]: Vertical offset[7:0]

5.5 MWB

The manual white balance (MWB) provides digital gain for R, G, and B channels. Each channel gain is 12-bit. 0x400 is 1x gain.

table 5-6 MWB control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3400	MWB GAIN00	0x04	RW	Bit[3:0]: MWB red gain[11:8] Digital gain in red channel Red gain = MWB red gain[11:0] / 0x400
0x3401	MWB GAIN01	0x00	RW	Bit[7:0]: MWB red gain[7:0] Digital gain in red channel Red gain = MWB red gain[11:0] / 0x400
0x3402	MWB GAIN02	0x04	RW	Bit[3:0]: MWB green gain[11:8] Digital gain in green channel Green gain = MWB green gain[11:0] / 0x400
0x3403	MWB GAIN03	0x00	RW	Bit[7:0]: MWB green gain[7:0] Digital gain in green channel Green gain = MWB green gain[11:0] / 0x400

table 5-6 MWB control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3404	MWB GAIN04	0x04	RW	Bit[3:0]: MWB blue gain[11:8] Digital gain in blue channel Blue gain = MWB blue gain[11:0] / 0x400
0x3405	MWB GAIN05	0x00	RW	Bit[7:0]: MWB blue gain[7:0] Digital gain in blue channel Blue gain = MWB blue gain[11:0] / 0x400
0x3406	MWB GAIN06	0x00	RW	Bit[0]: MWB gain enable 0: Disable 1: Enable

5.6 gain and exposure control

The OV8825 does not support auto exposure control (AEC) or auto gain control (AGC). Both exposure time and gain should be set manually from external control. The related registers are listed in **table 5-7**. The exposure values in registers 0x3500~0x3502 are in units of 1/16th of a line. The gain value in registers 0x350A~0x350B support a maximum of 16x analog gain. Best performance is achieved using sensor gain (register 0x3509[4]=0).

table 5-7 gain/exposure control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3500	EXPO	0x00	RW	Bit[3:0]: Expo[19:16]
0x3501	EXPO	0x02	RW	Bit[7:0]: Expo[15:8]
0x3502	EXPO	0x00	RW	Bit[7:0]: Expo[7:0] Low 4 bits are fraction bits which are not supported and should always be 0.
0x3503	R MANUAL	0x00	RW	Bit[5]: Gain delay option 0: 1 frame latch 1: Delay 1 frame latch Bit[4]: Choose delay option 0: Delay disable 1: Delay enable Bit[2]: gain_man_as_gain_snr 0: Manual gain is real gain 1: Manual gain is sensor gain Bit[1:0]: Debug mode

table 5-7 gain/exposure control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3509	AEC09	0x10	RW	AEC Manual Mode Control Bit[7:5]: Not used Bit[4]: Sensor gain convert enable 0: Use sensor gain, {0x350A, 0x350B} is sensor gain, 0x00 is 1x gain 1: Use real gain, {0x350A, 0x350B} is real gain, 0x10 is 1x gain Bit[3]: Gain manual enable 0: Manual disable, use register 0x350A/0x350B 1: Manual enable, use register 0x3504/0x3505 Bit[2:0]: Not used
0x350A	AEC AGC ADJ	0x00	RW	Gain Output to Sensor Bit[7:3]: Not used Bit[0]: Gain[10:8]
0x350B	AEC AGC ADJ	0x10	RW	Gain Output to Sensor Bit[7:0]: Gain[7:0] When 0x3509[4] = 0, this gain is sensor gain. Real gain = 2^n(16+x)/16, where N is the number of 1 in bits[9:4] and X is the low bits[3:0]. When 0x3509[4] = 1, this gain is real gain. The low 4 bits are fraction bits. Note: Real gain is non-continuous

5.7 average (AVG)

The main function of AVG is to average the data channel value using special filters.

table 5-8 AVG control registers

address	register name	default value	R/W	description
0x5041	ISP CTRL41	0x04	RW	Bit[2]: Average enable 0: Disable 1: Enable
0x5680	AVG CTRL00	0x00	RW	Bit[4:0]: X start offset[12:8]
0x5681	AVG CTRL01	0x00	RW	Bit[7:0]: X start offset[7:0]
0x5682	AVG CTRL02	0x00	RW	Bit[3:0]: Y start offset[11:8]
0x5683	AVG CTRL03	0x00	RW	Bit[7:0]: Y start offset[7:0]
0x5684	AVG CTRL04	0x10	RW	Bit[4:0]: Window width[12:8]
0x5685	AVG CTRL05	0xA0	RW	Bit[7:0]: Window width[7:0]
0x5686	AVG CTRL06	0x0C	RW	Bit[3:0]: Window height[11:8]
0x5687	AVG CTRL07	0x78	RW	Bit[7:0]: Window height[7:0]
0x5688	AVG CTRL08	0x02	RW	Bit[0]: Average size manual 0: Disable, use ISP pre-scale 1: Enable, use registers 0x5680~0x5687

6 system control

System control registers include clock, reset control, and PLL configure. Individual modules can be reset or clock gated by setting the appropriate registers (see **table 6-1**).

table 6-1 system control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x0100	MODE_SELECT	0x00	RW	Bit[7:1]: Not used Bit[0]: Streaming setting 0: software_standby 1: Streaming
0x0103	SOFTWARE_RST	0x00	RW	Bit[7:1]: Not used Bit[0]: software_reset
0x3000	PAD_OEN2	0x00	RW	Bit[4]: io_strobe_oen Bit[3]: io_sda_oen Bit[2]: io_frex_oen Bit[1]: io_vsync_oen Bit[0]: io_shutter_oen
0x3002	SCCB_ID	0x6C	RW	Bit[7:0]: sccb_id
0x3003	PLL_CTRL0	0x8E	RW	PLL1 Control Bit[7:6]: DivB[1:0] 00: /1 01: /1 10: /2 11: /4 Bit[5:3]: Debug mode Bit[2:0]: PreDiv[2:0] 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x3004	PLL_CTRL1	0x04	RW	PLL1 Control Bit[7]: sclk_dac 0: Sysclk from PLL1 1: Sysclk from PLL2 Bit[6:0]: DivP[6:0] 129 – DivP[6:0]
0x3005	PLL_CTRL2	0x10	RW	PLL1 Control Bit[7:4]: DivM[3:0] DivM[3:0] + 1 Bit[3:0]: DivS[3:0] DivS[3:0] + 1

table 6-1 system control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x3006	PLL_CTRL3	0x70	RW	PLL1 Control Bit[7]: R_divp 0: /8 1: /10 Bit[6:4]: R_seld5 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /3.5 110: /4 111: /5 Bit[3:0]: Sdiv1[3:0] Sdiv[3:0] + 1
0x3007	PLL_CTRL4	0x3B	RW	PLL2 Control Bit[7:3]: divp_sp[4:0] 32 – divp_sp[4:0] Bit[2]: Div_sp 0: /1 1: /2 Bit[1:0]: PreDiv 00: /1 01: /1.5 10: /2 11: /3
0x3008~ 0x3009	NOT USED	–	–	Not Used
0x300A	CHIP ID HIGH BYTE	0x88	R	Chip ID High Byte
0x300B	CHIP ID MIDDLE BYTE	0x20	R	Chip ID Middle Byte
0x300C	CHIP ID LOW BYTE	0x00	R	Chip ID Low Byte
0x302A	SENSOR REVISION	–	R	Bit[7:0]: Sensor revision control 0xB0: Rev 1A 0xB1: Rev 1B 0xB2: Rev 1C
0x300D	SC_PAD_OUT2	0x00	RW	Bit[4]: io_stobe_o Bit[3]: io_sda_o Bit[2]: io_frex_o Bit[1]: io_vsync Bit[0]: io_shutter_o
0x300E	SC_PAD_SEL0	0x00	RW	Bit[3:0]: bypass_ctrl
0x300F	SC_PAD_SEL1	0x00	RW	Bit[5:0]: bypass_sel

table 6-1 system control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x3010	SC_PAD_SEL2	0x00	RW	Bit[4]: io_strobe_sel Bit[3]: io_sda_sel Bit[2]: io_frex_sel Bit[1]: io_vsync_sel Bit[0]: io_shutter_sel
0x3011	SC_PLL_CTRL_S2	0x02	RW	Bit[2]: mipi_bit8 Bit[1:0]: mipi_lane_sel 00: 1 lane 01: 2 lane 10: 4 lane
0x3012	SC_PLL_CTRL_S1	0x80	RW	PLL1 Control Bit[7:6]: Div124_sp[1:0] 00: /1 01: /1 10: /2 11: /4 Bit[5:4]: Div12_sp[1:0] 00: /1 01: /1 10: /2 11: /2.5 Bit[3:0]: Divs_sp[3:0] Divs_sp[3:0] + 1
0x3013	SC_PLL_CTRL_S0	0x39	RW	Bit[7]: Debug mode Bit[6:3]: Div_dac[3:0] Div_dac[3:0] + 1 Bit[2:0]: Debug mode
0x3014~ 0x3017	NOT USED	–	–	Not Used
0x3018	SC_MIPI_SC_CTRL	0x18	RW	Bit[7:5]: Not used Bit[4]: r_phy_pd_mipi 0: Not used 1: Power down PHY HS TX Bit[3]: r_phy_pd_lprx 0: Not used 1: Power down PHY LP RX module Bit[3:0]: Not used
0x3019	NOT USED	–	–	Not Used

table 6-1 system control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x301A	SC_CLKRST0	0x1A	RW	Bit[7]: Not used Bit[6]: sclk_stb Bit[5]: sclk_aec Bit[4]: sclk_tc Bit[3]: mipi_phy_rst_o Bit[2]: rst_stb Bit[1]: rst_aec Bit[0]: rst_tc
0x301B	SC_CLKRST1	0xF0	RW	Bit[7]: sclk_blc Bit[6]: sclk_isp Bit[5]: sclk_avg Bit[4]: Not used Bit[3]: rst_blc Bit[2]: rst_isp Bit[1]: rst_avg Bit[0]: Not used
0x301C	SC_CLKRST2	0xF0	RW	Bit[7]: Not used Bit[6]: sclk_mipi Bit[5]: sclk_mwb_pk Bit[4]: sclk_otp Bit[3]: Not used Bit[2]: rst_mipi Bit[1]: rst_mwb_pk Bit[0]: rst_otp
0x301D	SC_CLKRST3	0xB4	RW	Bit[7]: sclk_asram_tst Bit[6]: padclk_srb Bit[5]: sclk_bist Bit[4]: sclk_ac Bit[3]: rst_asram_tst Bit[2]: rst_srb Bit[1]: rst_bist Bit[0]: rst_ac
0x301E	SC_CLKRST4	0xF1	RW	Bit[7:5]: Not used Bit[4]: pclk_mipi Bit[3:1]: Not used Bit[0]: daclk_o
0x301F	SC_FREX_RST_MASK0	0x09	RW	Bit[7]: frex_mask_aec Bit[6]: frex_mask_blc Bit[5]: frex_mask_isp Bit[4]: frex_mask_dvp Bit[3]: frex_mask_mipi Bit[2]: Not used Bit[1]: frex_mask_avg Bit[0]: frex_mask_mipi_phy

table 6-1 system control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x3020	SC_CLOCK_SEL	0x01	RW	Bit[7]: Debug mode Bit[6:5]: Not used Bit[4]: dvp_sclk_en 0: Not used 1: Use pll_sclk_i instead of pll_pclk_i for DVP Bit[3]: pclk_sel Bit[2:1]: sclk_sel Bit[0]: Not used
0x3021	SC_MISC_CTRL	0x03	RW	Bit[7:6]: Not used Bit[5]: dac_sclk_en Bit[4:1]: Not used Bit[0]: cen_global_o
0x3022	SC_SRAM_TST	0x00	RW	sc_sram_tst
0x3023	SC_SRAM_VAL0	0xFF	RW	sc_sram_val0
0x3024	SC_SRAM_VAL1	0x09	RW	sc_sram_val1

6.1 mobile industry processor interface (MIPI)

MIPI provides a single uni-directional clock lane and one, two, and four uni-directional data lanes to communicate to components in a mobile device. Each data lane has full support for high speed (HS) data transfer mode. Contact your local OmniVision FAE for more details.

table 6-2 MIPI registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4800	MIPI CTRL00	0x04	RW	Bit[5]: Clock lane gate enable 0: Clock lane is free running 1: Gate clock lane when no packet to transmit Bit[4]: Line sync enable 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Lane select 0: Use lane1 as default data lane 1: Use lane2 as default data lane

table 6-2 MIPI registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4801	MIPI CTRL01	0x03	RW	Bit[7]: Long packet data type manual enable 0: Use MIPI data 1: Use dt man o as long packet data Bit[4]: PH bit order for ECC 0: (DI[7:0],WC[7:0],WC[15:8]) 1: (DI[0:7],WC[0:7],WC[8:15]) Bit[3]: PH byte order for ECC 0: (DI,WC L,WC H) 1: (DI,WC H,WC L) Bit[2]: PH byte order2 for ECC 0: (DI,WC) 1: (WC,DI)
0x4837	PCLK PERIOD	0x15	RW	Bit[7:0]: Period of pclk2x, pclk_div = 1, and 1-bit decimal

7 register tables

The following tables provide descriptions of the device control registers contained in the OV8825. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x6C for write and 0x6D for read.

7.1 system control [0x0100 - 0x0103, 0x3000 - 0x302A]

table 7-1 system control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x0100	MODE_SELECT	0x00	RW	Bit[7:1]: Not used Bit[0]: Streaming setting 0: software_standby 1: Streaming
0x0103	SOFTWARE_RST	0x00	RW	Bit[7:1]: Not used Bit[0]: software_reset
0x3000	PAD_OEN2	0x00	RW	Bit[7:5]: Not used Bit[4]: io_strobe_oen Bit[3]: io_sda_oen Bit[2]: io_frex_oen Bit[1]: io_vsync_oen Bit[0]: io_shutter_oen
0x3001	NOT USED	–	–	Not Used
0x3002	SCCB_ID	0x6C	RW	Bit[7:0]: sccb_id
0x3003	PLL_CTRL0	0x8E	RW	PLL1 Control Bit[7:6]: DivB[1:0] 00: /1 01: /1 10: /2 11: /4 Bit[5:3]: Debug mode Bit[2:0]: PreDiv[2:0] 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x3004	PLL_CTRL1	0x04	RW	PLL1 Control Bit[7]: sclk_dac 0: Sysclk from PLL1 1: Sysclk from PLL2 Bit[6:0]: DivP[6:0] 129 – DivP[6:0]

table 7-1 system control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x3005	PLL_CTRL2	0x10	RW	PLL1 Control Bit[7:4]: DivM[3:0] DivM[3:0] + 1 Bit[3:0]: DivS[3:0] DivS[3:0] + 1
0x3006	PLL_CTRL3	0x70	RW	PLL1 Control Bit[7]: R_divp 0: /8 1: /10 Bit[6:4]: R_seld5 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /3.5 110: /4 111: /5 Bit[3:0]: Sdiv1[3:0] Sdiv[3:0] + 1
0x3007	PLL_CTRL4	0x3B	RW	PLL2 Control Bit[7:3]: divp_sp[4:0] 32 – divp_sp[4:0] Bit[2]: Div_sp 0: /1 1: /2 Bit[1:0]: PreDiv 00: /1 01: /1.5 10: /2 11: /3
0x3008~ 0x3009	NOT USED	–	–	Not Used
0x300A	CHIP ID HIGH BYTE	0x88	R	Chip ID High Byte
0x300B	CHIP ID MIDDLE BYTE	0x25	R	Chip ID Middle Byte
0x300C	CHIP ID LOW BYTE	0x00	R	Chip ID Low Byte
0x300D	SC_PAD_OUT2	0x00	RW	Bit[7:5]: Not used Bit[4]: io_stobe_o Bit[3]: io_sda_o Bit[2]: io_frex_o Bit[1]: io_vsync Bit[0]: io_shutter_o
0x300E	SC_PAD_SEL0	0x00	RW	Bit[7:4]: Not used Bit[3:0]: bypass_ctrl

table 7-1 system control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x300F	SC_PAD_SEL1	0x00	RW	Bit[7:6]: Not used Bit[5:0]: bypass_sel
0x3010	SC_PAD_SEL2	0x00	RW	Bit[7:5]: Not used Bit[4]: io_strobe_sel Bit[3]: io_sda_sel Bit[2]: io_frex_sel Bit[1]: io_vsync_sel Bit[0]: io_shutter_sel
0x3011	SC_PLL_CTRL_S2	0x02	RW	Bit[7:3]: Not used Bit[2]: mipi_bit8 Bit[1:0]: mipi_lane_sel 00: 1 lane 01: 2 lane 10: 4 lane
0x3012	SC_PLL_CTRL_S0	0x80	RW	PLL1 Control Bit[7:6]: Div124_sp[1:0] 00: /1 01: /1 10: /2 11: /4 Bit[5:4]: Div12_sp[1:0] 00: /1 01: /1 10: /2 11: /2.5 Bit[3:0]: Divs_sp[3:0] Divs_sp[3:0] + 1
0x3013	SC_PLL_CTRL_S1	0x39	RW	Bit[7]: Debug mode Bit[6:3]: Div_dac[3:0] Div_dac[3:0] + 1 Bit[2:0]: Debug mode
0x3014~ 0x3017	NOT USED	–	–	Not Used
0x3018	SC_MIPI_SC_CTRL	0x18	RW	Bit[7:5]: Not used Bit[4]: r_phy_pd_mipi 0: Not used 1: Power down PHY HS TX Bit[3]: r_phy_pd_lprx 0: Not used 1: Power down PHY LP RX module Bit[3:0]: Not used
0x3019	NOT USED	–	–	Not Used

table 7-1 system control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x301A	SC_CLKRST0	0x70	RW	Bit[7]: Not used Bit[6]: sclk_stb Bit[5]: sclk_aec Bit[4]: sclk_tc Bit[3]: mipi_phy_rst_o Bit[2]: rst_stb Bit[1]: rst_aec Bit[0]: rst_tc
0x301B	SC_CLKRST1	0xF0	RW	Bit[7]: sclk_blc Bit[6]: sclk_isp Bit[5]: sclk_avg Bit[4]: Not used Bit[3]: rst_blc Bit[2]: rst_isp Bit[1]: rst_avg Bit[0]: Not used
0x301C	SC_CLKRST2	0xF0	RW	Bit[7]: Not used Bit[6]: sclk_mipi Bit[5]: sclk_mwb_pk Bit[4]: sclk_otp Bit[3]: Not used Bit[2]: rst_mipi Bit[1]: rst_mwb_pk Bit[0]: rst_otp
0x301D	SC_CLKRST3	0xB4	RW	Bit[7]: sclk_asram_tst Bit[6]: padclk_srb Bit[5]: sclk_bist Bit[4]: sclk_ac Bit[3]: rst_asram_tst Bit[2]: rst_srb Bit[1]: rst_bist Bit[0]: rst_ac
0x301E	SC_CLKRST4	0xF1	RW	Bit[7:5]: Not used Bit[4]: pclk_mipi Bit[3:1]: Not used Bit[0]: daclk_o
0x301F	SC_FREX_RST_MASK0	0x09	RW	Bit[7]: frex_mask_aec Bit[6]: frex_mask_blc Bit[5]: frex_mask_isp Bit[4]: frex_mask_dvp Bit[3]: frex_mask_mipi Bit[2]: Not used Bit[1]: frex_mask_avg Bit[0]: frex_mask_mipi_phy

table 7-1 system control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x3020	SC_CLOCK_SEL	0x01	RW	Bit[7]: Debug mode Bit[6:5]: Not used Bit[4]: dvp_sclk_en 0: Not used 1: Use pll_sclk_i instead of pll_pclk_i for DVP Bit[3]: pclk_sel Bit[2:1]: sclk_sel Bit[0]: Not used
0x3021	SC_MISC_CTRL	0x03	RW	Bit[7:6]: Not used Bit[5]: dac_sclk_en Bit[4:1]: Not used Bit[0]: cen_global_o
0x3022	SC_SRAM_TST	0x00	RW	sc_sram_tst
0x3023	SC_SRAM_VAL0	0xFF	RW	sc_sram_val0
0x3024	SC_SRAM_VAL1	0x09	RW	sc_sram_val1
0x302A	SENSOR REVISION	–	R	Bit[7:0]: Sensor revision control 0xB0: Rev 1A 0xB1: Rev 1B 0xB2: Rev 1C

7.2 SCCB control [0x3100 - 0x3106]

table 7-2 SCCB registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3100	SCCB_CTRL0	0x00	RW	Not Used
0x3101	SCCB_CTRL1	0x12	RW	Bit[7:5]: Not used Bit[4]: en_ss_addr_inc Bit[3:0]: Debug mode
0x3102	SCCB_CTRL2	0x00	RW	Bit[7:0]: Debug mode
0x3103	NOT USED	–	–	Not Used

table 7-2 SCCB registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3104	SCCB_PLL	0x20	RW	Bit[7]: Not used Bit[6]: sda_vblank Bit[5]: r_sys_sel (sclk) 0: pll2_daclk 1: pll1_sclk Bit[4]: r_dac_sel (sen_clk) 0: pll2_daclk 1: pll1_sclk Bit[3]: r_daclk (dacclk) 0: pll2_daclk 1: pll1_sclk Bit[2:0]: Debug mode
0x3105	NOT USED	–	–	Not Used
0x3106	SRB_CTRL	0x15	RW	Bit[7:6]: Not used Bit[5:0]: Debug mode

7.3 context switching [0x3200 - 0x320F]

table 7-3 context switching registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3200	GROUP_ADDR0	0x00	RW	grp_group_addr0
0x3201	GROUP_ADDR1	0x10	RW	grp_group_addr1
0x3202	GROUP_ADDR2	0x1F	RW	grp_group_addr2
0x3203	GROUP_ADDR3	0x1F	RW	grp_group_addr3
0x3204	GROUP_LENG0	0x00	RW	grp_group_leng0
0x3205	GROUP_LENG1	0x00	RW	grp_group_leng1
0x3206	GROUP_LENG2	0x00	RW	grp_group_leng2
0x3207	GROUP_LENG3	0x00	RW	grp_group_leng3

table 7-3 context switching registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Bit[[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch Others: Reserved Bit[[3:0]: group_id 0000: Group bank 0, default start from address 0x00 0001: Group bank 1, default start from address 0x40 0010: Group bank 2, default start from address 0x80 0011: Group bank 3, default start from address 0xB0 Others: Reserved
0x3209	GRP0_PERIOD	0x00	RW	Frames For Staying in grp0
0x320A	GRP1_PERIOD	0x00	RW	Frames For Staying in grp1
0x320B	GRP_SWCTRL	0x01	RW	Bit[7:6]: Not used Bit[5]: grp0_start_opt Bit[4]: frame_cnt_trig Bit[3]: group_switch_repeat Bit[2]: context_en Bit[1:0]: Second group selection
0x320C	GRP_SRAM	0x0A	RW	Bit[7:5]: Not used Bit[4]: test_srm Bit[3:0]: sram_rm
0x320D	GRP_ACT	–	R	Indicates Which Group is Active
0x320E	FRAME_CNT_GRP0	–	R	frame_cnt_grp0
0x320F	FRAME_CNT_GRP1	–	R	frame_cnt_grp1

7.4 MWB control [0x3400 - 0x3406]

table 7-4 MWB control registers

address	register name	default value	R/W	description
0x3400	MWB GAIN00	0x04	RW	Bit[7:4]: Not used Bit[3:0]: MWB red gain[11:8] Digital gain in red channel Red gain = MWB red gain[11:0] / 0x400
0x3401	MWB GAIN01	0x00	RW	Bit[7:0]: MWB red gain[7:0] Digital gain in red channel Red gain = MWB red gain[11:0] / 0x400
0x3402	MWB GAIN02	0x04	RW	Bit[7:4]: Not used Bit[3:0]: MWB green gain[11:8] Digital gain in green channel Green gain = MWB green gain[11:0] / 0x400
0x3403	MWB GAIN03	0x00	RW	Bit[7:0]: MWB green gain[7:0] Digital gain in green channel Green gain = MWB green gain[11:0] / 0x400
0x3404	MWB GAIN04	0x04	RW	Bit[7:4]: Not used Bit[3:0]: MWB blue gain[11:8] Digital gain in blue channel Blue gain = MWB blue gain[11:0] / 0x400
0x3405	MWB GAIN05	0x00	RW	Bit[7:0]: MWB blue gain[7:0] Digital gain in blue channel Blue gain = MWB blue gain[11:0] / 0x400
0x3406	MWB GAIN06	0x00	RW	Bit[7:1]: Not used Bit[0]: Manually write MWB gain 0: Auto 1: Manual

7.5 manual AEC/AGC [0x3500 - 0x350F]

table 7-5 manual AEC/AGC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3500	AEC EXPO	0x00	RW	AEC Peak Exposure Bit[7:4]: Not used Bit[3:0]: Exposure[19:16]
0x3501	AEC EXPO	0x00	RW	AEC Peak Exposure Bit[7:0]: Exposure[15:8]
0x3502	AEC EXPO	0x00	RW	AEC Peak Exposure Bit[7:0]: Exposure[7:0] Low 4 bits are fraction bits which are not supported and should always be 0.
0x3503	AEC MANUAL	0x00	RW	AEC Manual Mode Control Bit[7:6]: Not used Bit[5:4]: Gain delay option x0: Gain has no delay 01: Gain delay to next frame 11: Gain delay two frames Bit[3]: Not used Bit[2]: VTS manual enable 0: Auto enable 1: Manual enable Bit[1]: AGC manual enable 0: Auto enable 1: Manual enable Bit[0]: AEC manual enable 0: Auto enable 1: Manual enable
0x3504	MAN GAIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Man gain[9:8]
0x3505	MAN GAIN	0x00	RW	Bit[7:0]: Man gain[7:0]
0x3506	ADD VTS	0x00	RW	Bit[7:0]: Add dummy lines VTS[15:8]
0x3507	ADD VTS	0x00	RW	Bit[7:0]: Add dummy lines VTS[7:0]
0x3508	NOT USED	–	–	Not Used

table 7-5 manual AEC/AGC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3509	AEC09	0x10	RW	AEC Manual Mode Control Bit[7:5]: Not used Bit[4]: Sensor gain convert enable 0: Use sensor gain, {0x350A, 0x350B} is sensor gain, 0x00 is 1x gain 1: Use real gain, {0x350A, 0x350B} is real gain, 0x10 is 1x gain Bit[3]: Gain manual enable 0: Manual disable, use register 0x350A/0x350B 1: Manual enable, use register 0x3504/0x3505 Bit[2:0]: Not used
0x350A	AEC AGC ADJ	0x00	RW	Gain Output to Sensor Bit[7:3]: Not used Bit[0]: Gain[10:8]
0x350B	AEC AGC ADJ	0x10	RW	Gain Output to Sensor Bit[7:0]: Gain[7:0] When 0x3509[4] = 0, this gain is sensor gain. Real gain = 2^n(16+x)/16. N is the number of 1 in bits[9:4]. X is the low bits[3:0]. When 0x3509[4] = 1, this gain is real gain. The low 4 bits are fraction bits. Note: Real gain is non-continuous.
0x350C~ 0x350F	NOT USED	–	–	Not Used

7.6 analog and VCM control [0x3600 - 0x361E]

table 7-6 analog and VCM registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3600	ANACTRL0	0x04	RW	Analog Control Register
0x3601	ANACTRL1	0x15	RW	Analog Control Register
0x3602	ANACTRL2	0x57	RW	Analog Control Register
0x3603	ANACTRL3	0x20	RW	Analog Control Register

table 7-6 analog and VCM registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3604	ANACTRL4	0x90	RW	Analog Control Register
0x3605	ANACTRL5	0x11	RW	Analog Control Register
0x3606	ANACTRL6	0x02	RW	Analog Control Register
0x3607	ANACTRL7	0x02	RW	Analog Control Register
0x3608	ANACTRL8	0x00	RW	Bit[7]: Analog control Bit[6]: bp_regulator Bit[5:0]: Analog control
0x3609	ANACTRL9	0xB8	RW	Analog Control Register
0x360A	ANACTRLA	0x84	RW	Analog Control Register
0x360B	ANACTRLB	0x3C	RW	Analog Control Register
0x360C	ANACTRLC	0x0C	RW	Analog Control Register
0x360D	ANACTRLD	0x00	RW	Analog Control Register
0x360E	ANACTRLE	0x00	RW	Analog Control Register
0x360F	ANACTRLF	0x48	RW	Analog Control Register
0x3610	ANACTRL10	0x00	RW	Analog Control Register
0x3611	ANACTRL11	0x00	RW	Analog Control Register
0x3612	ANACTRL12	0x03	RW	Bit[7]: Analog control Bit[6:5]: Pad I/O drive capability 00: 1x 01: 2x 10: 3x 11: 4x Bit[4:3]: Reserved Bit[2:1]: Not used Bit[0]: Analog control
0x3613	ANACTRL13	0x04	RW	Analog Control Register
0x3614	ANACTRL14	0xFF	RW	Analog Control Register
0x3615	ANACTRL15	0x00	RW	Analog Control Register
0x3616	ANACTRL16	0x03	RW	Analog Control Register
0x3617	ANACTRL17	0x01	RW	Analog Control Register
0x3618	A_VCM_LOW	0x00	RW	Bit[7:4]: din[3:0] Bit[3]: s3 Bit[2:0]: s[2:0]

table 7-6 analog and VCM registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3619	A_VCM_MID0	0x00	RW	Bit[7]: pdin Bit[6]: rv14 Bit[5:0]: din[9:4]
0x361A	A_VCM_MID1	0x00	RW	Bit[7:0]: rdiv[7:0]
0x361B	A_VCM_MID2	0x00	RW	Bit[7]: rmsb_inv 0: Normal 1: Switch **A_VCM_LOW** and **A_VCM_MID0** Bit[6]: rs14 Bit[5]: rs13 Bit[4]: vcm_rih_o Bit[3:0]: rdiv[11:8]
0x361C	A_VCM_HIGH	0x00	RW	Bit[7:3]: Not used Bit[2:0]: VCM output current control 000: 0.71 * Id 001: 0.77 * Id 010: 0.83 * Id 011: 0.91 * Id 100: 1.00 * Id 101: 1.11 * Id 110: 1.25 * Id 111: 1.43 * Id
0x361D	ANACTRL1D	0x00	RW	Analog Control Register
0x361E	ANACTRL1E	0x00	RW	Bit[7]: vsync_polarity 0: VSYNC output is low in active pixel period 1: VSYNC output is high in active pixel period Bit[6:4]: Debug mode Bit[3]: Not used Bit[2:0]: Debug mode

7.7 sensor control [0x3700 - 0x3712]

table 7-7 sensor control registers

address	register name	default value	R/W	description
0x3700	SENCTRL0	0x20	RW	Sensor Control Register
0x3701	SENCTRL1	0x44	RW	Sensor Control Register
0x3702	SENCTRL2	0x50	RW	Sensor Control Register
0x3703	SENCTRL3	0xBC	RW	Sensor Control Register
0x3704	SENCTRL4	0xF9	RW	Sensor Control Register
0x3705	SENCTRL5	0x14	RW	Sensor Control Register
0x3706	SENCTRL6	0x4B	RW	Sensor Control Register
0x3707	SENCTRL7	0x62	RW	Sensor Control Register
0x3708	SENCTRL8	0x81	RW	Sensor Control Register
0x3709	SENCTRL9	0x41	RW	Sensor Control Register
0x370A	SENCTRLA	0x12	RW	Sensor Control Register
0x370B	SENCTRLB	0x00	RW	Sensor Control Register
0x370C	SENCTRLC	0x10	RW	Sensor Control Register
0x370D	SENCTRLD	0x00	RW	Sensor Control Register
0x370E	SENCTRLE	0x00	RW	Sensor Control Register
0x370F	SENCTRLF	0x00	RW	Sensor Control Register
0x3710	SENCTRL10	0x02	RW	Sensor Control Register
0x3711	SENCTRL11	0x04	RW	Sensor Control Register
0x3712	SENCTRL12	0x3C	RW	Sensor Control Register

7.8 timing control [0x3800 - 0x382A]

table 7-8 timing control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3800	TIMING HS	0x00	RW	Bit[7:5]: Not used Bit[4:0]: HREF horizontal start point[12:8]
0x3801	TIMING HS	0x00	RW	Bit[7:0]: HREF horizontal start point[7:0]
0x3802	TIMING VS	0x00	RW	Bit[7:5]: Not used Bit[4:0]: HREF vertical start point[12:8]
0x3803	TIMING VS	0x00	RW	Bit[7:0]: HREF vertical start point[7:0]
0x3804	TIMING HW	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: HREF horizontal endpoint[12:8]
0x3805	TIMING HW	0xDF	RW	Bit[7:0]: HREF horizontal endpoint[7:0]
0x3806	TIMING VH	0x09	RW	Bit[7:5]: Not used Bit[4:0]: HREF vertical endpoint[12:8]
0x3807	TIMING VH	0x9B	RW	Bit[7:0]: HREF vertical endpoint[7:0]
0x3808	TIMING ISPHO	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: ISP output horizontal width[12:8]
0x3809	TIMING ISPHO	0xC0	RW	Bit[7:0]: ISP output horizontal width[7:0]
0x380A	TIMING ISPVO	0x09	RW	Bit[7:5]: Not used Bit[4:0]: ISP output vertical width[12:8]
0x380B	TIMING ISPVO	0x90	RW	Bit[7:0]: ISP output vertical width[7:0]
0x380C	TIMING HTS	0x0E	RW	Bit[7:0]: Total horizontal size[15:8]
0x380D	TIMING HTS	0x70	RW	Bit[7:0]: Total horizontal size[7:0]
0x380E	TIMING VTS	0x09	RW	Bit[7:0]: Total vertical size[15:8]
0x380F	TIMING VTS	0xB0	RW	Bit[7:0]: Total vertical size[7:0]
0x3810	TIMING HOFFS HIGH	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Horizontal offset[12:8]
0x3811	TIMING HOFFS LOW	0x10	RW	Bit[7:0]: Horizontal offset[7:0]
0x3812	TIMING VOFFS HIGH	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Vertical offset[12:8]
0x3813	TIMING VOFFS LOW	0x06	RW	Bit[7:0]: Vertical offset[7:0]
0x3814	TIMING X INC	0x11	RW	Bit[7:4]: X_odd_inc Bit[3:0]: X_even_inc

table 7-8 timing control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3815	TIMING Y INC	0x11	RW	Bit[7:4]: Y_odd_inc Bit[3:0]: Y_even_inc
0x3816	TIMING HSYNC START HIGH	0x00	RW	Bit[7:0]: hsync_start[15:8]
0x3817	TIMING HSYNC START LOW	0x00	RW	Bit[7:0]: hsync_start[7:0]
0x3818	TIMING HSYNC END HIGH	0x00	RW	Bit[7:0]: hsync_end[15:8]
0x3819	TIMING HSYNC END LOW	0x00	RW	Bit[7:0]: hsync_end[7:0]
0x381A	TIMING HSYNC FIRST HIGH	0x00	RW	Bit[7:0]: hsync_first[15:8]
0x381B	TIMING HSYNC FIRST LOW	0x00	RW	Bit[7:0]: hsync_first[7:0]
0x381C	TIMING THN X OUTPUT SIZE HIGH	0x00	RW	Bit[7:5]: Not used Bit[4:0]: thn_x_output_size[12:8]
0x381D	TIMING THN X OUTPUT SIZE LOW	0x00	RW	Bit[7:0]: thn_x_output_size[7:0]
0x381E	TIMING THN Y OUTPUT SIZE HIGH	0x00	RW	Bit[7:5]: Not used Bit[4:0]: thn_y_output_size[12:8]
0x381F	TIMING THN Y OUTPUT SIZE LOW	0x00	RW	Bit[7:0]: thn_y_output_size[7:0]
0x3820	TIMING REG20	0x00	RW	Bit[7]: vsub48_blc Bit[6]: vflip_blc Bit[5:3]: Debug mode Bit[2]: vflip_dig Bit[1]: vflip_arr Bit[0]: vbin
0x3821	TIMING REG21	0x00	RW	Bit[7]: hdr_en Bit[6]: thn_en Bit[5]: jpeg_en Bit[4:3]: Debug mode Bit[2]: mirr_dig Bit[1]: mirr_arr Bit[0]: hbin
0x3822	TIMING REG22	0x48	RW	Bit[7:0]: Debug mode
0x3823	TIMING REG23	0x40	RW	Bit[7:0]: Debug mode
0x3824	TIMING REG24	0x00	RW	Bit[7:0]: Debug mode

table 7-8 timing control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3825	TIMING REG25	0x00	RW	Bit[7:0]: Debug mode
0x3826	TIMING REG26	0x00	RW	Bit[7:0]: Debug mode
0x3827	TIMING REG27	0x00	RW	Bit[7:0]: Debug mode
0x3828	TIMING REG28	0x0B	RW	Bit[7:0]: Debug mode
0x3829	TIMING REG29	0x00	RW	Bit[7:1]: Not used Bit[0]: Debug mode
0x382A	TIMING XHS CTRL	0x10	RW	Bit[7:6]: Not used Bit[5]: xhs_polarity Bit[4:0]: xhs_width

7.9 strobe control [0x3B00 - 0x3B20]

table 7-9 strobe control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B00	STROBE CTRL00	0x00	RW	Bit[7]: Strobe request ON/OFF Bit[6]: Strobe polarity 0: Active high 1: Active low Bit[5:4]: Pulse width in xenon mode Bit[3]: Not used Bit[2:0]: Strobe mode select 000: Xenon 011: LED1 100: LED2
0x3B01	STROBE CTRL01	0x00	RW	Bit[7:4]: Not used Bit[3]: start_point_sel Bit[2]: Strobe repeat enable Bit[1:0]: Strobe latency 00: Strobe generated at next frame 01: Delay one frame, strobe generated 2 frames later 10: Delay one frame, strobe generated 3 frames later 11: Delay one frame, strobe generated 4 frames later

table 7-9 strobe control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B02	STROBE CTRL02	0x00	RW	Bit[7:2]: Strobe pulse width step Bit[1:0]: Strobe pulse width gain Strobe pulse width = 128 × (2**gain) × (step+1) × sclk_period
0x3B03~ 0x3B04	NOT USED	–	–	Not Used
0x3B05	FREX CTRL 00	0x00	RW	Bit[7:0]: frex_exp[23:16]
0x3B06	FREX CTRL 01	0x00	RW	Bit[7:0]: frex_exp[15:8]
0x3B07	FREX CTRL 02	0x00	RW	Bit[7:0]: frex_exp[7:0]
0x3B09	FREX CTRL 04	0x00	RW	Bit[7:4]: Not used Bit[3:0]: strobe_width[19:16]
0x3B0A	FREX CTRL 05	0x00	RW	Bit[7:0]: strobe_width[15:8]
0x3B0B	FREX CTRL 06	0x00	RW	Bit[7:0]: strobe_width[7:0]
0x3B0C	FREX CTRL 07	0x00	RW	Bit[7:5]: Not used Bit[4:0]: shutter_dly[12:8]
0x3B0D	FREX CTRL 08	0x00	RW	Bit[7:0]: shutter_dly[7:0]
0x3B0E	FREX CTRL 09	0x01	RW	Bit[7:0]: frex_pchg_width[15:8]
0x3B0F	FREX CTRL 0A	0x00	RW	Bit[7:0]: frex_pchg_width[7:0]
0x3B10	FREX CTRL 0B	0x00	RW	Bit[7:0]: datout_dly[15:8]
0x3B11	FREX CTRL 0C	0x00	RW	Bit[7:0]: datout_dly[7:0]
0x3B12~ 0x3B1E	NOT USED	–	–	Not Used
0x3B1F	FREX CTRL 0D	0x04	RW	Bit[7]: Not used Bit[6]: frex_sccb_req_repeat Bit[5]: frex_strobe_out_sel Bit[4]: frex_nopchg Bit[3]: frex_strobe_pol 0: Active high 1: Active low Bit[2]: frex_shutter_pol Bit[1]: frex_sel 0: Internal FREX 1: External FREX Bit[0]: no_latch
0x3B20	FREX CTRL 0E	0x00	RW	Bit[7:1]: Not used Bit[0]: frex_repeat_trig

7.10 OTP control [0x3D80 - 0x3Dn]

table 7-10 OTP control registers

address	register name	default value	R/W	description
0x3D80	OTP DUMP / PROGRAM	0x00	RW	Bit[7:1]: Not used Bit[0]: Program OTP
0x3D81	OTP DUMP / PROGRAM	–	R	Bit[7]: Load_o Bit[6:1]: Not used Bit[0]: Load / dump OTP
0x3D82	OTP DUMP / PROGRAM	0x7D	RW	Bit[7:0]: pgm_pulse
0x3D83	OTP DUMP / PROGRAM	0x05	RW	Bit[7:0]: load_pulse
0x3D84	OTP DUMP / PROGRAM	0x00	RW	Bit[7:5]: Not used Bit[4]: pgm_dis Bit[3]: Bank mode enable Bit[2:0]: Bank index
0x3D85	OTP DUMP / PROGRAM	0x03	RW	Bit[7:6]: Not used Bit[5:0]: start_address
0x3D86	OTP DUMP / PROGRAM	0x03	RW	Bit[7:6]: Not used Bit[5:0]: end_address
0x3D87	OTP DUMP / PROGRAM	0x06	RW	Bit[7:4]: Not used Bit[3:0]: r_ps2cs
0x3D0n (n<0x10) 0x3Dn (0x20>n>0x0F)	OTP DATA “N”	0x00	RW	Bit[7:0]: Data dumped or data to be programmed for Bit[8*(n+1)-1:8*n]

7.11 PSRAM [0x3F00 - 0x3F07]

Changing these register values is not recommended.

table 7-11 PSRAM registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3F00	PSRAM_CTRL0	0x00	RW	Bit[7:2]: Not used Bit[1]: Internal clock option Bit[0]: PSRAM control
0x3F01	PSRAM_CTRL1	0xF0	RW	PSRAM Control Register
0x3F02	PSRAM_CTRL2	0x06	RW	PSRAM Control Register

table 7-11 PSRAM registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3F03	PSRAM_CTRL3	0x66	RW	PSRAM Control Register
0x3F04	PSRAM_CTRL4	0x00	RW	PSRAM Control Register
0x3F05	PSRAM_CTRL5	0x00	RW	PSRAM Control Register
0x3F06	PSRAM_CTRL6	0x00	RW	PSRAM Control Register
0x3F07	PSRAM_CTRL7	0x00	RW	PSRAM Control Register

7.12 BLC control [0x4000 - 0x44013]

table 7-12 BLC control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x29	RW	Bit[7]: BLC bypass enable 0: Disable 1: Enable Bit[6:4]: BLC control 0: Disable 1: Enable Bit[3]: Not used Bit[2]: Apply to black line 0: Disable 1: Enable Bit[1]: Black line average frame 0: Disable 1: Enable Bit[0]: BLC control
0x4001	BLC CTRL01	0x02	RW	Bit[7:6]: Not used Bit[5:0]: BLC start line
0x4002	BLC CTRL02	0x45	RW	Bit[7]: Format change enable 0: BLC remains the same after format change 1: BLC will redo after format change Bit[6]: BLC auto enable 0: BLC offset from manual register 1: BLC offset from auto statistics Bit[5:0]: Reset frame number[5:0]

table 7-12 BLC control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x4003	BLC CTRL03	0x08	RW	Bit[7]: BLC redo enable 0: Normal 1: BLC will redo N frames where N = 0x4003[5:0] Bit[6]: Freeze enable 0: Normal 1: BLC and even offsets will not update priority lower than always update Bit[5:0]: Manual frame number BLC redo frame number
0x4004	BLC CTRL04	0x04	RW	Bit[7:6]: Not used Bit[5:0]: blc_line_num Number of black lines used
0x4005	BLC CTRL05	0x18	RW	Bit[7:5]: Debug mode Bit[4]: Do not output black line 0: Output black line 1: No black line output Bit[3]: blc_man_1_en Apply one channel offset (registers **0x400C**, **0x400D**) to all manual BLC channels Bit[2]: Debug mode Bit[1]: blc_always_up_en 0: BLC will freeze several frames after reset priority higher than freeze enable 1: BLC always update Bit[0]: Debug mode
0x4006	NOT USED	–	–	Not Used
0x4007	BLC CTRL07	0x00	RW	Bit[7:0]: Debug mode
0x4008	BLC TARGET	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Black level target[9:8]
0x4009	BLC TARGET	0x10	RW	Bit[7:0]: Black level target[7:0]
0x400A~ 0x400B	NOT USED	–	–	Not Used
0x400C	BLC CTRL0C	0x00	RW	Bit[7:4]: Not used Bit[3:0]: BLC manual offset channel 0[11:8]
0x400D	BLC CTRL0D	0x00	RW	Bit[7:0]: BLC manual offset channel 0[7:0]
0x400E	BLC CTRL0E	0x00	RW	Bit[7:4]: Not used Bit[3:0]: BLC manual offset channel 1[11:8]
0x400F	BLC CTRL0F	0x00	RW	Bit[7:0]: BLC manual offset channel 1[7:0]
0x4010	BLC CTRL10	0x00	RW	Bit[7:4]: Not used Bit[3:0]: BLC manual offset channel 2[11:8]

table 7-12 BLC control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x4011	BLC CTRL11	0x00	RW	Bit[7:0]: BLC manual offset channel 2[7:0]
0x4012	BLC CTRL12	0x00	RW	Bit[7:4]: Not used Bit[3:0]: BLC manual offset channel 3[11:8]
0x4013	BLC CTRL13	0x00	RW	Bit[7:0]: BLC manual offset channel 3[7:0]

7.13 frame control [0x4200 - 0x4203]

table 7-13 frame control registers

address	register name	default value	R/W	description
0x4200	FC CTRL00	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Debug mode
0x4201	FC CTRL01	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_on_number
0x4202	FC CTRL02	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_off_number
0x4203	FC CTRL03	0x00	RW	Bit[7]: Not used Bit[6:0]: Debug mode

7.14 format control [0x4300 - 0x430F]

table 7-14 format control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x4300	MAX VALUE	0xFF	RW	Bit[7:0]: Max clip value[9:2]
0x4301	MIN VALUE	0x00	RW	Bit[7:0]: Min clip value[9:2]
0x4302	MAX/MIN VALUE	0x0C	RW	Bit[7:4]: Not used Bit[3:2]: Max clip value[1:0] Bit[1:0]: Min clip value[1:0]

table 7-14 format control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x4303	FMT_CTRL3	0x00	RW	Bit[7]: r_inc_en Bit[6]: r_inc_pattern Bit[5]: r_pad_lsb Bit[4]: r_bar_mux Bit[3]: r_bar_en Bit[2]: r_bit_tst_en Bit[1]: r_tst_bit8 Bit[0]: r_bit_tst_md
0x4304	FMT_CTRL4	0x08	RW	Bit[7:5]: Not used Bit[4]: data_swap 0: Normal data output 1: Output {DATA[7:0], DATA[9:8]} Bit[3]: tst_full_win 0: Test pattern in user-defined window 0x4308~0x0430F 1: Test pattern in full window Bit[2:0]: bar_pad
0x4305	FMT_PAD_LOW1	0x40	RW	Bit[7:6]: pad99 Bit[5:4]: pad66 Bit[3:2]: pad33 Bit[1:0]: pad00
0x4306	FMT_PAD_LOW2	0x0E	RW	Bit[7:4]: Not used Bit[3:2]: padff Bit[1:0]: padcc
0x4307	EMBEDED_CTRL	0x31	RW	Bit[7:4]: embed_line_st Bit[3]: embed_start_man Bit[2]: dpc_threshold_opt 0: For white pixel 1: For black pixel Bit[1]: embed_byte_order Bit[0]: embedded_en
0x4308	FMT_TST_X_START_HIGH	0x00	RW	Bit[7:4]: Not used Bit[3:0]: tst_x_start[10:7]
0x4309	FMT_TST_X_START_LOW	0x00	RW	Bit[7:1]: tst_x_start[6:0] Bit[0]: VSYNC mode 0: Mode 1 1: Mode 2
0x430A	FMT_TST_Y_START_HIGH	0x00	RW	Bit[7:4]: Not used Bit[3:0]: tst_y_start[10:7]
0x430B	FMT_TST_Y_START_LOW	0x00	RW	Bit[7:1]: tst_y_start[6:0] Bit[0]: Not used

table 7-14 format control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x430C	FMT_TST_WIDTH_HIGH	0x00	RW	Bit[7:3]: Not used Bit[2:0]: tst_width[10:8]
0x430D	FMT_TST_WIDTH_LOW	0x00	RW	Bit[7:0]: tst_width[7:0]
0x430E	FMT_TST_HEIGHT_HIGH	0x00	RW	Bit[7:3]: Not used Bit[2:0]: tst_height[10:8]
0x430F	FMT_TST_HEIGHT_LOW	0x00	RW	Bit[7:0]: tst_height[7:0]

7.15 VFIFO control [0x4600 - 0x4604]

table 7-15 VFIFO control registers

address	register name	default value	R/W	description
0x4600	VFIFO_CTRL0	0x14	RW	Bit[7:6]: Not used Bit[5]: start_1_line delay Bit[4]: more_auto_en 0: Use 0x4601/0x4602 1: Auto mode Bit[3:0]: Debug mode
0x4601	VFIFO_READ_ST_HIGH	0x14	RW	Bit[7:3]: Not used Bit[2:0]: read_start[10:8]
0x4602	VFIFO_READ_ST_LOW	0x00	RW	Bit[7:0]: read_start[7:0]
0x4603	VFIFO_CTRL3	0x0A	RW	Bit[7:5]: Not used Bit[4:0]: Debug mode
0x4604	VFIFO_PCLK_DIV_MAN	0x01	RW	Bit[7:6]: Not used Bit[5:0]: Debug mode

7.16 MIPI control [0x4800 - 0x485F]

table 7-16 MIPI control registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x4800	MIPI CTRL 00	0x04	RW	MIPI Control 00 Bit[7:6]: Not used Bit[5]: Clock lane gate enable 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: Line sync enable 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: Lane select 0: Use lane1 as default data lane 1: Use lane2 as default data lane Bit[2]: idle_sts 0: MIPI bus will be LP00 when there is no packet to transmit 1: MIPI bus will be LP11 when there is no packet to transmit Bit[1:0]: Debug mode
0x4801	MIPI CTRL 01	0x03	RW	MIPI Control 01 Bit[7]: Long packet data type manual enable 0: Use MIPI data 1: Use dt man o as long packet data Bit[6:5]: spkt_dt_sel 1: Use dt_spkt as short packet data (0x4812/0x4813) Bit[4]: PH bit order for ECC 0: (DI[7:0],WC[7:0], WC[15:8]) 1: (DI[0:7],WC[0:7], WC[8:15]) Bit[3]: PH byte order for ECC 0: (DI,WC L,WC H) 1: (DI,WC H,WC L) Bit[2]: PH byte order2 for ECC 0: (DI,WC) 1: (WC,DI) Bit[1:0]: Debug mode

table 7-16 MIPI control registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x4802	MIPI CTRL 02	0x00	RW	MIPI Control 02 Bit[7]: hs_prepare select 0: Auto calculate T_hs_prepare, unit is pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare select 0: Auto calculate T_clk_prepare, unit is pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post select 0: Auto calculate T_clk_post, unit is pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail select 0: Auto calculate T_clk_trail, unit is pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit select 0: Auto calculate T_hs_exit, unit is pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero select 0: Auto calculate T_hs_zero, unit is pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail select 0: Auto calculate T_hs_trail, unit is pclk2x 1: Use hs_trail_min_o[7:0] Bit[0]: clk_zero select 0: Auto calculate T_clk_zero, unit is pclk2x 1: Use clk_zero_min_o[7:0]
0x4803	MIPI CTRL 03	0x50	RW	Bit[7:0]: Debug mode
0x4804	MIPI CTRL 04	0x8D	RW	Bit[7:0]: Debug mode

table 7-16 MIPI control registers (sheet 3 of 9)

address	register name	default value	R/W	description
0x4805	MIPI CTRL 05	0x10	RW	MIPI Control 05 Bit[7]: lane_disable2 1: Disable MIPI data lane1, lane1 will be LP00 Bit[6]: lane_disable1 1: Disable MIPI data lane2, lane2 will be LP00 Bit[5]: lpx_p_sel 0: Auto calculate t_lpx_o in pclk2x domain, unit clk2x 1: Use lp_p_min[7:0] Bit[4]: lp_rx_intr_sel 0: Send lp_rx_intr_o as the first byte 1: Send lp_rx_intr_o at the end of receiving Bit[3:1]: Debug mode Bit[0]: Not used
0x4806	MIPI CTRL06	0x88	RW	Bit[7:0]: Debug mode
0x4807	MIPI CTRL07	0xA0	RW	Bit[7:0]: Debug mode
0x4808	MIPI CTRL08	0x02	RW	Bit[7:0]: Debug mode
0x4809	MIPI CTRL09	0x01	RW	Bit[7:0]: Debug mode
0x4810	MIPI FCNT MAX	0xFF	RW	Bit[7:0]: Max frame counter of frame sync short packet[15:8]
0x4811	MIPI_FCNT MAX	0xFF	RW	Bit[7:0]: Max frame counter of frame sync short packet[7:0]
0x4812	MIPI SPKT WC REG	0x00	RW	Bit[7:0]: Short packet word counter[15:8]
0x4813	MIPI SPKT WC REG	0x00	RW	Bit[7:0]: Short packet word counter[7:0]
0x4814	MIPI CTRL14	0x2A	RW	MIPI Control 14 Bit[7:6]: vc MIPI virtual channel Bit[5:0]: dt_man Manual data type
0x4815	MIPI DT SPKT	0x00	RW	Bit[7]: Not used Bit[6]: Debug mode Bit[5:0]: Manual data type for short packet
0x4816~ 0x4817	NOT USED	–	–	Not Used
0x4818	MIPI HS ZERO MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_zero_min[9:8] High byte of minimum value of hs_zero, unit ns

table 7-16 MIPI control registers (sheet 4 of 9)

address	register name	default value	R/W	description
0x4819	MIPI HS ZERO MIN	0x96	RW	Bit[7:0]: hs_zero_min[7:0] Low byte of minimum value of hs_zero hs_zero_real = hs_zero_min_o + tui × ui_hs_zero_min_o
0x481A	MIPI HS TRAIL MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_trail_min[9:8] High byte of minimum value of hs_trail, unit ns
0x481B	MIPI HS TRAIL MIN	0x3C	RW	Bit[7:0]: hs_trail_min[7:0] Low byte of minimum value of hs_trail hs_trail_real = hs_trail_min_o + tui × ui_hs_trail_min_o
0x481C	MIPI CLK ZERO MIN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: clk_zero_min[9:8] High byte of minimum value of clk_zero, unit ns
0x481D	MIPI CLK ZERO MIN	0x1C	RW	Bit[7:0]: clk_zero_min[7:0] Low byte of minimum value of clk_zero clk_zero_real = clk_zero_min_o + tui × ui_clk_zero_min_o
0x481E	MIPI CLK PREPARE MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_prepare_min[9:8] High byte of minimum value of clk_prepare, unit ns
0x481F	MIPI CLK PREPARE MIN	0x3C	RW	Bit[7:0]: clk_prepare_min[7:0] Low byte of minimum value of clk_prepare clk_prepare_real = clk_prepare_min_o + tui × ui_clk_prepare_min_o
0x4820	MIPI CLK POST MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_post_min[9:8] High byte of minimum value of clk_post, unit ns
0x4821	MIPI CLK POST MIN	0x56	RW	Bit[7:0]: clk_post_min[7:0] Low byte of minimum value of clk_post clk_post_real = clk_post_min_o + tui × ui_clk_post_min_o

table 7-16 MIPI control registers (sheet 5 of 9)

address	register name	default value	R/W	description
0x4822	MIPI CLK TRAIL MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_trail_min[9:8] High byte of minimum value of clk_trail, unit ns
0x4823	MIPI CLK TRAIL MIN	0x3C	RW	Bit[7:0]: clk_trail_min[7:0] Low byte of minimum value of clk_trail clk_trail_real = clk_trail_min_o + tui × ui_clk_trail_min_o
0x4824	MIPI LPX PCLK MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: lpx_p_min[9:8] High byte of minimum value of lpx_p, unit ns
0x4825	MIPI LPX PCLK MIN	0x32	RW	Bit[7:0]: lpx_p_min[7:0] Low byte of minimum value of lpx_p lpx_p_real = lpx_p_min_o + tui × ui_lpx_p_min_o
0x4826	MIPI HS PREPARE MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_prepare_min[9:8] High byte of minimum value of hs_prepare, unit ns
0x4827	MIPI HS PREPARE MIN	0x32	RW	Bit[7:0]: hs_prepare_min[7:0] Low byte of minimum value of hs_prepare hs_prepare_real = hs_prepare_min_o + tui × ui_hs_prepare_min_o
0x4828	MIPI HS EXIT MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_exit_min[9:8] High byte of minimum value of hs_exit, unit ns
0x4829	MIPI HS EXIT MIN	0x64	RW	Bit[7:0]: hs_exit_min[7:0] Low byte of minimum value of hs_exit hs_exit_real = hs_exit_min_o + tui × ui_hs_exit_min_o
0x482A	MIPI UI HS ZERO MIN	0x05	RW	Bit[7:6]: Not used Bit[5:0]: Minimum UI value of hs_zero, unit UI
0x482B	MIPI UI HS TRAIL MIN	0x04	RW	Bit[7:6]: Not used Bit[5:0]: Minimum UI value of hs_trail, unit UI
0x482C	MIPI UI CLK ZERO MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Minimum UI value of clk_zero, unit UI
0x482D	MIPI UI CLK PREPARE MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Minimum UI value of clk_prepare, unit UI

table 7-16 MIPI control registers (sheet 6 of 9)

address	register name	default value	R/W	description
0x482E	MIPI UI CLK POST MIN	0x34	RW	Bit[7:6]: Not used Bit[5:0]: Minimum UI value of clk_post, unit UI
0x482F	MIPI UI CLK TRAIL MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Minimum UI value of clk_trail, unit UI
0x4830	MIPI UI LPX P MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Minimum UI value of lpx_p (pclk2x domain), unit UI
0x4831	MIPI UI HS PREPARE MIN	0x04	RW	Bit[7:6]: Not used Bit[5:0]: Minimum UI value of hs_prepare, unit UI
0x4832	MIPI UI HS EXIT MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Minimum UI value of hs_exit, unit UI
0x4833	MIPI REG MIN	0x00	RW	Bit[7:0]: mipi_reg_min[15:8] MIPI register address minimum value
0x4834	MIPI REG MIN	0x00	RW	Bit[7:0]: mipi_reg_min[7:0] MIPI register address minimum value
0x4835	MIPI REG MAX	0xFF	RW	Bit[7:0]: mipi_reg_max[15:8] MIPI register address maximum value
0x4836	MIPI REG MAX	0xFF	RW	Bit[7:0]: mipi_reg_max[7:0] MIPI register address maximum value
0x4837	MIPI PCLK PERIOD	0x15	RW	Bit[7:0]: Period of pclk2x, pclk_div = 1, and 1-bit decimal
0x4838	MIPI WKUP DLY	0x02	RW	Bit[7:6]: Not used Bit[5:0]: Wakeup delay for MIPI (Mark1 state) / 2^{12}
0x4839	NOT USED	–	–	Not Used
0x483A	MIPI DIR DLY	0x08	RW	Bit[7:6]: Not used Bit[5:0]: Debug mode

table 7-16 MIPI control registers (sheet 7 of 9)

address	register name	default value	R/W	description
0x483B	MIPI LP GPIO	0x33	RW	Bit[7]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 and lp_p1_o/lp_n1_o (bit[6:4]) to control lane 1 status in software standby mode Bit[6]: lp_dir_man1 0: Input 1: Output Bit[5]: lp_p1_o Bit[4]: lp_n1_o Bit[3]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 and lp_p2_o/lp_n2_o (bit[2:0]) to control lane 2 status in software standby mode Bit[2]: lp_dir_man2 0: Input 1: Output Bit[1]: lp_p2_o Bit[0]: lp_n2_o
0x483C	MIPI CTRL 33	0x42	RW	Bit[7:0]: Debug mode
0x483D	MIPI T TA GO	0x10	RW	Bit[7:0]: Debug mode
0x483E	MIPI T TA SURE	0x06	RW	Bit[7:0]: Debug mode
0x483F	MIPI T TA GET	0x14	RW	Bit[7:0]: Debug mode
0x4840	START OFFSET	0x00	RW	Bit[7:0]: Debug mode
0x4841	START OFFSET	0x00	RW	Bit[7:0]: Debug mode
0x4842	START MODE	0x01	RW	Bit[7:0]: Debug mode
0x4843	SNR PCLK DIV	0x00	RW	Bit[7:2]: Not used Bit[1]: pclk_div_man Global timing control unit 0: Auto calculated pclk divider 1: Manually set pclk divider Bit[0]: Not used
0x4844 0x4849	NOT USED	–	–	Not Used

table 7-16 MIPI control registers (sheet 8 of 9)

address	register name	default value	R/W	description
0x484A	MIPI CTRL4A	0x00	RW	MIPI Control 4A Bit[7]: prbs Test mode Bit[6]: lane_disable4 1: Disable MIPI data lane4, lane4 will be LP00 Bit[5]: lane_disable3 1: Disable MIPI data lane3, lane3 will be LP00 Bit[4]: mipi_test 1: MIP output uses 0x484D, 0x484E, 0x484F, 0x485A, 0x485B values Bit[3:0]: Debug mode
0x484B	MIPI CTRL4B	0x33	RW	MIPI Control 4B Bit[7]: lp_sel3 0: Auto generate mipi_lp_dir3_o 1: Use lp_dir_man3 and lp_p3_o/lp_n3_o (bit[6:4]) to control lane 3 status in software standby mode Bit[6]: lp_dir_man3 0: Input 1: Output Bit[5]: lp_p3_o Bit[4]: lp_n3_o Bit[3]: lp_sel4 0: Auto generate mipi_lp_dir4_o 1: Use lp_dir_man4 and lp_p4_o/lp_n4_o (bit[2:0]) to control lane 4 status in software standby mode Bit[2]: lp_dir_man4 0: Input 1: Output Bit[1]: lp_p4_o Bit[0]: lp_n4_o
0x484C	MIPI CTRL4C	0x02	RW	MIPI Control 4C Bit[7:4]: Not used Bit[3]: cklane_dis 0: Enable, force clock lane to LP00 in software standby mode 1: Disable Bit[2]: Vsub select 0: Valid behind 1: Valid in front Bit[1:0]: Input data valid (e.g., valid for YUV420) 01: Valid = 1 10: Valid = 2 11: Valid = 3

table 7-16 MIPI control registers (sheet 9 of 9)

address	register name	default value	R/W	description
0x484D	MIPI CTRL4D	0xB6	RW	Bit[7:0]: Test pattern data 0
0x484E	MIPI CTRL4E	0xB6	RW	Bit[7:0]: Test pattern data 1
0x484F	MIPI CTRL4F	0xB6	RW	Bit[7:0]: Test pattern data 2
0x4850~ 0x4859	NOT USED	–	–	Not Used
0x485A	MIPI CTRL5A	0xB6	RW	Bit[7:0]: Test pattern data 3
0x485B	MIPI CTRL5B	0x01	RW	Bit[7:2]: Not used Bit[7:0]: Test pattern data 4
0x485C	MIPI CTRL5C	0x3F	RW	Bit[7]: Not used Bit[6]: Debug mode Bit[5]: mipi_slp_man_st MIPI bus status manual control enable in sleep mode Bit[4]: clk_lane_state 0: LP00 1: LP11 Bit[3]: data_lane4_state 0: LP00 1: LP11 Bit[2]: data_lane3_state 0: LP00 1: LP11 Bit[1]: data_lane2_state 0: LP00 1: LP11 Bit[0]: data_lane1_state 0: LP00 1: LP11
0x485D~ 0x485F	NOT USED	–	–	Not Used

7.17 ISP top [0x5000 - 0x5055]

table 7-17 ISP top registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x86	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6:3]: Not used Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Not used
0x5001	ISP CTRL01	0x01	RW	Bit[7:1]: Not used Bit[0]: Manual white balance (MWB) enable 0: Disable 1: Enable
0x5002	NOT USED	–	–	Not Used
0x5003	ISP CTRL03	0x20	RW	Bit[7:6]: Not used Bit[5]: Buffer control enable Must be enabled if DPC or binning filter is used. 0: Disable 1: Enable Bit[4:0]: Not used
0x5004	ISP CTRL04	0x0C	RW	Bit[7:4]: Not used Bit[3]: Debug mode Bit[2:0]: Not used
0x5005	ISP CTRL05	0xDC	RW	Bit[7:5]: Not used Bit[4]: MWB bias ON 0: Disable 1: Enable Bit[3:0]: Not used
0x5006	ISP CTRL06	0x11	RW	Bit[7:0]: Debug mode
0x5007	ISP CTRL07	0x50	RW	Bit[7:0]: Debug mode
0x5008	ISP CTRL08	0x0C	RW	Bit[7:0]: Debug mode
0x5009	ISP CTRL09	0xFC	RW	Bit[7:0]: Debug mode
0x500A	ISP CTRL0A	0x11	RW	Bit[7:0]: Debug mode
0x500B	ISP CTRL0B	0x40	RW	Bit[7:0]: Debug mode
0x500C	ISP CTRL0C	0x0C	RW	Bit[7:0]: Debug mode

table 7-17 ISP top registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x500D	ISP CTRL0D	0xF0	RW	Bit[7:0]: Debug mode
0x500E	ISP CTRL0E	0x11	RW	Bit[7:0]: Debug mode
0x500F	ISP CTRL0F	0x50	RW	Bit[7:0]: Debug mode
0x5010	ISP CTRL10	0x0C	RW	Bit[7:0]: Debug mode
0x5011	ISP CTRL11	0xFC	RW	Bit[7:0]: Debug mode
0x5012~ 0x501E	NOT USED	–	–	Not Used
0x501F	ISP CTRL1F	0x00	RW	Bit[7:6]: Not used Bit[5]: Bypass ISP 0: Disable 1: Enable Bit[4:0]: Debug mode
0x5020~ 0x5024	NOT USED	–	–	Not Used
0x5025	ISP CTRL25	0x00	RW	Bit[7:4]: Debug mode Bit[3:2]: Not used Bit[1:0]: avg_sel 00: Sensor RAW 01: After LENC 10: After MWB gain
0x5026~ 0x5029	NOT USED	–	–	Not Used
0x502A	ISP CTRL2A	0x00	RW	Bit[7:4]: mux_pad_ctrl[3:0] Bit[1]: Debug mode Bit[0]: Not used
0x502B~ 0x503C	NOT USED	–	–	Not Used
0x503D	ISP CTRL3D	0x08	RW	Bit[7:0]: Debug mode
0x503E	ISP CTRL3E	0x00	RW	Bit[7:0]: Debug mode
0x503F	ISP CTRL3F	0x20	RW	Bit[7:0]: Debug mode
0x5040	NOT USED	–	–	Not Used

table 7-17 ISP top registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5041	ISP CTRL41	0x0C	RW	Bit[7]: Manual scaling select 0: Disable 1: Enable Bit[6]: Not used Bit[5]: Manual scaling enable 0: Scaling disable 1: Scaling enable Bit[4]: Post binning filter enable 0: Disable 1: Enable Bit[3]: Not used Bit[2]: Average enable 0: Disable 1: Enable Bit[1:0]: Not used
0x5042	NOT USED	–	–	Not Used
0x5043	ISP CTRL43	0x08	RW	Bit[7:0]: Debug mode
0x5044	ISP CTRL44	0x00	RW	Bit[7:0]: Debug mode
0x5045	ISP CTRL45	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Not used
0x5046	ISP CTRL46	0x00	RW	Bit[7:0]: Debug mode
0x5047	ISP CTRL47	0x00	RW	Bit[7:0]: Debug mode
0x5048	ISP CTRL48	0x10	RW	Bit[7:0]: Debug mode
0x5049	ISP CTRL49	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Debug mode
0x504A	ISP CTRL4A	0x00	RW	Bit[7:0]: Debug mode
0x504B	ISP CTRL4B	0x00	RW	Bit[7:0]: Debug mode
0x504C	ISP CTRL4C	0x00	RW	Bit[7:0]: Debug mode
0x504D	ISP CTRL4D	0x00	RW	Bit[7:0]: Debug mode
0x504E~ 0x5055	NOT USED	–	–	Not Used

7.18 scale control [0x5041, 0x5600 - 0x5608]

table 7-18 scale control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5041	ISP CTRL41	0x0C	RW	Bit[7]: Manual scaling select 0: Disable, scale is auto enable when the output size is less than the input size 1: Enable, scale is manually enabled or disabled, depending on register 0x5041[5] Bit[6]: Not used Bit[5]: Manual scaling enable 0: Scaling disable 1: Scaling enable Bit[4]: Post binning filter enable 0: Disable 1: Enable Bit[3]: Not used Bit[2]: Average enable 0: Disable 1: Enable Bit[1:0]: Not used
0x5600	SCALE CTRL00	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Scale horizontal factor[9:8]
0x5601	SCALE CTRL01	0x00	RW	Bit[7:0]: Scale horizontal factor[7:0]
0x5602	SCALE CTRL02	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Scale vertical factor[9:8]
0x5603	SCALE CTRL03	0x00	RW	Bit[7:0]: Scale vertical factor[7:0]
0x5604	SCALE CTRL04	0x01	RW	Bit[7:1]: Not used Bit[0]: Scale auto enable 0: Use manual scaling factor from registers 0x5600~0x5603 1: Calculate the scaling factor from the input size and the output size set in registers 0x3800~0x380B
0x5068	HSCALE_CTRL	0x00	RW	Bit[7:6]: Horizontal MSB Bit[5]: Not used Bit[4:0]: scale_ctrl0
0x506A	VSCALE_CTRL	0x00	RW	Bit[7:6]: Vertical MSB Bit[5]: Not used Bit[4:0]: scale_ctrl1

table 7-18 scale control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5605	SCALE CTRL05	–	R	Bit[7:0]: Horizontal scale factor[15:8]
0x5606	SCALE CTRL06	–	R	Bit[7:0]: Horizontal scale factor[7:0]
0x5607	SCALE CTRL07	–	R	Bit[7:5]: Not used Bit[4:0]: Inverse vertical scale factor[4:0]
0x5608	SCALE CTRL08	–	R	Bit[7:5]: Not used Bit[4:0]: Inverse horizontal scale factor[4:0]

7.19 average control [0x5041, 0x5680 - 0x5688]

table 7-19 average control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5041	ISP CTRL41	0x0C	RW	Bit[7]: Manual scaling select 0: Disable 1: Enable Bit[6]: Not used Bit[5]: Manual scaling enable 0: Scaling disable 1: Scaling enable Bit[4]: Post binning filter enable 0: Disable 1: Enable Bit[3]: Not used Bit[2]: Average enable 0: Disable 1: Enable Bit[1:0]: Not used
0x5680	AVG CTRL00	0x00	RW	Bit[7:4]: Not used Bit[3:0]: X start offset[11:8]
0x5681	AVG CTRL01	0x00	RW	Bit[7:0]: X start offset[7:0]
0x5682	AVG CTRL02	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Y start offset[11:8]
0x5683	AVG CTRL03	0x00	RW	Bit[7:0]: Y start offset[7:0]
0x5684	AVG CTRL04	0x10	RW	Bit[7:4]: Not used Bit[3:0]: Window width[11:8]
0x5685	AVG CTRL05	0xA0	RW	Bit[7:0]: Window width[7:0]

table 7-19 average control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5686	AVG CTRL06	0x0C	RW	Bit[7:4]: Not used Bit[3:0]: Window height[11:8]
0x5687	AVG CTRL07	0x78	RW	Bit[7:0]: Window height[7:0]
0x5688	AVG CTRL08	0x02	RW	Bit[7:2]: Not used Bit[1]: Average option Bit[0]: Average size manual 0: Disable, use ISP pre-scale 1: Enable, use registers 0x5680~0x5687

7.20 DPC control [0x5000, 0x5780 - 0x5791]

table 7-20 DPC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x86	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6:3]: Not used Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Not used
0x5780	DPC CTRL00	0x1C	RW	DPC Control Register
0x5781	DPC CTRL01	0x13	RW	DPC Control Register
0x5782	DPC CTRL02	0x03	RW	DPC Control Register
0x5783	DPC CTRL03	0x08	RW	DPC Control Register
0x5784	DPC CTRL04	0x0C	RW	DPC Control Register
0x5785	DPC CTRL05	0x10	RW	DPC Control Register
0x5786	DPC CTRL06	0x08	RW	DPC Control Register
0x5787	DPC CTRL07	0x10	RW	DPC Control Register
0x5788	DPC CTRL08	0x10	RW	DPC Control Register

table 7-20 DPC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5789	DPC CTRL09	0x08	RW	DPC Control Register
0x578A	DPC CTRL0A	0x04	RW	DPC Control Register
0x578B	DPC CTRL0B	0x02	RW	DPC Control Register
0x578C	DPC CTRL0C	0x02	RW	DPC Control Register
0x578D	DPC CTRL0D	0x0C	RW	DPC Control Register
0x578E	DPC CTRL0E	0x06	RW	DPC Control Register
0x578F	DPC CTRL0F	0x02	RW	DPC Control Register
0x5790	DPC CTRL10	0x02	RW	DPC Control Register
0x5791	DPC CTRL11	0xFF	RW	DPC Control Register

7.21 LENC control [0x5000, 0x5800 - 0x5856]

table 7-21 LENC registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x86	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6:3]: Not used Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Not used
0x5800	LENC CTRL00	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Magnitude of parameter of G channel matrix (g00)
0x5801	LENC CTRL01	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Magnitude of parameter of G channel matrix (g01)
0x5802	LENC CTRL02	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Magnitude of parameter of G channel matrix (g02)

table 7-21 LENC registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5803	LENC CTRL03	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Magnitude of parameter of G channel matrix (g03)
0x5804	LENC CTRL04	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Magnitude of parameter of G channel matrix (g04)
0x5805	LENC CTRL05	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Magnitude of parameter of G channel matrix (g05)
0x5806~ 0x580B	LENC CTRL06~ LENC CTRL0B	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Magnitude of parameter of G channel matrix (g10~g15)
0x580C~ 0x5811	LENC CTRL0C~ LENC CTRL11	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Magnitude of parameter of G channel matrix (g20~25)
0x5812~ 0x5817	LENC CTRL12~ LENC CTRL17	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Magnitude of parameter of G channel matrix (g30~35)
0x5818~ 0x581D	LENC CTRL18~ LENC CTRL1D	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Magnitude of parameter of G channel matrix (g40~g45)
0x581E~ 0x5823	LENC CTRL1E~ LENC CTRL23	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Magnitude of parameter of G channel matrix (g50~g55)
0x5824	LENC CTRL24	0x00	RW	Bit[7:4]: Magnitude of parameter of B channel matrix (b00) Bit[3:0]: Magnitude of parameter of R channel matrix (r00)
0x5825	LENC CTRL25	0x00	RW	Bit[7:4]: Magnitude of parameter of B channel matrix (b01) Bit[3:0]: Magnitude of parameter of R channel matrix (r01)
0x5826	LENC CTRL26	0x00	RW	Bit[7:4]: Magnitude of parameter of B channel matrix (b02) Bit[3:0]: Magnitude of parameter of R channel matrix (r02)
0x5827	LENC CTRL27	0x00	RW	Bit[7:4]: Magnitude of parameter of B channel matrix (b03) Bit[3:0]: Magnitude of parameter of R channel matrix (r03)

table 7-21 LENC registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5828	LENC CTRL28	0x00	RW	Bit[7:4]: Magnitude of parameter of B channel matrix (b04) Bit[3:0]: Magnitude of parameter of R channel matrix (r04)
0x5829~ 0x583C	LENC CTRL29~ LENC CTRL3C	0x00	RW	Bit[7:4]: Magnitude of parameter of B channel matrix (b10~b14, b20~b24, b30~b34, b40~b44) Bit[3:0]: Magnitude of parameter of R channel matrix (r10~r14, r20~r24, r30~r34, r40~r44)
0x583D	LENC CTRL3D	0x88	RW	Bit[7:4]: LENC B offset Bit[3:0]: LENC R offset
0x583E	LENC CTRL3E	0x40	RW	Bit[7:0]: Maximum gain
0x583F	LENC CTRL3F	0x20	RW	Bit[7:0]: Minimum gain
0x5840	LENC CTRL40	0x18	RW	Bit[7:0]: Minimum Q
0x5841	LENC CTRL41	0x0D	RW	Bit[7:4]: Not used Bit[3]: Enable add BLC 0: Disable 1: Enable Bit[2]: Black level enable 0: Disable 1: Enable Bit[1]: Not used Bit[0]: Auto Q enable 0: Disable 1: Enable
0x5842	LENC CTRL42	0x00	RW	Bit[7:3]: Not used Bit[2:0]: br_Hscale[10:8]
0x5843	LENC CTRL43	0x99	RW	Bit[7:0]: br_Hscale[7:0]
0x5844	LENC CTRL44	0x00	RW	Bit[7:3]: Not used Bit[2:0]: br_Vscale[10:8]
0x5845	LENC CTRL45	0xCC	RW	Bit[7:0]: br_Vscale[7:0]
0x5846	LENC CTRL46	0x00	RW	Bit[7:3]: Not used Bit[2:0]: g_Hscale[10:8]
0x5847	LENC CTRL47	0xCC	RW	Bit[7:0]: g_Hscale[7:0]
0x5848	LENC CTRL48	0x00	RW	Bit[7:3]: Not used Bit[2:0]: g_Vscale[10:8]
0x5849	LENC CTRL49	0x88	RW	Bit[7:0]: g_Vscale[7:0]
0x584A~ 0x584F	NOT USED	–	–	Not Used

table 7-21 LENC registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5850	LENC CTRL50	–	R	Bit[7:2]: Not used Bit[1:0]: x_offset[9:8]
0x5851	LENC CTRL51	–	R	Bit[7:0]: x_offset[7:0]
0x5852	LENC CTRL52	–	R	Bit[7:2]: Not used Bit[1:0]: y_offset[9:8]
0x5853	LENC CTRL53	–	R	Bit[7:0]: y_offset[7:0]
0x5854	LENC CTRL54	–	R	Bit[7:6]: Not used Bit[5]: Flip Bit[4]: Mirror Bit[3:2]: y_skip Bit[1:0]: x_skip
0x5855	LENC CTRL55	–	R	Bit[7:4]: Not used Bit[3]: overflow_gh Bit[2]: overflow_brh Bit[1]: overflow_gv Bit[0]: overflow_brv
0x5856	LENC CTRL56	–	R	Bit[7]: Not used Bit[6:0]: m_nq[9:8]

7.22 pre BLC [0x5C00 - 0x5C08]

table 7-22 pre BLC registers

address	register name	default value	R/W	description
0x5C00	PBLC CTRL00	0x80	RW	Pre BLC Control Registers
0x5C01	PBLC CTRL01	0x00	RW	Pre BLC Control Registers
0x5C02	PBLC CTRL02	0x00	RW	Pre BLC Control Registers
0x5C03	PBLC CTRL03	0x00	RW	Pre BLC Control Registers
0x5C04	PBLC CTRL04	0x00	RW	Pre BLC Control Registers
0x5C05	PBLC CTRL05	0x00	RW	Pre BLC Control Registers
0x5C06	PBLC CTRL06	0x00	RW	Pre BLC Control Registers
0x5C07	PBLC CTRL07	0x80	RW	Pre BLC Control Registers
0x5C08	PBLC CTRL08	0x10	RW	Pre BLC Control Registers

7.23 pre ISP [0x5E00 - 0x5E11]

table 7-23 pre ISP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5E00	PRE ISP CTRL00	0x00	RW	Bit[7]: Test enable Bit[6]: Rolling enable Rolling bar in test mode Bit[5]: Transparent image + normal image enable Bit[4]: test_squ Square B&W enable Bit[3:2]: Color bar pattern select 00: Normal color bar pattern 01: Color bar pattern with vertical fading 10: Color bar pattern with horizontal fading 11: Color bar pattern with horizontal and vertical fading Bit[1:0]: test_sel
0x5E01	PRE ISP CTRL01	0x41	RW	Bit[7]: Not used Bit[6]: win_cut enable Bit[5]: isp_test Low bits to 0 Bit[4]: Random Random data reset Bit[3:0]: random_seed
0x5E02	PRE ISP CTRL02	0x00	RW	Bit[7:0]: Line number INT[15:8]
0x5E03	PRE ISP CTRL03	0x01	RW	Bit[7:0]: Line number INT[7:0]
0x5E04	PRE ISP CTRL04	0x00	RW	Bit[7:0]: Scale X input manual size[15:8]
0x5E05	PRE ISP CTRL05	0x00	RW	Bit[7:0]: Scale X input manual size[7:0]
0x5E06	PRE ISP CTRL06	0x01	RW	Bit[7:0]: Scale Y input manual size[15:8]
0x5E07	PRE ISP CTRL07	0x00	RW	Bit[7:0]: Scale Y input manual size[7:0]
0x5E08	PRE ISP CTRL08	0x00	RW	Bit[7:0]: X manual offset[15:8]
0x5E09	PRE ISP CTRL09	0x00	RW	Bit[7:0]: X manual offset[7:0]
0x5E0A	PRE ISP CTRL10	0x00	RW	Bit[7:0]: Y manual offset[15:8]
0x5E0B	PRE ISP CTRL11	0x01	RW	Bit[7:0]: Y manual offset[7:0]
0x5E0C	PRE ISP CTRL12	–	R	Bit[7:0]: pixel_number[15:8]
0x5E0D	PRE ISP CTRL13	–	R	Bit[7:0]: pixel_number[7:0]

table 7-23 pre ISP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5E0E	PRE ISP CTRL14	–	R	Bit[7:0]: line_number[15:8]
0x5E0F	PRE ISP CTRL15	–	R	Bit[7:0]: line_number[7:0]
0x5E10	PRE ISP CTRL16	0x0C	RW	Bit[7:6]: Not used Bit[5:2]: Debug mode Bit[1]: Offset manual enable Bit[0]: Scale input size manual mode
0x5E11	PRE ISP CTRL17	0x00	RW	Bit[7:0]: Debug mode

7.24 illumination control [0x6600 - 0x6611]

table 7-24 illumination control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x6600	ILLUMINATION CTRL00	0x10	RW	Bit[7:5]: Not used Bit[4:0]: pulse_dly1 First pulse delay 0~31 0x00: -0.5 frame 0x1F: 0.5 frame
0x6601	ILLUMINATION CTRL01	0x10	RW	Bit[7:5]: Not used Bit[4:0]: pulse_dly2 Second pulse delay 0~31 0x00: -0.5 frame 0x1F: 0.5 frame
0x6602	ILLUMINATION CTRL02	0x10	RW	Bit[7:5]: Not used Bit[4:0]: pulse_dly3 Third pulse delay 0~31 0x00: -0.5 frame 0x1F: 0.5 frame
0x6603	ILLUMINATION CTRL03	0x10	RW	Bit[7:5]: Not used Bit[4:0]: pulse_dly4 Fourth pulse delay 0~31 0x00: -0.5 frame 0x1F: 0.5 frame
0x6604	ILLUMINATION CTRL04	0x11	RW	Bit[7:4]: Second pulse duration (0~15 frames) Bit[3:0]: First pulse duration (0~15 frames)

table 7-24 illumination control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x6605	ILLUMINATION CTRL05	0x11	RW	Bit[7:4]: Fourth pulse duration (0~15 frames) Bit[3:0]: Third pulse duration (0~15 frames)
0x6606	ILLUMINATION CTRL06	0x1F	RW	Bit[7:5]: Not used Bit[4:0]: duty_cycle_pulse1 (0~31)
0x6607	ILLUMINATION CTRL07	0x1F	RW	Bit[7:5]: Not used Bit[4:0]: duty_cycle_pulse2 (step)
0x6608	ILLUMINATION CTRL08	0x1F	RW	Bit[7:5]: Not used Bit[4:0]: duty_cycle_pulse3 (0~31)
0x6609	ILLUMINATION CTRL09	0x1F	RW	Bit[7:5]: Not used Bit[4:0]: duty_cycle_pulse4 (step)
0x660A	ILLUMINATION CTRL0A	0x00	RW	Bit[7:0]: Gap1 between pulse0 and pulse1 (0~255 frames)
0x660B	ILLUMINATION CTRL0B	0x00	RW	Bit[7:0]: Gap2 between pulse1 and pulse2
0x660C	ILLUMINATION CTRL0C	0x00	RW	Bit[7:0]: Gap3 between pulse2 and pulse3
0x660D	ILLUMINATION CTRL0D	0x00	RW	Bit[7:0]: Gap4 between pulse3 and pulse0
0x660E	ILLUMINATION CTRL0E	0x00	RW	Bit[7]: pwm_req Bit[6]: Not used Bit[5]: Illum_sel Bit[4]: duty_no_map Bit[3]: no_gap Bit[2]: sel_slot_out Bit[1]: Manual duty cycle for d1 and d3 Bit[0]: pwm_repeat
0x660F	ILLUMINATION CTRL0F	0x02	RW	Bit[7:4]: Not used Bit[3:0]: slot_width
0x6610	ILLUMINATION CTRL10	0x01	RW	Bit[7:4]: Not used Bit[3:0]: ramp2_xstep_r Second pulse duty cycle step
0x6611	ILLUMINATION CTRL11	0x01	RW	Bit[7:4]: Not used Bit[3:0]: ramp4_xstep_r Fourth pulse duty cycle step

7.25 TPM control [0x6700 - 0x6721]

table 7-25 TPM registers

address	register name	default value	R/W	description
0x6700~ 0x6705	TPM CTRL00~05	–	–	TPM Control Registers
0x6706	TPM CTRL06	0x78	RW	Bit[7]: Debug mode Bit[6:4]: db_period Bit[3:0]: Temp clock divisor Sample clock = XVCLK/clock divisor Divisor = 1 if bit[3:0] = 0 Sample clock must be around 3MHz
0x6707~ 0x670A	TPM CTRL07~0A	–	–	TPM Control Registers
0x670B	TPM CTRL0B	0x00	RW	Bit[7]: Trigger temperature sensor Bit[6:0]: Measured temperature (0°C ~ 80°C)
0x670C~ 0x6721	TPM CTRL0C~21	–	–	TPM Control Registers

7.26 CADC [0x6900 - 0x6901]

table 7-26 CADC registers

address	register name	default value	R/W	description
0x6900	CADC CTRL00	0x61	RW	CADC Control Registers
0x6901	CADC CTRL01	0x04	RW	CADC Control Registers

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +95°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-30°C to +70°C junction temperature
stable image temperature[b]	0°C to +50°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

8.3 DC characteristics

table 8-3 DC characteristics (-30°C < T_J < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-D}[a]	supply voltage (digital core)	1.425	1.5	1.575	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.0	V
I_{DD-A}	active (operating) current[b]		70	85	mA
I_{DD-IO}			90	110	mA
$I_{DDS-SCCB}$	standby current[c]		30	60	µA
$I_{DDS-PWDN}$			30	60	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[d]	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}[d]	SIOC and SIOD	1.28	1.8	3.0	V

a. using the internal regulator is strongly recommended for minimum power down currents

b. active current is based on sensor resolution at full size and full speed, with AVDD = 2.8V and DOVDD = 1.8V

c. standby current is measured at room temperature

d. based on DOVDD = 1.8V

8.4 timing characteristics

table 8-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns

a. if using internal PLL

8.5 VCM characteristics

table 8-5 VCM characteristics

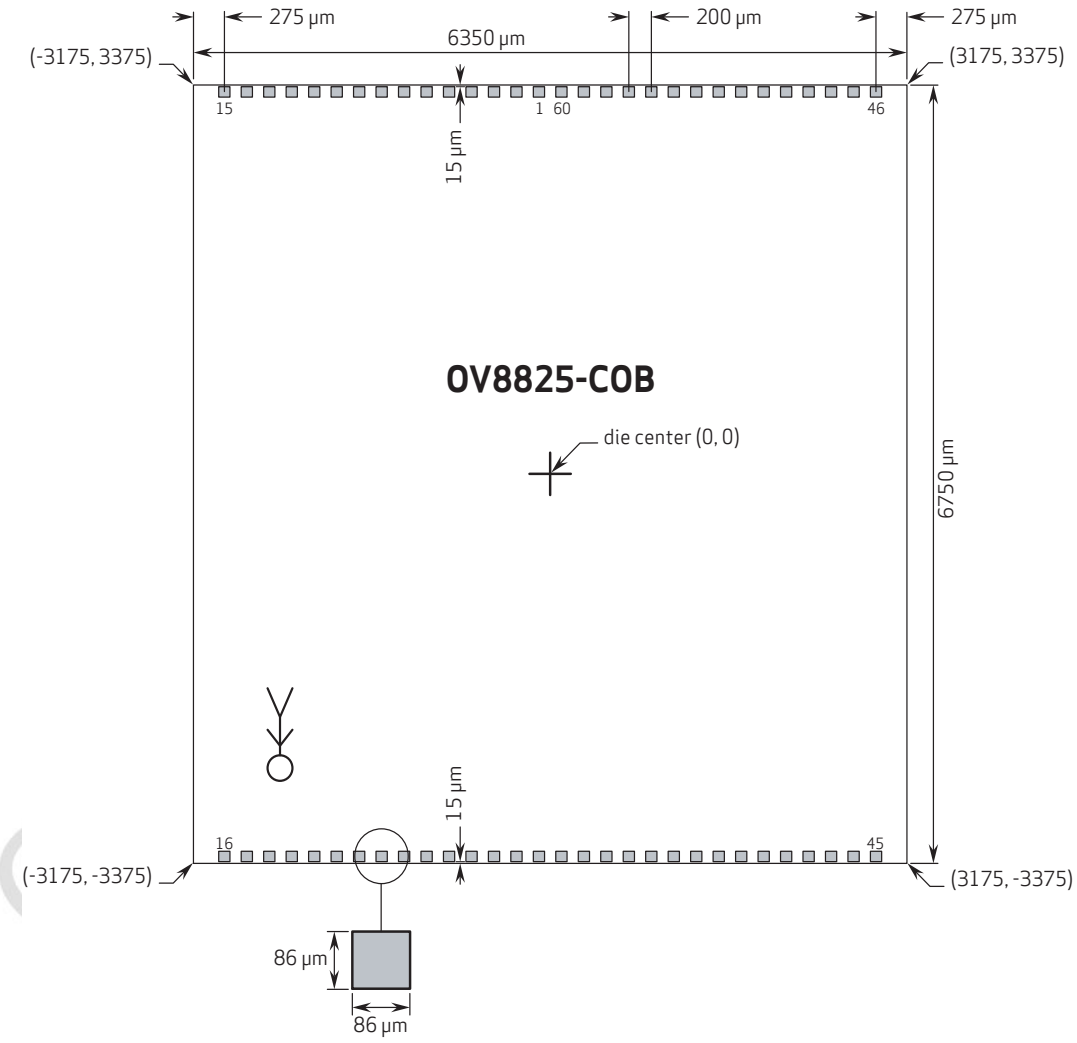
parameter[a]	condition	min	typ	max	unit
power	AVDD, AGND	2.6	2.8	3.1	V
power on time			10		µs
DC performance					
resolution	100 µA/LSB		10		bits
differential non-linearity (DNL)	guaranteed monotonic	-1		+1	LSB
relative accuracy (INL)			±1		LSB
zero code error	set all 10 bits low		0.2		mA
output characteristics					
minimum output current			0.2		mA
maximum output current				100	mA
output power down current			4.5		µA
output current settling time	test code changed from 1/4 FS to 3/4 FS		200		µs

a. AVDD = 2.6 ~ 3.1V, Rs = 3.3Ω, Vvcm = AVDD, temperature = -30 ~ 70°C, VCM model as a R series with L where R = 26Ω and L = 680 uH

9 mechanical specifications

9.1 physical specifications

figure 9-1 die specifications



note 1 all dimensions and coordinates are in µm.

8825_COB_DS_9_1

table 9-1 pad location coordinates (sheet 1 of 2)

pad number	pad name	x coordinate	y coordinate	bond pad opening size
01	SIOD	-100	3315	86x86
02	VSYNC	-300	3315	86x86
03	FREX	-500	3315	86x86
04	SHUTTER	-700	3315	86x86
05	AVDD	-900	3315	86x86
06	AGND	-1100	3315	86x86
07	STROBE	-1300	3315	86x86
08	RESETB	-1500	3315	86x86
09	PWDNB	-1700	3315	86x86
10	TM	-1900	3315	86x86
11	SGND	-2100	3315	86x86
12	DVDD	-2300	3315	86x86
13	DGND	-2500	3315	86x86
14	AVDD	-2700	3315	86x86
15	AGND	-2900	3315	86x86
16	AGND	-2900	-3315	86x86
17	AVDD	-2700	-3315	86x86
18	DGND	-2500	-3315	86x86
19	DVDD	-2300	-3315	86x86
20	EGND	-2100	-3315	86x86
21	PVDD	-1900	-3315	86x86
22	XVCLK	-1700	-3315	86x86
23	DOVDD	-1500	-3315	86x86
24	MDP2	-1300	-3315	86x86
25	MDN2	-1100	-3315	86x86
26	MDP0	-900	-3315	86x86
27	MDN0	-700	-3315	86x86
28	MCP	-500	-3315	86x86
29	MCN	-300	-3315	86x86
30	EGND	-100	-3315	86x86

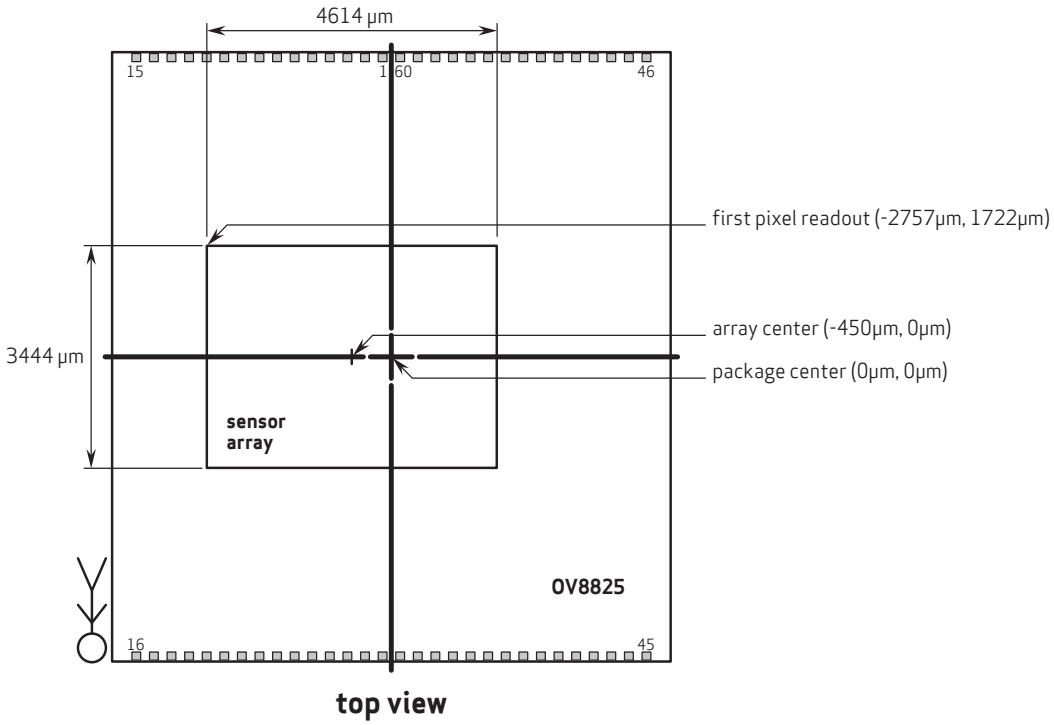
table 9-1 pad location coordinates (sheet 2 of 2)

pad number	pad name	x coordinate	y coordinate	bond pad opening size
31	EVDD	100	-3315	86x86
32	MDP1	300	-3315	86x86
33	MDN1	500	-3315	86x86
34	MDP3	700	-3315	86x86
35	MDN3	900	-3315	86x86
36	DVDD	1100	-3315	86x86
37	DGND	1300	-3315	86x86
38	AVDD	1500	-3315	86x86
39	AGND	1700	-3315	86x86
40	VSNK	1900	-3315	86x86
41	VSNK	2100	-3315	86x86
42	VGND	2300	-3315	86x86
43	VGND	2500	-3315	86x86
44	DVDD	2700	-3315	86x86
45	DGND	2900	-3315	86x86
46	DGND	2900	3315	86x86
47	DVDD	2700	3315	86x86
48	DOVDD	2500	3315	86x86
49	DVDD	2300	3315	86x86
50	DOVDD	2100	3315	86x86
51	DVDD	1900	3315	86x86
52	DOVDD	1700	3315	86x86
53	AGND	1500	3315	86x86
54	AVDD	1300	3315	86x86
55	DOGND	1100	3315	86x86
56	VH	900	3315	86x86
57	VNH	700	3315	86x86
58	VNL	500	3315	86x86
59	AGND	300	3315	86x86
60	SIOC	100	3315	86x86

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pad 1 oriented down on the PCB.

8825_COB_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

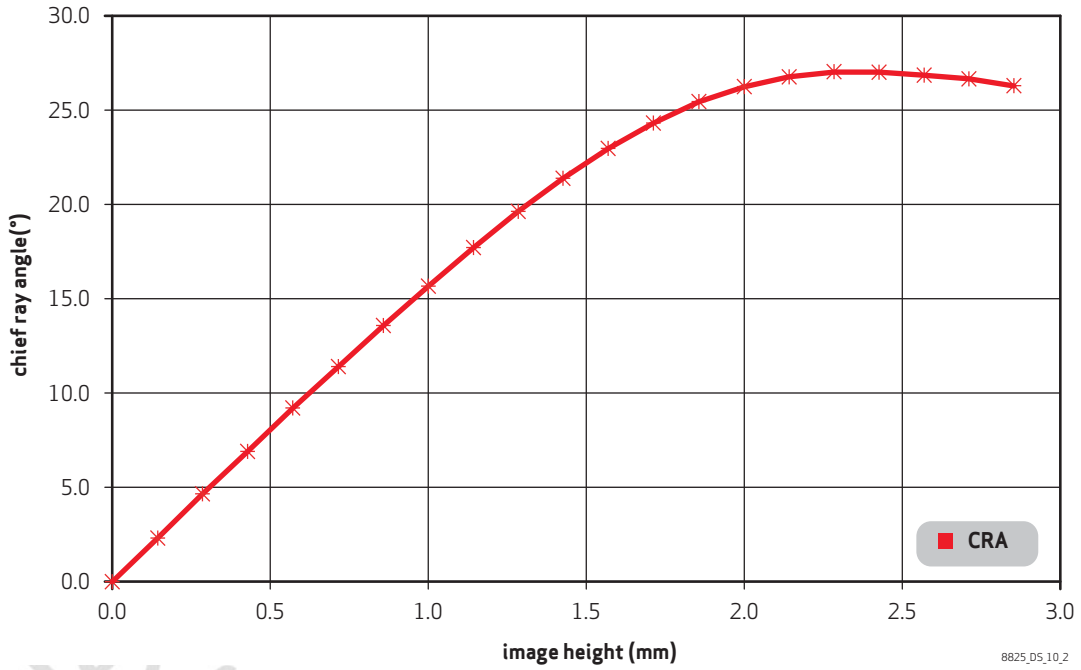


table 10-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0.00	0.000	0.0
0.05	0.143	2.3
0.10	0.286	4.6
0.15	0.428	6.9
0.20	0.571	9.2
0.25	0.714	11.4
0.30	0.857	13.6
0.35	1.000	15.7
0.40	1.142	17.7
0.45	1.285	19.6
0.50	1.428	21.4

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.55	1.571	23.0
0.6	1.714	24.4
0.65	1.856	25.5
0.70	1.999	26.3
0.75	2.142	26.8
0.80	2.285	27.0
0.85	2.428	27.0
0.90	2.570	26.9
0.95	2.713	26.7
1.00	2.856	26.3

appendix A handling of RW devices

A.1 ESD /EOS prevention

1. Ensure that there is 500V ESD control in all work areas.
2. Use ESD safety shoes, ground strap, and static control smocks in test areas.
3. Use grounded work carts and tables in inspection areas.
4. OmniVision recommends the use of ionized air in all work areas.

A.2 particles and cleanliness of environment

1. All production, inspection and packaging areas should meet Class10 environment requirements.
2. Use optical microscopes with 50X and 100X magnifications for particle inspection.
3. Ensure that there is good cassette sealing for particle protection during storage.
4. OmniVision recommends air blowing to remove removable particles.
5. RW die should be stored in nitrogen gas purged cabinets with temperature less than 30°C and relative humidity of 60% before assembly.

A.3 other requirements

1. Reliability assurance of RW or COB bare die is certified by product reliability of the bare die in a CLCC, CSP or QFP package form factor. Precautions should be taken if the packaging form factor of the bare die is other than these specified.
2. Avoid exposure to strong sunlight for extended periods of time as the color filter of the image sensor may become discolored.
3. Avoid direct exposure of the sensor bare die to high temperature and/or humidity environment as sensor characteristics will be affected. Extra precautions should be exercised if the bare die experiences temperatures exceeding 260°C for more than 75 seconds.

revision history

version 1.0 08.24.2011

- initial release

version 1.1 01.19.2012

- changed OmniBSI to OmniBSI+ in all places
- in key specifications on page i, changed active power requirements to 160 mA (358 mW)
- in table 8-3, changed typ and max values for active (operating) current (I_{DD-A}) to 70 and 85, respectively
- in table 8-3, changed typ and max values for active (operating) current (I_{DD-IO}) to 90 and 110, respectively
- changed figure 9-1 to show bond pad opening size of 86x86
- in table 9-1, deleted x pitch and y pitch columns, changed last column name to "bond pad opening size" and changed bond pad size 150x70 to bond pad opening size 86x86

version 1.11 02.01.2012

- in table 1-1, changed pad type for pads 12, 19, 31, 36, 44, 47, 49, and 51 to "power"
- in table 1-2, changed SIOD configuration for RESET, after RESET release, software standby, and hardware standby conditions to "open drain", "I/O", "I/O", and "open drain", respectively
- in table 1-2, changed VSYNC, FREX, SHUTTER, and STROBE configurations for RESET and after RESET release conditions to "high-z"
- in table 1-2, changed MDP2, MDN2, MDP0, MDN0, MDP1, MDN1, MDP3, and MDN3 configurations for after RESET release condition to "high-z"
- in table 1-2, changed MCP and MCN configurations for RESET and after RESET release conditions to "zero" and for software standby and hardware standby conditions to "zero by default (configurable)"

version 1.2 03.13.2012

- changed "I2C" to "SCCB" throughout entire datasheet
- on page i, removed "...and mobile..."
- in section 2.1, updated second paragraph
- in section 2, updated figure 2-1and section descriptions for sections 2.5, 2.6, 2.7.1, 2.8, and 2.12
- in section 2.3, updated section description from "...1/2/4..." to "a one, two, or four"
- in table 2-1, changed header description from "technology" to "methodology"
- in section 2.8.1, updated information for list numbers 3 and 7
- in sub-section 2.8.2, updated information for list numbers 5
- in section 2.9, updated second sentence of section description

- in section 3.2, updated section title and description
- in section 4.2, updated last sentence of section description
- in section 4.5, replaced first paragraph, added second paragraph, and subsections 4.5.1 and 4.5.2
- in sub-section 4.10.1, changed "It" to "The OV8825" in last sentence of section description
- in sub-section 4.10.2, updated section description
- in section 5, updated section descriptions for sections 5.1 and 5.3, and 5.6
- in section 6.1 updated section description
- in table 6-1, changed bit description for register 0x0100[0] to "Streaming..."
- in table 7-1, changed bit description for register 0x0100[0] to "Streaming..."
- in section 7.11, added "It is not recommended to change these register values." to section description

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- changed datasheet from Preliminary Specification to Product Specification

the clear advantage™

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