MLX83202/MLX83203

Automotive NFET pre-drivers

Features and Benefits

- Level shifting between micro-controller PWM outputs and 3 external N-FET half-bridges
- 100% PWM operation
- Low offset, low drift, fast current sense amplifier
- Operating range VSUP = [4.5, 28] V, 45V Abs. Max
- Fault interrupt & feedback to microcontroller
- Under & overvoltage protection
- Overtemperature protection
- VDS and VGS external FET monitoring
- Sleep mode with low quiescent current
- Compatible with 3V and 5V micro-controllers
- Charge-pump provides NFET reverse polarity drive

Application Examples

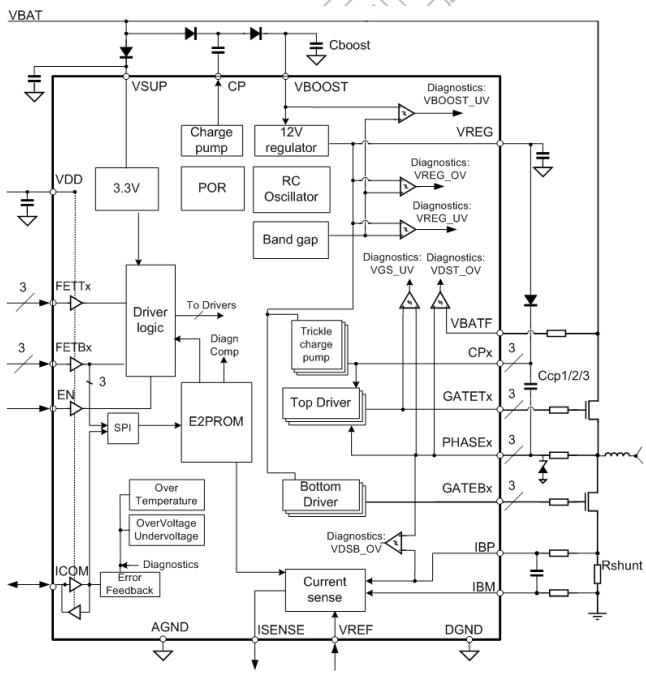
- Fail-safe applications
- Low-torque control applications
- BLDC sine wave applications (PMSM)

Ordering Information

Part No.	Temperature Code	Package Code	Option code	Comment
MLX83202	K (-40°C to 125°C)	LQ (QFN32, 5x5mm)	AAA 000	25 Ohm 3HB (*)
MLX83202	K	PF (TQFP48, 7x7mm)	AAA 000	25 Ohm 3HB (*)
MLX83203	**K**	**LQ (QFN32, 5x5mm)**	**AAA 000**	**8 Ohm 3HB**
MLX83203	K	PF (TQFP48, 7x7mm)	AAA 000	8 Ohm 3HB (*)

(*): Derivatives of MLX83203KLQAAA-000 available on high volume request

1 Functional Diagram



2 General Description

The MLX83202/MLX83203 family of pre-drivers is designed to drive high-current N-type FET 3-phase motor control applications.

The built-in EEPROM allows extensive configurability of the pre-driver without the need for external resistors and SPI interface programming. This reduces the package pin count to only 32.

All output voltages are monitored for failure conditions. The microcontroller is informed of the failure condition via a fast serial interface.

The device comprises a current shunt amplifier, with a high gain bandwidth (GBW), offering a fast settling time with low noise. This makes the pre-drivers ideal for precise torque control applications like e.g. electrical power steering and brake by wire.

A combination of bootstrap and charge pump enables driving 6 NFETs, with gate charges up to 400nC/NFET with a minimum of device self-heating.

The IC reset level below 4.5V allows for low-voltage operation.

Table of Contents

3 Glossary of Terms

OVT	Overtemperature
OV	Overvoltage
UV	Undervoltage
POR	Power-On-Reset
CP	Charge pump
VDD	Logic supply (3.3V or 5V)
Vds	Drain-source voltage
Vgs	Gate-source voltage
HV	High Voltage (>5V)

4 Absolute Maximum Ratings

All voltages are referenced to ground (GND). Positive currents flow into the IC. The absolute maximum ratings given in the table below are limiting values that do not lead to a permanent damage of the device. Exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Reliable operation of the IC is only specified within the limits shown in “Operating conditions”.

Parameter	Symbol	Condition	Limit		Unit
			Min	Max	
Supply voltage	VSUP, VBATF	t < 500ms (note 1)	-0.3	45	V
		Permanent (functional)	-0.3	28	V
VDD supply voltage	VDD		-0.3	5.5	V
Voltage on Analog LV	VAN_LV		-0.3	VDD+0.3	V
Digital Output Voltage	VOUT_DIG		-0.3	VDD+0.3	V
Digital Input Voltage	VIN_DIG		-0.3	VDD+0.3	V
Digital Input Current	IIN_DIG		-10	10	mA
Input voltage on PHASEX pins	VIN_PHASE		-0.7	45	V
Maximum latch–up free current at any pin	ILATCH	according JEDEC JESD78, AEC-Q100-004	-100	100	mA
ESD capability of any other pin	ESD	Human body model (note 2)	-2	+2	kV
Storage temperature	Tstg		-55	150	°C
Junction Temperature	TJ	(note 3)	-40	150 (175 under revision)	°C
Thermal resistance Package	Rthja	in free air on multilayer pcb (JEDEC 1s2p)	37		K/W
	Rthjc	referring to center of exposed pad	10		K/W

Table 1. Maximum ratings

Note:

1. Only during Loaddump pulse.
2. Equivalent to discharging a 100pF capacitor through a 1.5kOhm resistor conform to MIL STD 883 method 3015.7
3. For applications with Tj > 125C: The Extended temperature range is only allowed for a limited period of time. The application mission profile has to be agreed by Melexis. Some analog parameters may drift out of limits, but chip functionality is guaranteed.

5 Pin Definitions and Descriptions

MLX8320x QFN32	MLX8320x TQFP48	Name	Type	Function
1	4	IBM	LV analog input	Current sensor input (negative input)
2	5	IBP	LV Analog input	Current sensor input (positive input)
3	6	ISENSE	LV Analog	Current sensor output
4	7	FETB1	LV Digital input	PWM input for low-side N-FET1 (active low), MISO for SPI
5	8	FETB2	LV Digital input	PWM input for low-side N-FET2 (active low), CLK for SPI
6	9	FETB3	LV Digital input	PWM input for low-side N-FET3 (active low), MOSI for SPI
7	10	ICOM	LV IO	Diagnostic feedback IO, !CS for SPI
8	11	EN	LV IO	Enable input
9	14	PHASE2	HV output	Motor phase 2: high-side N-FET2 Source connection
10	15	GATET2	HV output	PWM output to high-side N-FET2 Gate
11	16	CP2	HV input	Supply input (bootstrap) for high-side N-FET2 Gate
12	17	PHASE1	HV output	Motor phase 1: high-side N-FET1 Source connection
13	18	GATET1	HV output	PWM output to high-side N-FET1 Gate
14	19	CP1	HV input	Supply (bootstrap) input for high-side NFET1
15	20	PHASE3	HV output	Motor phase 3: high-side N-FET3 Source connection
16	21	GATET3	HV output	PWM output to high-side N-FET3 Gate
17	22	CP3	HV input	Supply (bootstrap) input for high-side NFET3 Gate
18	26	VBOOST	HV input	Charge pump generated supply input
19	28	VREG	HV output	Regulated supply for bootstrap capacitors and low-side pre-driver
20	29	GATEB2	HV Output	PWM output to low-side N-FET2 Gate
21	30	GATEB3	HV Output	PWM output to low-side N-FET3 Gate
22	31	GATEB1	HV Output	PWM output to low-side N-FET1 Gate
23	33	DGND	Ground	Driver ground
24	35	CP	HV Output	Charge pump driver output to boost VBOOST
25	38	VSUP	HV Supply input	Power supply input
26	39	VBATF	HV input	VBAT sense input for 3 high-side N-FETs to monitor Vds
27	41	AGND	Ground	Analog ground
28	43	FETT2	LV Digital	PWM input for high-side N-FET2
29	44	FETT1	LV Digital	PWM input for high-side N-FET1
30	45	FETT3	LV Digital	PWM input for high-side N-FET3
31	47	VDD	LV Supply	Digital IO and current sensor amplifier supply.
32	3	VREF	LV Analog input	Reference voltage input for current sense

Table 2. Pin definitions and descriptions

6 Electrical Specifications

DC and AC Operating Range (unless otherwise specified)

- T_A = -40°C to 125°C,
- VSUP = [7, 18]V
- VDD = 3.3V or 5V

	Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Battery Supply							
P.1	Supply voltage	VSUP		7		18	V
P.2	Supply voltage extended range low	VSUP_ERL	Functional with relaxed specification	4.5		7	V
P.2b	Supply voltage extended range high	VSUP_ERH	Functional with relaxed specification	18		28	V
P.3	Quiescent current drawn from VSUP	Issleep	VDD=low			30	uA
P.4	Operating current drawn from VSUP	Isup_int	Pre-driver operation without charge pump operation (EN_CP=0) and without switching			1	mA
P.5	Battery overvoltage threshold high	VSUP_OVH	Warning on ICOM			35	V
P.6	Battery overvoltage threshold low	VSUP_OVL	ICOM released	30			V
P.7	Battery overvoltage threshold hysteresis	VSUP_OVHY		0.4	1		V
P.102	Battery overvoltage debounce time	VSUP_OV_deb				2	us
P.8	Battery undervoltage threshold low	VSUP_UVH	Warning on ICOM	5			V
P.9	Battery undervoltage threshold high	VSUP_UVL	ICOM released			6	V
P.10	Battery undervoltage threshold hysteresis	VSUP_UVHY		0.2	0.5		V
P.103	Battery undervoltage debounce time	VSUP_UV_deb				10	us
P.11	Power on reset level	VPOR	Reset released on rising edge of VSUP, while VDD = high	3		4.5	V
Power and Temperature							
P.12	Overtemperature protection high	OVT_h	Warning on ICOM	153	166	183	°C
P.13	Overtemperature protection low	OVT_l	ICOM released	123	137	153	°C

VDD IO supply input							
P.14	VDD operating current	IDD	Maximum input current Includes ICOM current sourcing			20	mA
P.15	VDD pull down resistance	VDDRPD		200	300	370	KOhm
P.16	VDD input voltage	VDD	VDD= 3.3V or 5V logic supply	3		5.5	V
P.17	VDD undervoltage high[1]	VDD_UV_H	NFET control activated	2.7		2.85	V
P.18	VDD undervoltage low	VDD_UV_L	NFET control disabled	2.55		2.7	V
P.19	VDD undervoltage hysteresis	VDD_UV_HY		0.07	0.1	0.13	V
P.20	VDD sleep voltage high	VDDsleepH	Out of sleep	2.1		2.7	V
P.21	VDD sleep voltage low	VDDsleepL	Goto sleep	1.5		2.05	V
P.22	VDD sleep voltage hysteresis	VDDsleepHY		0.45	0.58	0.85	V
On-chip oscillator							
P.25	ICOM PWM frequency fast	FICOMF		85	100	115	KHz
P.26	ICOM PWM frequency slow	FICOMS		10.6	12.5	14.4	KHz
	Oscillator frequency	FOSC	Internal Oscillator	6.8	8	9.2	MHz
P.27	SPI start up pulse duration	Tspi_su	EN=Low, FETT1/2/3=low, FETB1/2/3=high	2048/FOSC		4096/FOSC	s
Charge pump: CPMODE=x		**(Silicon diodes BAS16, Cpump=1uF,Cboost=1uF +Creg=4.7uF)**					
	Resistive Load from VBOOST to GND	Rboost_leak	Rtyp at room temperature Rmin at 150C Tj (excluding Rvreg_leak)	6	8		MOhm
	Output slew rate				100		V/us
	Charge pump Frequency	FreqCP		170	200	230	kHz
Charge pump: CPMODE=0							
	Load current on VREG	Ireg_cpmode0	VREG > 11V, EN_CP = 1			40	mA
	Output voltage VREG	Vreg	VSUP > 8V, I reg < 40mA	11	12	13	V
	Output voltage VREG	Vreg	VSUP =[7,8]V, Ireg <40mA	10		13	V
	VBOOST undervoltage high	Vboost_UVH	ICOM released	6.1		7.2	V
	VBOOST undervoltage low	Vboost_UVL	Warning on ICOM	5.7		6.7	V
Charge pump: CPMODE=1							
	Load current on VREG	Ireg_cpmode1	VREG > 11V, EN_CP = 1			20	mA
	Reverse polarity NFET gate voltage (VBOOST-VSUP)	Vgs_RPFET	VSUP > 7 Ireg < 20mA	5	12	13	V
	Output voltage VREG	Vreg	Ireg < 20mA	11	12	13	V
	VBOOST undervoltage high (VBOOST-VSUP)	Vboost_UVH	ICOM released	6.1		7.2	V
	VBOOST undervoltage low (VBOOST-VSUP)	Vboost_UVL	Warning on ICOM	5.7		6.7	V
	VBOOST overvoltage	Vboost_dis	Disable and discharge charge pump at VSUP_OV				

[1] The info VDD_UV_X is used to disable the control of the external FETs

VREG warnings (CPMODE=X)							
	Internal Resistive Load from VREG to GND	Rvreg_leak	Rtyp at room temperature Rmin at 150C Tj	0.3	0.4		MOhm
P.34	VREG overvoltage high	Vreg_OVH	Warning on ICOM	14.2		16.5	V
P.35	VREG overvoltage low	Vreg_OVL	ICOM released	13.5		15.8	V
P.36	VREG overvoltage hysteresis	Vreg_OVHY		0.65	1.3		V
P.37	VREG undervoltage high	Vreg_UVH	ICOM released	7.2		8.1	V
P.38	VREG undervoltage low	Vreg_UVL	Warning on ICOM	6.9		7.8	V
VBATF							
	Internal leakage from VBATF to GND	Rvbatf_leak	Pre-driver is not in sleep mode			20	uA
FET Gate drivers							
P.40	Driver ON resistance [2]	R_dr_on			4	8	Ohm
P.41	Rise time	Tr	Cload = 1nF, 20% to 80%	6	7	15	ns
P.42	Fall time	Tf	Cload = 1nF, 80% to 20%	4	7	15	ns
P.43	Pull-up ON resistance low-side pre-driver	Ron_up	-10mA Tj = -40 -10mA, Tj = 150	2.4	4	7	Ohm
	Pull-up ON resistance high-side pre-driver				4	8.5	Ohm
P.44	Pull-down ON resistance low-side pre-driver	Ron_dn	10mA Tj = -40 10mA, Tj = 150	1.5		5.7	Ohm
	Pull-down ON resistance high-side pre-driver					9.2	Ohm
P.45	Turn-on Gate drive peak current	Igon	VGS=0V		-1	-1.4	A
P.46	Turn-off Gate drive peak current	Igoff	VGS=12V		1	1.6	A
P.50	Propagation delay	Tpddrv	From logic input threshold to 2V VGS drive output at no load	20		100	ns
P.51	Propagation delay matching	Tpddrvm	Transitions at the different phases at no load condition	-20		20	ns
P.52	Programmable dead time : asynchronous internal delay between high-side and low-side pre-driver	Tdead	DEAD_TIME [2:0]=000 001 010 011 100 101 110 111		0 0.5 0.75 1.0 1.5 2.0 3.0 6.0		us
P.55	Dead time tolerance	Tdead_tol		-15		15	%
P.53b	Programmable Vds monitor voltage	Vds_mon	VDSMON[2:0]=000: Disabled 001 010 011 100 101 110 111	 0.4 0.6 0.85 1.05 1.25 1.5 1.70	 0.5 0.75 1.00 1.25 1.50 1.75 2.00	 0.6 0.9 1.15 1.45 1.75 2.00 2.3	V

[2] The driver on resistance is < 5 Ohm at 25°C, maximum values correspond with 150°C

P.54	Programmable Vds monitor blanking time: Internal delay between GATE signal high and enabling the corresponding Vds monitor	Tvds_bl	VDS_BLANK_TIME[1:0] =00 01 10 11	0.59 1.22 2.5 4.9	0.75 1.5 3 6	0.93 1.94 4.12 8.44	us
P.56	Sleep gate discharge resistor	Rsgd	Internal resistance between FET gate-source pins to switch-off FET. VDD = 0V (sleep mode) VGS =0.5V			1	KOhm
P.57	Trickle charge pump current capability	Itcp	VSUP>12V, PHASE2/3 = VSUP, CP2/3=PHASE2/3+6.5V	-35		-25	uA
P.58	VGS undervoltage high	Vgs_UVH	ICOM released	42		70	%VREG
	VGS undervoltage low	Vgs_UVL	Warning on ICOM	36		63	%VREG
P.60	PWM frequency	F_dr_pwm		5	20	100	KHz
P.61	Leakage from CPx to PHx	Rcp_leak	Typ at room temperature Min at 150C Tj	0.75	1		MOhm
Logic IO (FET inputs, EN input)							
P.63	Digital input high Voltage	VIN_dig_h	Minimum voltage for input to be treated as logical high	70			%VDD
P.64	Digital input low Voltage	VIN_dig_l	Maximum voltage for input to be treated as logical low			30	%VDD
P.65	Input pull-up resistance	RIN_dig_pu	FETB1, FETB2, FETB3	90		410	KOhm
P.66	Input pull-down resistance	RIN_dig_pd	FETT1,FETT2, FETT3	90		410	KOhm
P.67	Input pull-down resistance	R_EN_pd	EN	90		410	KOhm
SPI timing							
P.68	SPI initial setup time	Tspi_isu		2			us
P.69	SPI clock frequency	Fspi				500	KHz
P.70	Rise/fall times	Tspi_rf	CLK, CSB, MISO, MOSI			200	ns
P.71	CSB setup time	TCSB_su		1			us
P.72	CSB high time	TCSB_H		2			us
P.73	Clock high time	TCLK_H		1			us
P.74	Clock low time	TCLK_L		1			us
P.75	Data in setup time	TDI_su		1			us
P.76	Data in hold time	TDI_h		500			us
P.77	Data out ready delay	TDO_r	Cload at FETB1<50pF		500		us
	EEPROM read delay	T_EE_RD	EE_RD = 1	6			us
	EEPROM write delay	T_EE_WR	EE_RD = 1	12			ms
ICOM output							
P.78	pullup current	ICOM_PU	Vicom=0V	-2.23		-5	mA
P.79	pulldown current	ICOM_PD	Vicom=VDD	5		2.6	mA
Enable input							
P.80	Bridge disable propagation delay	EN_PR_DEL	From Bridge enable EN < 0.2*VDD to VGS < 0.5V, Cload=1nF			1	us

Current sense amplifier							
P.81	Input offset voltage	VIS_IO	Input diff. voltage within +/-100mV, Common mode [-0.5,1.0]V	-7.3		7.6	mV
P.82	Input offset voltage thermal drift	VIS_IO_TDRIFT		-10		10	uV/°C
P.83	Input common mode rejection DC	IS_CMRR_DC		60			dB
P.84	Input common mode rejection 1MHz	IS_CMRR_AC		40			dB
P.85	Input power supply rejection DC for VDD supply	IS_PSRR_DC		60			dB
P.86	Input power supply rejection 1MHz for VDD supply	IS_PSRR_AC		40			dB
P.87	Closed loop gain	IS_GAIN	Gain programmable in EEPROM	-3%	8.0 10.3 13.3 17.2 22.2 28.7 37.0 47.8	+3%	-
P.88	Output settling time	IS_SET	Amplified output to 99% of final value after input change			1.0	us
P.89	Output voltage range high	V_ISENSEmax	Current sense output max level	VDD-0.020		VDD	V
P.90	Output voltage range low	V_ISENSEmin	Current sense output min level	GND		GND +0.020	V
P.91	Output short circuit current to ground	I_Isensesc	Output current saturation level		1.4		mA
P.92	GBW	IS_GBW		10			MHz
P.93	Output slew rate	IS_SR			40		V/us
P.94	CM spike recovery	IS_CM_REC	CM spike=+- 1.5V, duration=250nsec			730	ns
P.95	VREF voltage input	Vref		0		50	%VDD

Table 3. Electrical specifications

7 Block diagram and application circuit

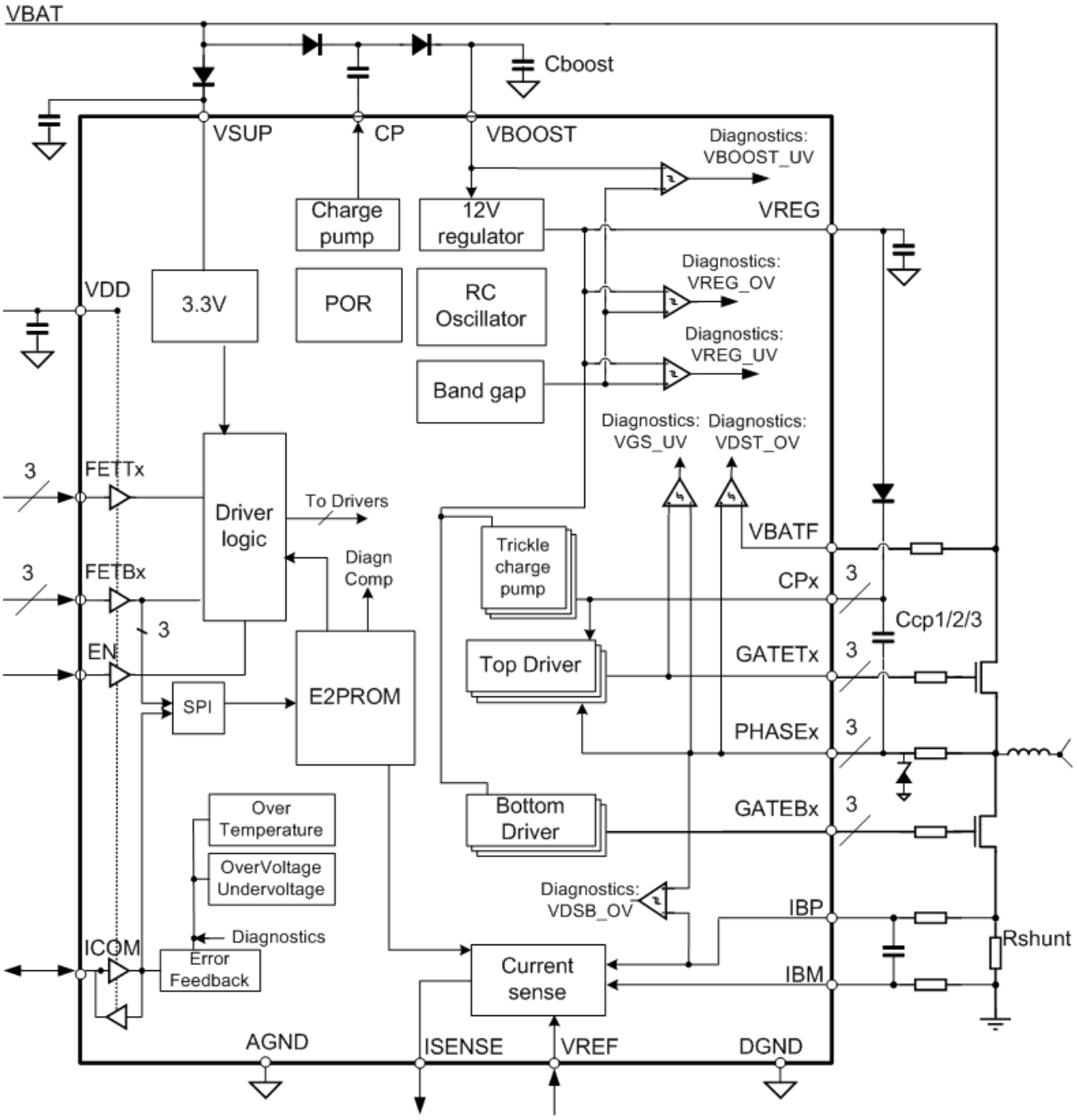


Figure 1. Block diagram

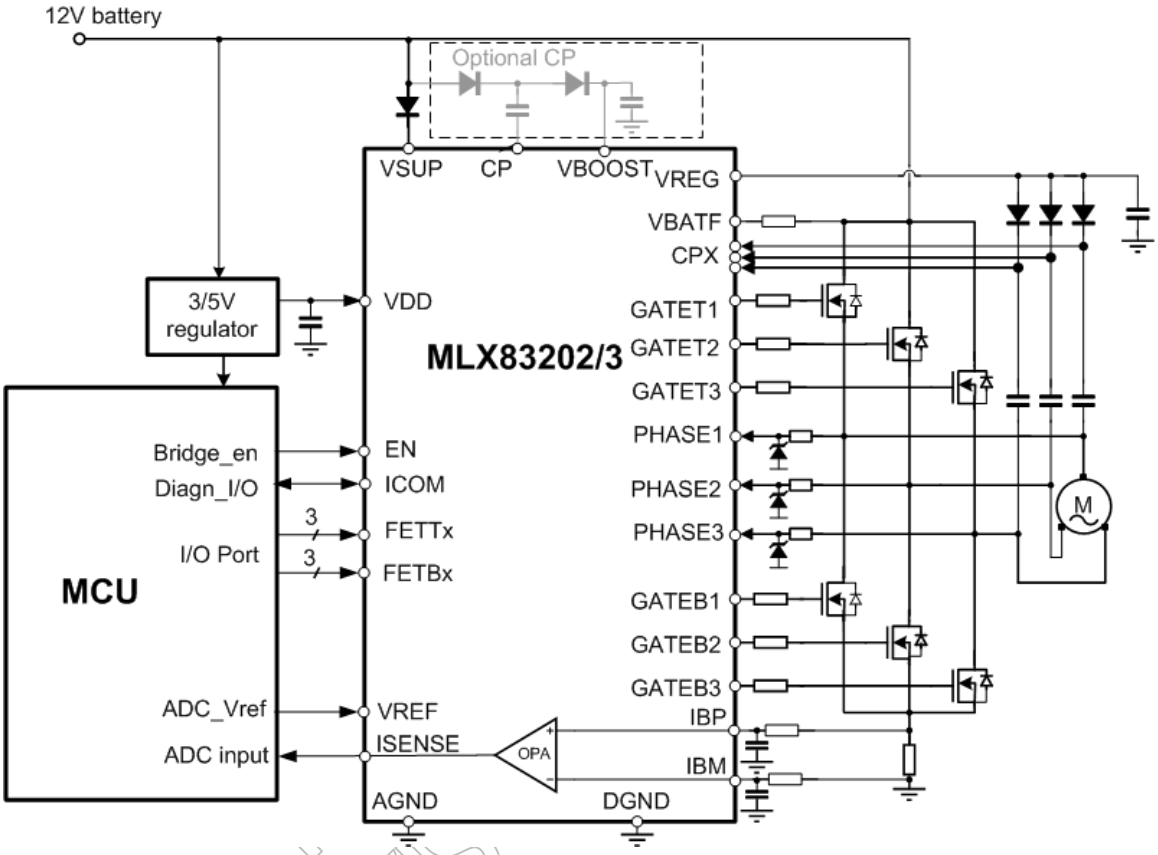


Figure 2. Application schematic 1

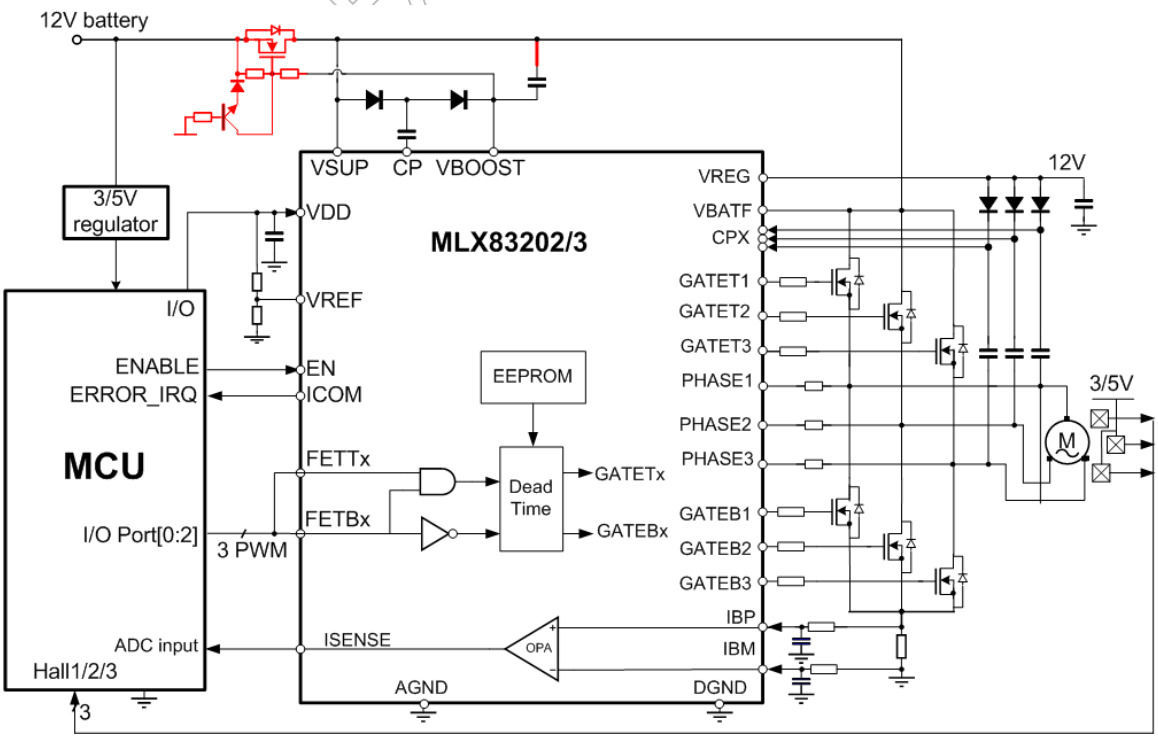


Figure 3. Application schematic 2: internal dead time + HS Reverse Polarity NFET

7.1 Pinout schematics

Principle schematics highlighting ESD connections:

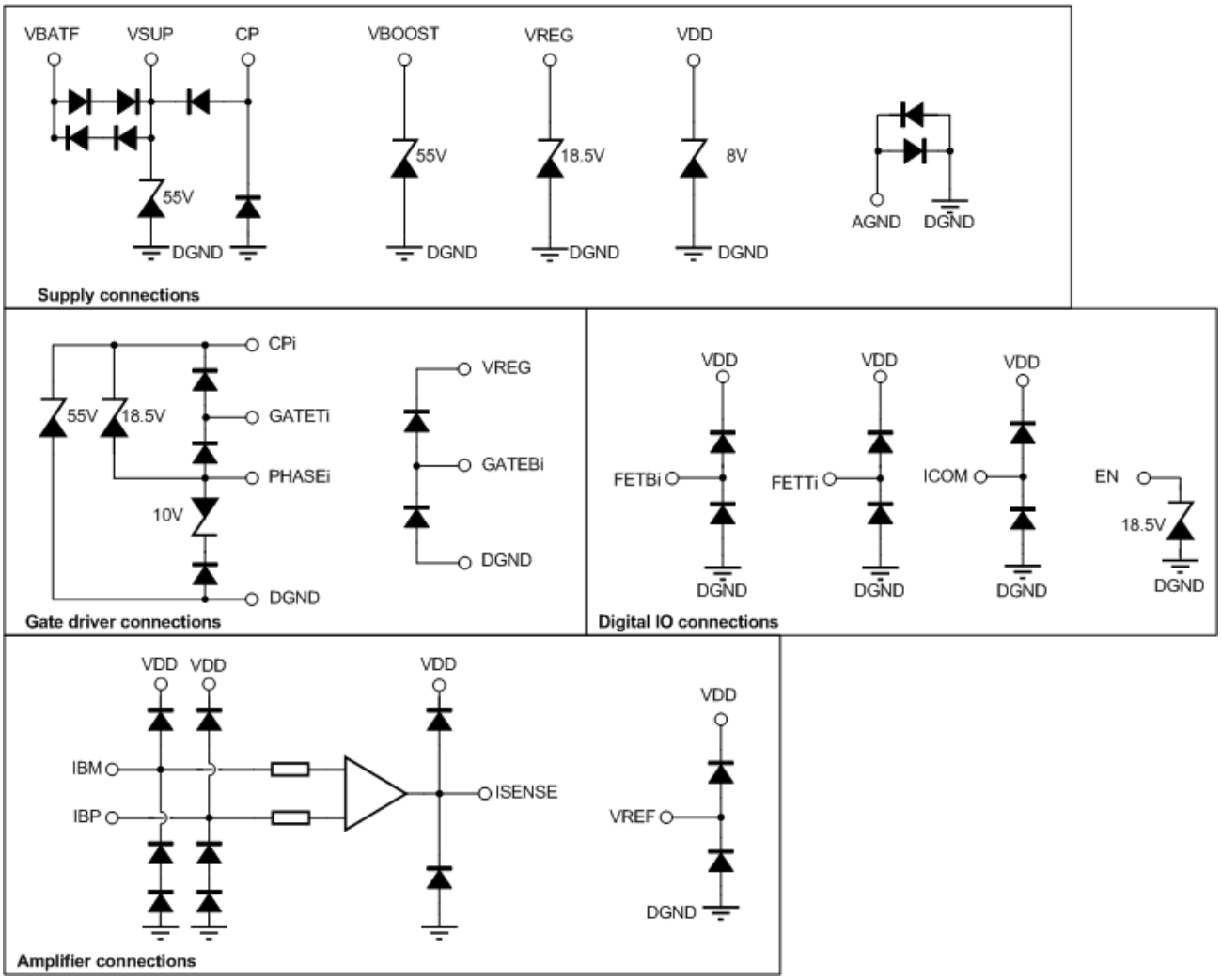


Figure 4. Pin Internal connections

7.2 Ground connections

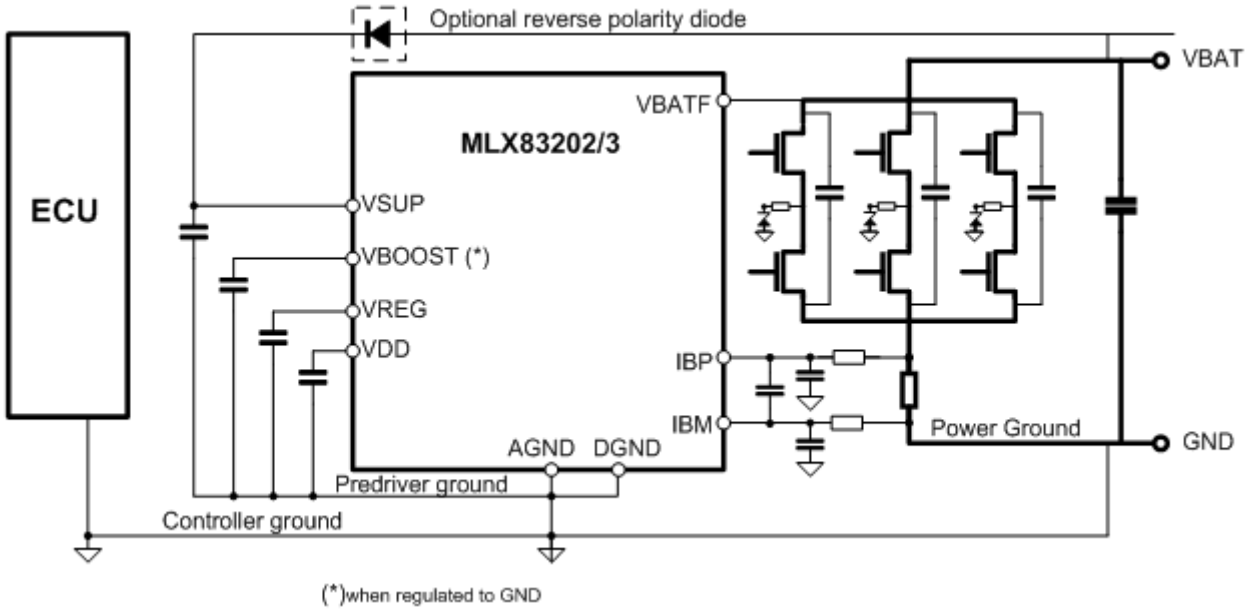


Figure 5. Ground connections

8 Description

8.1 Supply system

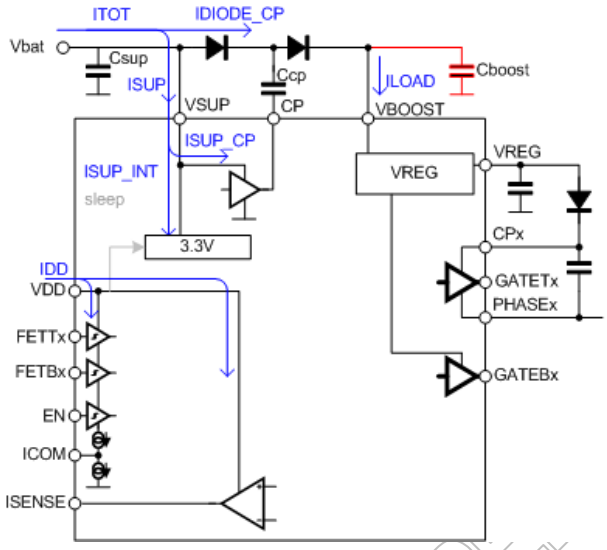


Figure 6. Supply system, CPMODE=0

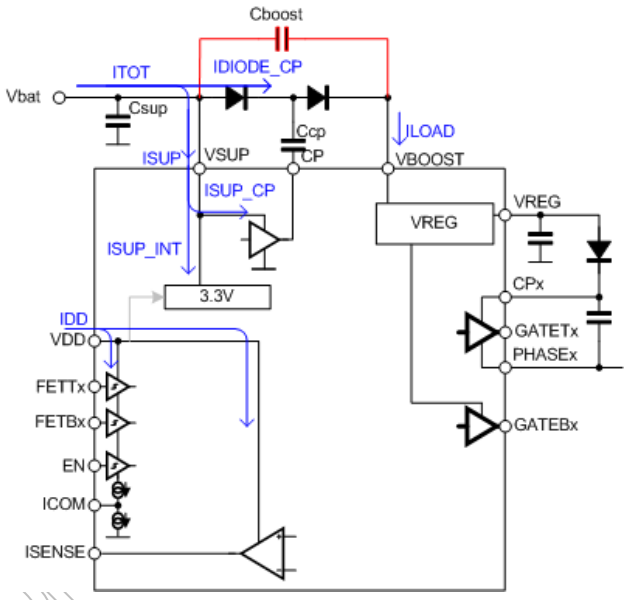


Figure 7. Supply system, CPMODE=1

The supply for the IC operation is supplied via VSUP and VDD:

- VDD supplies the IO's, and the amplifier.
  - Mind when supplying VDD with a limited output impedance (for instance from a microcontroller IO) that the performance of the amplifier may be affected.
- VSUP supplies the internal operation and the charge pump.

See also chapter: 8.8 Charge pump.

8.2 Sleep mode

Sleep mode is activated when the supply input VDD is pulled below VDDsleepL.
In sleep mode the current consumption on VSUP is reduced to Issleep.

Pin	State in sleep mode	Input/Output
FETTX, FETBX, EN, VREF, ICOM	Input pins, supplied from VDD.	GND
ISENSE	Supplied from VDD	GND
VREG	Supply regulator is disabled	GND
VBOOST, HSD	Externally connected to supply	~VBAT
CP	Charge pump is disabled	GND
CPX	Any charge that remains after VREG is disabled will leak to ground	GND
GATETX PHASEX	**VSUP>4.5V** In sleep mode gate-discharge-resistors (Rsgd) between GATETX and PHASEX are activated (see chapter 8.7.2 FET driver during sleep mode)	GND
GATEBX	**VSUP>4.5V** In sleep mode gate-discharge-resistors (Rsgd) between GATEBX and DGND are activated. (see chapter 8.7.2 FET driver during sleep mode)	GND

Table 4. State of IC during sleep mode

Note:

- In case input pins are externally pulled high while VDD LOW, current will flow into VDD via internal ESD protection diodes. This condition is not allowed.
- When VDD is pulled low, also ICOM will go low. This should not be interpreted as a diagnostic interrupt.

8.2.1 Sleep mode status overview

Name	Type	State in sleep mode
IBM	LV Analog input	GND
IBP	LV Analog input	GND
ISENSE	LV Analog output	GND (tied to VDD)
FETB1	LV Digital input	GND (tied to VDD)
FETB2	LV Digital input	GND (tied to VDD)
FETB3	LV Digital input	GND (tied to VDD)
ICOM	LV IO	GND (tied to VDD)
EN	LV IO	GND (tied to VDD)
PHASE2	HV output	Connected via Diode to GATE2
GATET2	HV output	Internal pull down (Rsgd) to GND
CP2	HV input	Any present charge leaks to GND
PHASE1	HV output	Connected via Diode to GATE1
GATET1	HV output	Internal pull down (Rsgd) to GND
CP1	HV input	Any present charge leaks to GND
PHASE3	HV output	Connected via Diode to GATE3
GATET3	HV output	Internal pull down (Rsgd) to GND
CP3	HV input	Any present charge leaks to GND
VBOOST	HV input	Connected via CP diodes to VBAT
VREG	HV output	GND
GATEB2	HV Output	Internal pull down (Rsgd) to GND
GATEB3	HV Output	Internal pull down (Rsgd) to GND
GATEB1	HV Output	Internal pull down (Rsgd) to GND
DGND	Ground	Driver ground
CP	HV Output	GND
VSUP	HV Supply input	Power supply input
VBATF	HV input	Connected to supply
AGND	Ground	Analog ground
FETT2	LV Digital	GND (tied to VDD)
FETT1	LV Digital	GND (tied to VDD)
FETT3	LV Digital	GND (tied to VDD)
VDD	LV Supply input	Externally pulled low
VREF	LV Analog input	GND

Table 5. Pin definitions and descriptions

8.3 Enable input

Pulling the Enable input (EN) low forces the pre-driver to pull all FET gate voltages to ground, switching off all external transistors (high impedance). While EN is low, the programming of the EEPROM via SPI can be initiated by pulling ICOM low for a time Tspi_su.

8.4 Protection and diagnostic functions

8.4.1 Drain-source voltage monitoring

The MLX8320x provides a drain-source voltage monitoring feature for each external FET to protect against short circuits. This drain-source voltage monitoring comparator can be enabled/disabled in EEPROM.

The drain-source voltage monitor for a certain external FET is only active when the corresponding input is set to “on” and the dead time is over. An additional blanking time can be programmed in EEPROM. If the drain-source voltage stays higher than the VDS monitor threshold voltage, the VDS error is raised. This threshold voltage is configurable in EEPROM.

The reaction of the pre-driver on a VDS error can be configured in EEPROM with the Bridge Feedback bit. If this bit is set the pre-driver will automatically disable the drivers when a VDS error is detected. If not set the pre-driver remains active. In any case the VDS error will be reported.

VDS_COMP_EN	VDS_BF_EN	Pre-driver reaction on error event
0	x	Any drain-source over voltage event is ignored and no error is reported on ICOM.
1	0	VDS_ERR is reported on ICOM, but the pre-driver remains active.
1	1	VDS_ERR is reported on ICOM and the pre-driver is disabled.

Table 6. Pre-driver reaction on VDS error

8.4.2 Programmable dead time

The pre-drivers’ internal implementation guarantees that low side and high side of the same external half bridge can not be “on” at the same time connecting supply directly to ground. See Figure 12 for this internal implementation of the pre-driver. The pre-driver also provides a programmable dead time in EEPROM.

8.4.3 Supply overvoltage shutdown

The pre-driver has an integrated VSUP over voltage shut down to prevent destruction of the pre-driver at high supply voltages. A VSUP_OV event will always switch off the pre-driver, this reaction can not be masked.

8.4.4 Regulated supply overvoltage shutdown

The pre-driver has an integrated VREG over voltage shut down. The reaction of the pre-driver on this VREG_OV depends on the status of the Bridge Feedback bit in EEPROM. If this VREG_OV_BF_EN bit is set the pre-driver will pull all gate voltages low, switching off all external FETs.

VREG_OV_BF_EN	Pre-driver reaction on error event
0	VREG_OV is reported on ICOM, but the pre-driver remains active.
1	VREG_OV is reported on ICOM and the pre-driver is disabled.

Table 7. Pre-driver reaction on VREG_OV

8.4.5 Undervoltage warnings

Comparators are implemented to detect an under voltage on VSUP, VBOOST, VREG, VDD and VGS. If an under voltage is detected, it will be reported to the MCU. It is the responsibility of the user to take action to assure functional operation.

8.4.6 Over temperature warning

If the junction temperature exceeds the specified threshold, a warning will be communicated to the MCU. The pre-driver will continue in normal operation. It is the responsibility of the user to protect the IC against over temperature destruction.

8.4.7 EEPROM error warning

To ensure reliable communication with EEPROM the pre-driver provides an automatic single bit error correction. If two bits in the addressed word are bad the EEPROM gives the EEP_ERR warning, indicating a double error was detected.

8.4.8 ICOM diagnostics interface

ICOM is a serial interface that feeds back detailed diagnostics information to the MCU over a single wire. In normal operation, when no error is detected, ICOM is high. When an error is detected the pre-driver will inform the MCU via a PWM duty cycle on ICOM. It is the responsibility of the MCU to catch the ICOM duty cycle and disable the driver if necessary, by pulling EN low.

Each error corresponds to a duty cycle with a 5 bit resolution. The duty cycle is transmitted until the MCU acknowledges the reception of the duty cycle.

For the MCU to acknowledge the error, it should be able to keep the line low while ICOM is pulling the line high, for a period $T_{Ack} > T_{ICOM}$. At each ICOM falling edge the pre-driver checks the actual voltage on ICOM to detect an acknowledgement. When an acknowledgement is detected the PWM duty cycle is changed to the corresponding duty cycle of the next error to be transmitted.

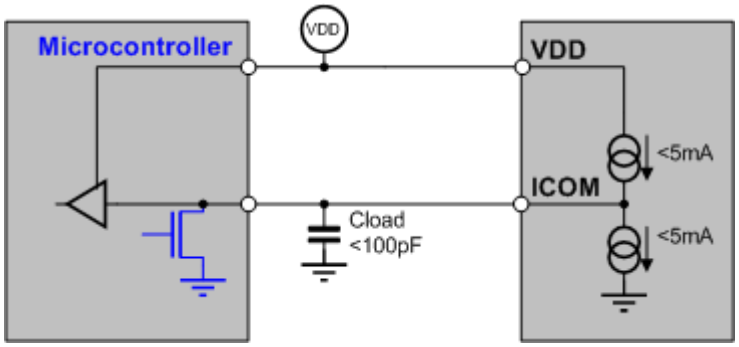
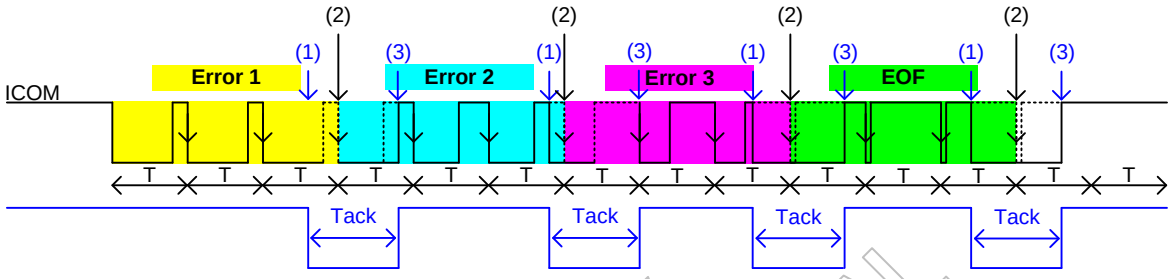


Figure 8. ICOM diagnostics interface

This sequence of capturing duty cycle and acknowledging continues until all error duty cycles are communicated and the End Of Frame (EOF) duty cycle is being transmitted. By acknowledging this EOF all error latches are reset and the ICOM line goes high again, until a new error is detected.



(1): MCU pulls ICOM low
(2): MLX8320x detects acknowledge on falling edge
(3): MCU releases ICOM line

Figure 9. ICOM serial interface for diagnostics information over a single wire

In case multiple errors occur at the same time, priority is defined: 0 is the highest priority and 16 is the lowest priority. See Table 8 for an overview of all error conditions that are monitored, the corresponding PWM duty cycle and the priority.

Priority	Input error code	% Duty cycle	Debounce time	Description
16	ICOM_EOF	93.5	n/a	End of frame
9	EEP_ERR	55.0	n/a	EEPROM DED error
8	VDD_UV	49.5	8us	VDD Under Voltage
7	VSUP_OV	44.0	2us	VSUP Over Voltage
6	VSUP_UV	38.5	8us	VSUP Under Voltage
5	OVT	33.0	2us	OVT (over temperature)
4	VREG_UV	27.5	16us	VREG Under Voltage
3	VGS_UV	22.0	2us	Vgs Under Voltage *This event can be masked by setting VGS_UV_COMP_EN=0*
2	VBOOST_UV	16.5	16us	VBOOST Under Voltage
1	VREG_OV	11.0	2us	Voltage regulator over voltage *This event can be masked by setting VREG_OV_BF_EN=0*
0	VDS_ERR	5.5	2us	Vds Error =VDS_T1 || VDS_T2 || VDS_T3 || VDS_B1 || VDS_B2 || VDS_B3 *Can be Masked by VDS_COMP_EN* *To avoid erronous triggering due to switching there is a programmable blanking time on top of the debounce time: VDS_BLANKTIME[1:0].*

Table 8. Overview diagnostic errors over ICOM

Two modes for supplying diagnostic feedback to the MCU are possible and can be set in EEPROM.
The first mode is the slow response diagnostic mode and uses a larger PWM period to communicate diagnostics information to the MCU over ICOM.
The second mode is the fast response diagnostic mode and uses a PWM period that is ~8 times smaller. This fast mode allows the fastest response time of the interrupt routine form the external MC, but also implies the MCU needs to be fast enough in order to be able to capture the duty cycle. For the fast response diagnostic mode the MCU clock needs to be minimum 20MHz.

Note:

- The different diagnostic feedback modes (slow/fast) are applicable independent of the configuration of the internal hardware protection features.
- When VDD is pulled low to put the pre-driver in sleep mode ICOM will go low as well. As soon as VDD goes high, ICOM will go high as well and remains high. No EOF may be required.
- At POR it is possible that the voltages on VSUP, VBOOST and VREG have not been achieved (dut to charging of the external capacitors) and thus it is possible ICOM may immediately go in diagnostic mode. This implies the MCU has to acknowledge these errors until the under voltage conditions have been resolved. As soon as the EOF duty cycle is acknowledged and ICOM remains high, the pre-driver is ready for normal operation.

8.4.9 Pre-driver output state summary

Below table shows all conditions due to which the pre-driver may be disabled:

The pre-driver is disabled (high-impedance state)	The Pre-driver is released again
As soon as an error condition appears for which the hardware protection is activated • VSUP_OV • VDS • VREG_OV	As soon as the EOF has been acknowledged.
As soon as VDD = LOW	As soon as VDD = HIGH
As soon as EN = LOW	As soon as EN = HIGH

Table 9. Pre-driver output summary

8.5 EEPROM programming

- The EEPROM data can be programmed during customer production testing by using a PTC-04, or by the microcontroller via an SPI interface. The pre-driver is programmed with default settings per table below.
- The EEPROM features single error correction and double error detection.
- **Note:** SPI_Address[6] == SPI_Address[7] == SPI_Address[5]

8.5.1 Memory map

SPI Address[2:0]	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
0	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
1	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
2	DEAD_TIME[2:0]			VDSMON[2:0]			CPMODE	Res.
3	VDS_BLANK_TIME[1:0]		PWM_SPEED	Res.	CUR_GAIN[2:0].			Res.
4	VREG_OV_BF_EN	VDS_BF_EN	VDS_COMP_EN	VGS_UV_COMP_EN	EN_TCP	EN_CP	Res.	Res.
5	SPI_EN	1	Res.	Res.	Res.	Res.	Res.	Res.

Table 10. Memory map EEPROM

Bit name	Description	Default
Driver configuration		
DEAD_TIME[2:0]	Defines the DEAD TIME between the HS FET and LS FET of the same phase	011
VDSMON[2:0]	Defines the detection threshold level of the Vds monitoring	111
VDS_BLANK_TIME[1:0]	Defines the duration of the Vds monitor blanking time after the on-transition of the FET	10
CUR_GAIN[2:0]	Defines the gain of the current sense amplifier	011
CPMODE	1: VBOOST voltage is regulated relative to VSUP. 0: VBOOST voltage is regulated relative to ground	0
IC configuration		
SPI_EN	When set, the SPI block is enabled. When reset, no SPI possible. (In SPI mode this value can only be programmed from 1 to 0, not from 0 to 1)	1
VREG_OV_BF_EN	VREG Over voltage Bridge Feedback Enable 1: When VREG_OV=1 → Bridge driver is SET in tri-state 0: When VREG_OV=1 → No effect on Bridge driver.	1
VDS_BF_EN	VDS Bridge Feedback Enable 1: When VDS_ERR=1 → Bridge driver is SET in tri-state 0: When VDS_ERR=1 → No effect on Bridge driver.	1
VDS_COMP_EN	1: VDS comparator enabled 0: VDS comparator disabled	1
VGS_UV_COMP_EN	1: VGS_UV comparator enabled 0: VGS_UV comparator disabled	1
PWM_SPEED	1: PWM = FICOMF 0: PWM = FICOMS	0
EN_CP	1: enables boost charge pump 0: disables boost charge pump	1
EN_TCP	1: enables trickle charge pump 0: disables trickle charge pump	0
OUT_RESERVE_RG	Undefined	0

Table 11. EEPROM bits

8.5.2 SPI communication

When the chip is in SPI mode the EEPROM is programmable and readable via the SPI port.

8.5.2.1 Entering / exiting SPI mode

The MLX83203 will enter from NORMAL mode into SPI mode when ALL below conditions are present:

- EN = 0
- All FETTx = low AND all FETBx high (all FET inputs are disabled)
- ICOM:
  - Any pending errors have been acknowledged
  - A Low Level pulse is applied on ICOM between 256us (2048/FOSC) and 512us (4096/FOSC)

The chip will return from SPI MODE to NORMAL MODE when

- EN = 1.

This means that

- any ongoing EEPROM writes will be completed
- the EEPROM state machine will copy all EEPROM contents into registers

During this time the ICOM pin will be kept low.

Similar to when the MLX83203 comes out of POR, after leaving SPI MODE and returning to NORMAL MODE, the MLX83203 will be blocked until the data have been copied to the registers. This assures that all chip parameters are set correctly before starting.

Note: It only makes sense for the MCU to call for SPI if all errors are clear and acknowledged.

8.5.2.1 SPI protocol

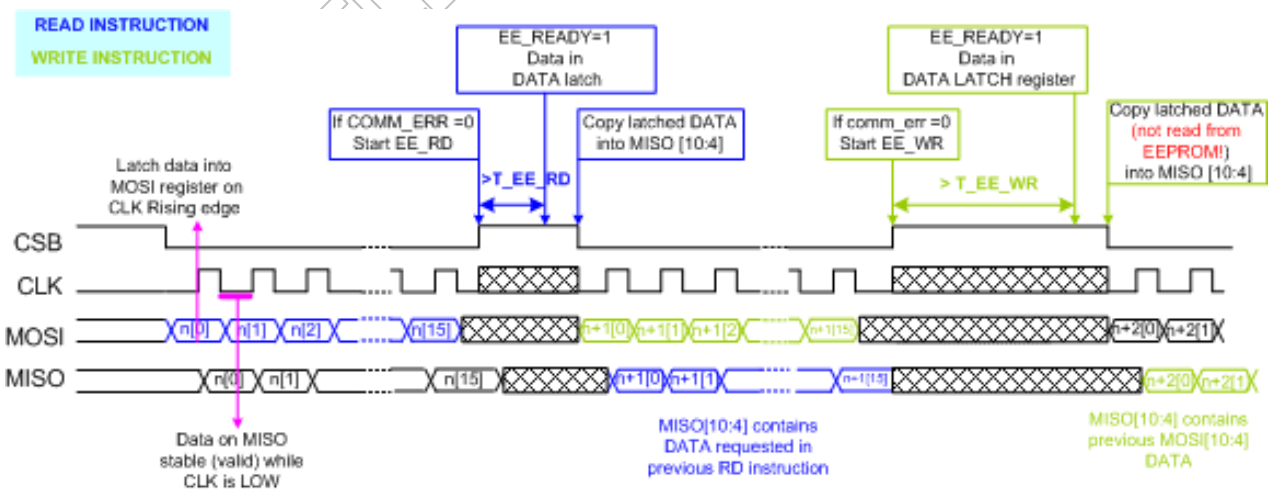


Figure 10. SPI waveform example for read and write (LSB first)

The 16 bit MISO/MOSI shift registers are controlled via 4 pins which are shared with other functions:

Pin	SPI signal	Comment
FETB1	MISO	The signal on the MISO output is guaranteed to be stable while CLK is low
FETB2	CLK	Clock input
FETB3	MOSI	The MOSI shift register is reading in data on the rising edge of CLK

ICOM_IN	CSB	Frames are defined by CSB low and have to consist of 16 clock pulses on CLK.
		On the rising edge of CSB:
		• If COMM_ERR=0 the read/write action is started as requested in the previous frame.
		• Else (COMM_ERR = MISO[14]=1): a communication error is detected. No action will occur (EE_READY latch will remain 0). This can be:
		  ◦ Either due to a parity bit failure: MOSI[15] in frame N was incorrect.
		  ◦ Or because less or more then 16 rising edges were received during CSB low of frame N
		
		CSB has to remain high until the read (T_EE_RD) / write (T_EE_WR) action is completed.
		In this case EE_READY= MISO[13] bit in the next frame will be high
		Else IF CSB goes low before the requested action is completed
		• EE_READY= MISO[13] bit in the next frame will be low.

Table 12. SPI signals

8.5.2.2 SPI registers

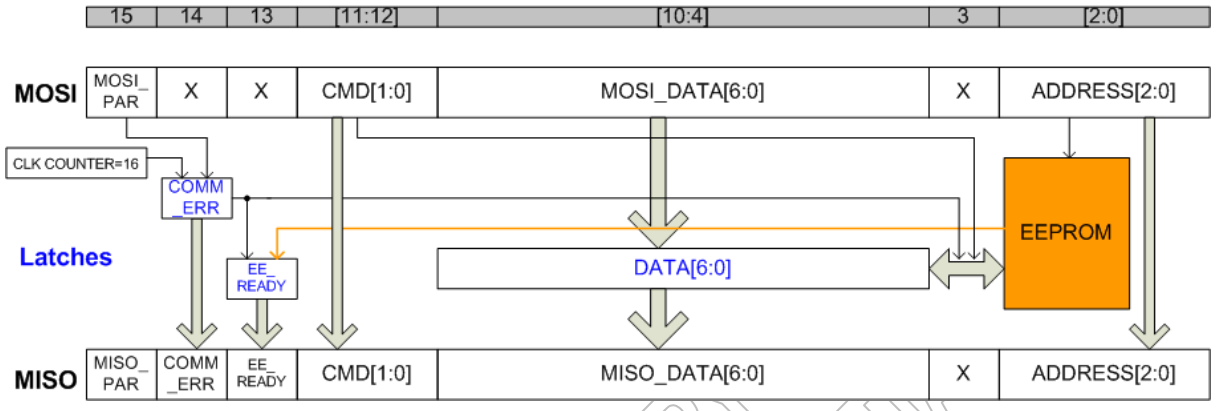


Figure 11. SPI REGISTERS and relation to internal Data latches

MOSI							
Bit[7]	**Bit[6]**	**Bit[5]**	**Bit[4]**	**Bit[3]**	**Bit[2]**	**Bit[1]**	**Bit[0]**
MOSI_DATA [3:0]				x	Address [2:0]		
Bit[15]	**Bit[14]**	**Bit[13]**	**Bit[12]**	**Bit[11]**	**Bit[10]**	**Bit[9]**	**Bit[8]**
Mosi_Parity	x	x	CMD [1:0] 00: EE_RD 01: EE_WR 10: EE_RDAW1 11: EE_RDAW2		MOSI_DATA [6:4]		
MISO							
Bit[7]	**Bit[6]**	**Bit[5]**	**Bit[4]**	**Bit[3]**	**Bit[2]**	**Bit[1]**	**Bit[0]**
MISO_DATA [3:0] (*)				x	The content from previous MOSI[2:0]		
Bit[15]	**Bit[14]**	**Bit[13]**	**Bit[12]**	**Bit[11]**	**Bit[10]**	**Bit[9]**	**Bit[8]**
Miso_ Parity	COMM_ERR	EE_READY	The content from previous MOSI[12:11]		MISO_DATA [6:4] (*)		

Table 13. SPI registers description

(*) MISO_DATA [10:4]	**Comment**
IF MOSI(N)[11:12] = EE_WR (Write command) THEN MISO(N+1)[10:4] = MOSI(N)[10:4] from previous WR instruction	The data received via MOSI have been shifted into the MISO register. This allows the MCU to verify the correct data have been transmitted. In order to verify if the data have been correct stored into the EEPROM, a dedicated read command is required.
ELSE ; MOSI(N)[11:12] <> EE_WR MISO(N+1)[10:4] = EEPROM(address=MOSI(N)[2:0])	In case a read command is received, the data in the MISO register have been copied out of the designated address in the EEPROM. Mind that 3 read consecutive read commands have to be successful to ensure retention time.

8.5.2.3 Bit definition

Bit	Comment
MISO_PAR **MOSI_PAR**	Odd parity of the actual data. So respectively the odd parity of the actual MOSI data, or the odd parity of the actual MISO data.
EE_READY	0: EE_WR or EE_RD command were not completed when the new frame was started (on the falling edge of CSB) 1: No EE_WR or EE_RD activity ongoing on falling edge of CSB
COMM_ERR	1: Communication error occurred during the previous MOSI message. Possible errors: • Parity bit failure • Less or more the 16 rising edges received during CSB low 0: Previous dataframe was received ok: no communication error
CMD [1:0]	**EE_RD, EE_RDAW1, EE_RDAW2**: 1. A MOSI frame is sent with command: MOSI[12:11] = EE_RD (below is also applicable for EE_RDAWx). 2. CSB is kept high long enough (>T_EE_RD) to ensure the read command can be completed. (else EE_READY will be 0 in next MISO frame) 3. The requested data will be transmitted in the next MISO frame. 4. The data in this frame is valid in case a. COMM_ERR = 0 (there was no comm. error during the previous MOSI frame) b. EE_READY =1 (the read command was completed on the falling edge of CSB) c. MISO [15] has the correct parity. **EE_WR** 1. A MOSI frame N is sent with MOSI[12:11] = EE_WR. 2. CSB is kept high long enough (>T_EE_WR) to ensure the write command can be completed. (else EE_READY will be 0 in next MISO frame) 3. The received data are used in the next MISO frame as a first verification step in a total of 3 steps need to verify if the EE_WR was successful. a. *Verification of the N+1 MISO frame*. The N+1 MISO frame should have. i. COMM_ERR = 0 (there was no comm. error during the previous MOSI frame) ii. EE_READY =1 (the EE_WR command was completed on the falling edge of CSB) iii. MISO[15] has the correct parity. iv. MISO_DATA(N+1) = MOSI_DATA(N) *b. Verification step2: EE_RDAW1:* The N+1 MOSI frame should have CMD = EE_RDAW1 Then the N+2 MISO frame should have. i. COMM_ERR = 0 (there was no comm. error during the previous MOSI frame) ii. EE_READY =1 (the EE_WR command was completed on the falling edge of CSB) iii. MISO[15] has the correct parity. iv. MISO_DATA(N+2) = MOSI_DATA(N) *c. Verification step3: EE_RDAW2:* The N+2 MOSI frame should have CMD = EE_RDAW2 Then the N+3 MISO frame should have. i. COMM_ERR = 0 (there was no comm. error during the previous MOSI frame) ii. EE_READY =1 (the EE_WR command was completed on the falling edge of CSB) iii. MISO[15] has the correct parity. iv. MISO_DATA(N+3) = MOSI_DATA(N) Conclusion: in total 3 MOSI frames should be generated to ensure successful writing of data.

8.6 Current sense amplifier

The sense amplifier offers low input offset, and fast settling times. Its input range can be adjusted by applying a suitable voltage on the VREF pin, typically as a resistor divider from VDD to GND. For the definition of VREF, the input offset, the current range, and the linear output range of the ISENSE pin should all be taken into account.

For input signal:

Vin = Visp - Visn,
Max input offset: Voffsetmax = Vis_iomax + Trange * Vis_io_tdrift
(over full temperature range =Trange)

Visense = (Vin +/-Voffset)*IS_Gain + VREF has to be in the range [V_ISENSEmin, V_ISENSEmax]

- ⇨ Imin = [(Visensemin – VREF) / IS_GAIN + Voffset] / Rshunt
- ⇨ Imax = [(Visensemax – VREF) / IS_GAIN - Voffset] / Rshunt

Input offset voltage	Vis_io
Input offset voltage thermal drift	Vis_io_tdrift
Closed loop gain	IS_GAIN
ISENSE Output voltage range HIGH	V_ISENSEmax
ISENSE Output voltage range LOW	V_ISENSEmin

The below table shows the current input range (Amp) for two resistive divider settings on VREF:

1) VREF = VDD/2 for a symmetrical input range
2) VREF = VDD/18 for a maximum current level, while ensuring it is possible to measure the input offset before starting the motor (Isense_min > 0A).

Remark: for ease of calculation a max temperature offset drift of 1mV was added to the 5mV offset
=> max input offset = 6mV

VDD	3.3	3.3	3(**)	3(**)	5	5	4.5(**)	4.5(**)
Visensemin	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02
Visensemax	3.28	3.28	2.98	2.98	4.98	4.98	4.48	4.48
div	2	18	2	18	2	18	2	18
VREF	1.65	0.18	1.50	0.17	2.50	0.28	2.25	0.25

Voffset **0.006**

Isense min. **1** **mOhm**

gain	DIV2	DIV18	DIV2	DIV18	DIV2	DIV18	DIV2	DIV18
8	-198	-14.4	-179	-12	-304	-26.2	-273	-23
10.3	-152	-9.9	-138	-8	-235	-19.0	-211	-16
13.3	-117	-6.3	-105	-5	-180	-13.4	-162	-11
17.2	-89	-3.5	-80	-3	-138	-9.0	-124	-7
22.2	-67	-1.4	-61	-0.6	-106	-5.6	-94	-4
28.7	-51	0.3(*)	-46	0.9(*)	-80	-3.0	-72	-2
37.0	-38	1.6(*)	-34	2.0(*)	-61	-1.0	-54	0
47.8	-28	2.6(*)	-25	3(*)	-46	0.6	-41	1

Isense max.

gain	DIV2	DIV18	DIV2	DIV18	DIV2	DIV18	DIV2	DIV18
8	198	381	179	346	304	582	273	523
10.3	152	295	138	267	235	451	211	405
13.3	117	227	105	206	180	348	162	312
17.2	89	174	80	158	138	267	124	240
22.2	67	133	61	121	106	206	94	185
28.7	51	102	46	92	80	158	72	141
37.0	38	78	34	70	61	121	54	108
47.8	28	59	25	53	46	92	41	82

Table 14. Sense amplifier current ranges in Amp. Examples for 1mOhm shunt

Note:

- (*) Applying a GAIN of 28.7 or higher with DIV 18 for 3.3V does not allow the measure the input offset
- (**) examples taking a 10% supply variation into account.

8.7 FET driver implementation

8.7.1 Normal operation

The top side FET drivers are bootstrapped drivers. Each of the 6 external FET transistors can be controlled directly via the 6 digital inputs. The 6 external FET transistors (or 3 half bridges) can also be controlled with only 3 digital input signals. This can be done by connecting the FETTi to VDD and control the 3 phases via the FETBi inputs. In this mode the MLX83203 will automatically generate the programmed dead times. Figure 12 shows the internal implementation of the driver stage from input to output.

The drain source voltage VDS as well as the gate voltage VGS are monitored to ensure fail safe operation. The FET gate outputs are all pulled low by pulling EN low.

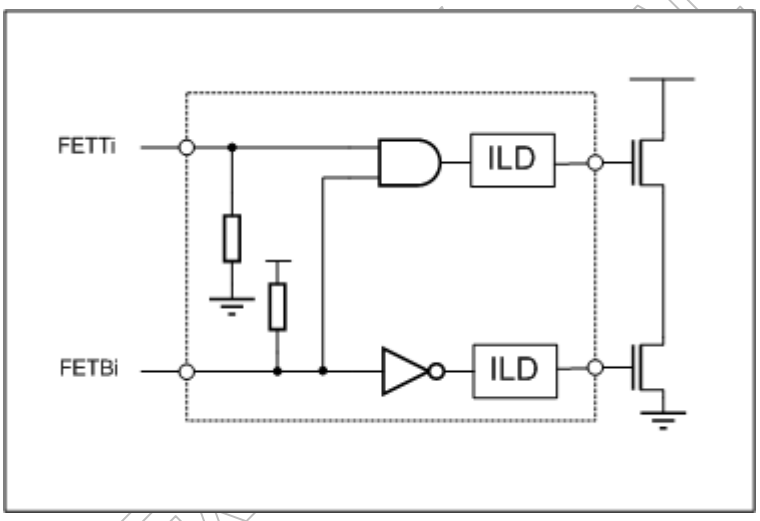


Figure 12. Internal implementation of the driver stage

8.7.2 FET driver during sleep mode

When the MLX83203 is in sleep mode a gate discharge resistance (Rsgd~1kOhm) is activated which ensures the FET gates remain fully in OFF state.

Note that is the responsibility of the microcontroller to ensure all gate voltages are low, for instance by setting the EN input low, prior to switching to sleep mode.

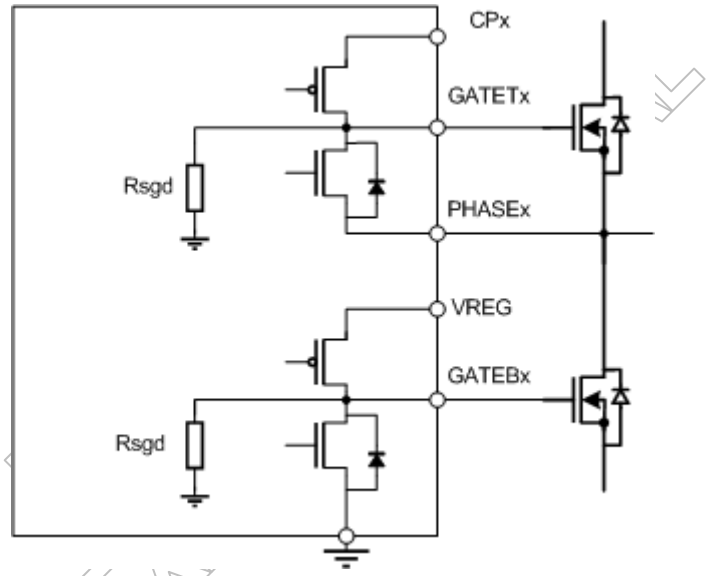


Figure 13. State of pre-driver in sleep mode

Figure 13 PHASEx is kept low with GATETx through the internal body diode of the pre-driver.

8.8 Charge pump

EEPROM configuration bits		Default
CPMODE	1: VBOOST voltage is regulated relative to VSUP. 0: VBOOST voltage is regulated relative to ground	0
EN_CP	1: enables boost charge pump 0: disables boost charge pump	1

Table 15. CP configuration in EEPROM

Standard operation of the Charge pump (CPMODE=0) is to ensure sufficient gate voltage to the bootstrap capacitors in case of low battery voltage conditions. In this case VBOOST is regulated compared to GND level. The charge pump will not be switching when VSUP > VREG + 2* Vf, with Vf= forward voltage of the charge pump diodes.

Alternatively (CPMODE=1) the charge pump can regulate VBOOST compared to VSUP. In this case the Cboost cap should be connected to VSUP to ensure any supply variations are coupled to the VBOOST level. In this case VBOOST can be applied to drive a high side reverse polarity NFET.
The disadvantage is an additional amount of dissipation inside the driver to regulate VREG.

8.9 100% PWM with bootstrap

A current is drawn from the CP bootstrap pin to the phase pins. This current will discharge the gate voltage on top of any external pull down gate resistance. The below tables show some calculation examples.

bootstrap	330	nF
Vreg	12	V
Qbootstr	3960	nC
QFET	200	nC
Vgs_initial	**11.4**	**V**
Rcp_leak	0.75	Mohm
leakage	15	uA
On time	60	ms
Qleak	914	nC
Vgs_end	**9.4**	**V**
Vgs drop	**2.06**	**V**

bootstrap	100	nF
Vreg	12	V
Qbootstr	1200	nC
QFET	120	nC
Vgs_initial	**10.9**	**V**
leakage	15	uA
On time	10	ms
Qleak	152	nC
Vgs_end	**9.8**	**V**
Vgs drop	**1.13**	**V**

This gate leakage will limit the maximum state time during which 100% PWM can be applied.

9 Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020

Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)

- EIA/JEDEC JESD22-A113

Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20

Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat

- EIA/JEDEC JESD22-B106 and EN60749-15

Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21

Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website:
http://www.melexis.com/quality.asp

10 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

11 Package Information

11.1 Package data QFN32 (5x5, 32 leads)

	A	A1	A3	b	D/E	D2/E2	e	K	L	N
min	0.80	0.00	0.20 REF	0.18	5.00 B.S.C	3.50	0.50 B.S.C	0.2	0.3	32
max	1.00	0.05		0.30		3.70		-	0.5	

Table 16. Mechanical Dimensions QFN32 5x5, all dimensions in mm

[1] General tolerance of D and E is +/-0.1mm
[2] Bottom pin 1 identification may vary depending on supplier

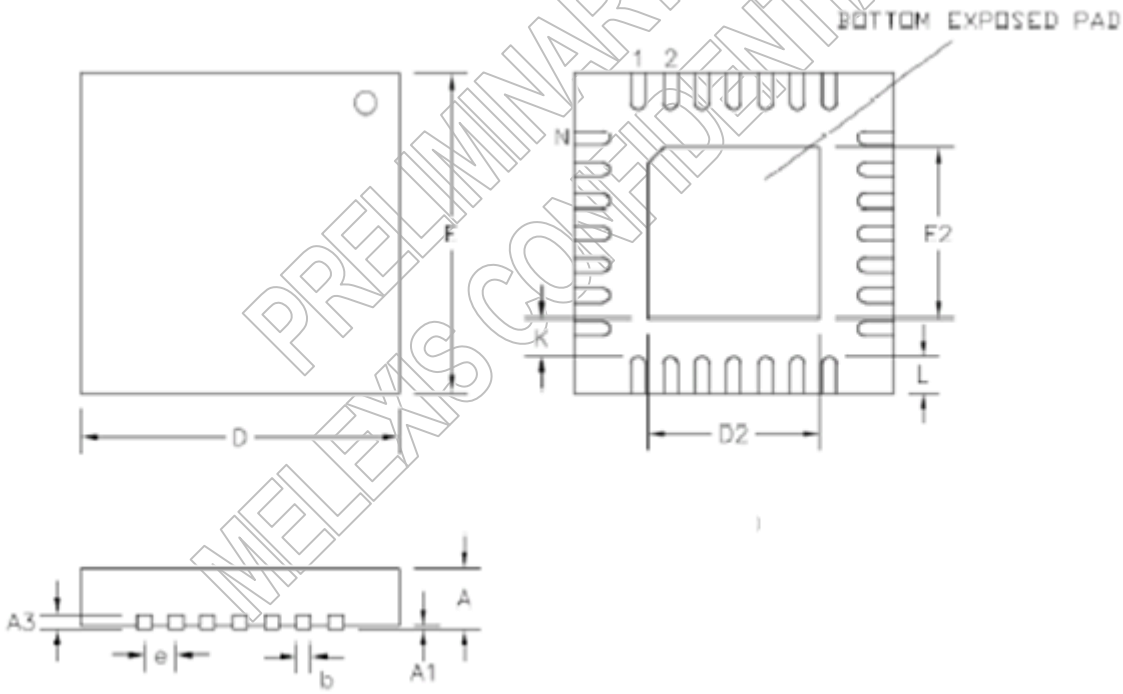


Figure 14. Package QFN32

11.2 *Package data TQFP48_EP 7x7 (48 leads, exposed pad)*

	A	A1	A2	D/E	D1/E1	D2/E2	e	L	N	b	c	α
Min	-	0.05	0.95	9.00	7.00	4.00	0.50	0.45	48	0.17	0.09	0^o
Max	1.20	0.15	1.05	B.S.C	B.S.C	B.S.C	B.S.C	0.75		0.27	0.20	7^o

Table 17. Mechanical Dimensions TQFP48_EP 7x7, all dimensions in mm

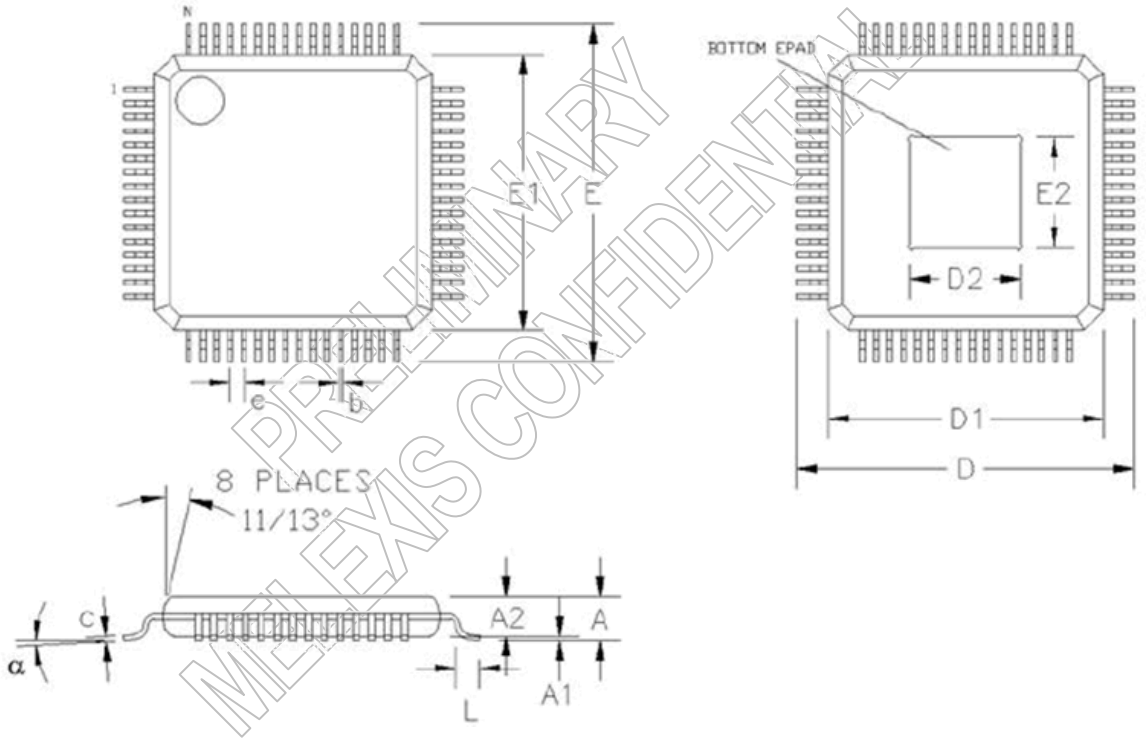


Figure 15. Package TQFP48_EP

11.3 Package Marking

Product name:	MLX8320X	X = 2 or 3
Date Code:	YYWW	year and week
Lot number	ZZZZZZZZ	format free

Top view of the package

12 Disclaimer

Devices sold by Melexis are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. Melexis makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Melexis reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with Melexis for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by Melexis for each application.
The information furnished by Melexis is believed to be correct and accurate. However, Melexis shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interrupt of business or indirect, special incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of Melexis' rendering of technical or other services.

For the latest version of this document, go to our website at
www.melexis.com

Or for additional information contact Melexis Direct:

Europe, Africa, Asia:
Phone: +32 1367 0495
E-mail: sales_europe@melexis.com

America:
Phone: +1 603 223 2362
E-mail: sales_usa@melexis.com

ISO/TS 16949 and ISO14001 Certified

13 History of changes

Revision	Author	Date	Description
1.1	DLM	1-3-12	• EE_RD meaning in SPI description corrected • RDSon specification split up in ON/OFF • Added RDSon for 83202 variant • Added package marking
1.2	DLM	28-3-12	TQFP48 pin out included
1.3	DLM	15-5-12	• Added appl. Schematics, Pin internal structures, updated block diagram • Updated SPI enabling. • Updated ICOM duty cycles • Updated sleep mode • Updated leakage spec on VBATF
			Max voltage on all pins
1.4	DLM	3-7-12	Final package dimensions.
1.5	RRR	28-11-12	• Parameters updated per test data. • Device description updated
1.6	SOE	21-12-12	• Information about DC variant of pre-driver moved to separate datasheet
1.7	SOE	15-01-13	• Protection and diagnostic functions updated • Trickle Charge Pump included
2.0	SOE	26-02-13	
2.1	SOE	06-05-13	Max voltage on phase pins updated
2.1	SOE	04-12-13	Entering SPI mode by disabling all 6x FET input signals