



August 2014

FCD1300N80Z

N-Channel SuperFET[®] II MOSFET

800 V, 4 A, 1.3 Ω



Features

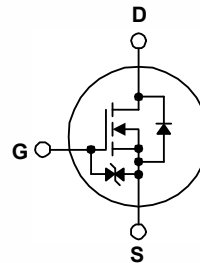
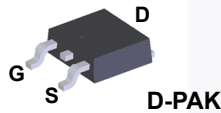
- $R_{DS(on)} = 1.05 \Omega$ (Typ.)
- Ultra Low Gate Charge (Typ. $Q_g = 16.2 \text{ nC}$)
- Low E_{oss} (Typ. $1.57 \mu\text{J} @ 400\text{V}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 48.7 \text{ pF}$)
- 100% Avalanche Tested
- RoHS Compliant
- ESD Improved Capability

Description

SuperFET[®] II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. In addition, internal gate-source ESD diode allows to withstand over 2kV HBM surge stress. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as Audio, Laptop adapter, Lighting, ATX power and industrial power applications.

Applications

- AC - DC Power Supply
- LED Lighting



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCD1300N80Z	Unit
V_{DSS}	Drain to Source Voltage	800	V
V_{GSS}	Gate to Source Voltage	- DC	± 20
		- AC ($f > 1 \text{ Hz}$)	± 30
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	4
		- Continuous ($T_C = 100^\circ\text{C}$)	2.5
I_{DM}	Drain Current	- Pulsed (Note 1)	12
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	48	mJ
I_{AR}	Avalanche Current (Note 1)	0.8	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.26	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	52
		- Derate Above 25°C	0.42
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FCD1300N80Z	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	100	

FCD1300N80Z — N-Channel SuperFET[®] II MOSFET

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD1300N80Z	FCD130080Z	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	800	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}$, Referenced to 25°C	-	0.85	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 640\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	-	250	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 0.4\text{ mA}$	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 2\text{ A}$	-	1.05	1.3	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 2\text{ A}$	-	4.5	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	661	880	pF
C_{oss}	Output Capacitance		-	22.3	30	pF
C_{rss}	Reverse Transfer Capacitance		-	0.74	-	pF
C_{oss}	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	11.4	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	48.7	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 640\text{ V}, I_D = 4\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	16.2	21	nC
Q_{gs}	Gate to Source Gate Charge		-	3.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	6.8	-	nC
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	4	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 4\text{ A}, V_{GS} = 10\text{ V}, R_g = 4.7\ \Omega$ (Note 4)	-	14	38	ns
t_r	Turn-On Rise Time		-	8.3	27	ns
$t_{d(off)}$	Turn-Off Delay Time		-	33	76	ns
t_f	Turn-Off Fall Time		-	6	22	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	4	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	12	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 4\text{ A}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	275	-	ns
Q_{rr}	Reverse Recovery Charge		-	2.9	-	μC

Notes:

1. Repetitive rating: pulse width limited by maximum junction temperature.
2. $I_{AS} = 0.8\text{ A}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 4\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature typical characteristic.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

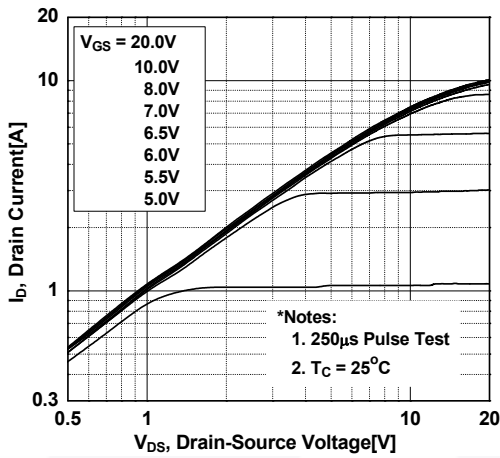


Figure 2. Transfer Characteristics

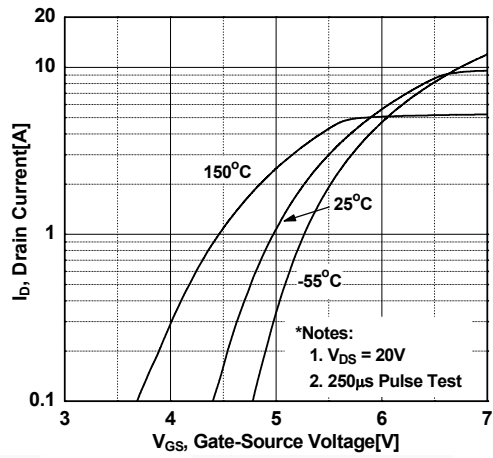


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

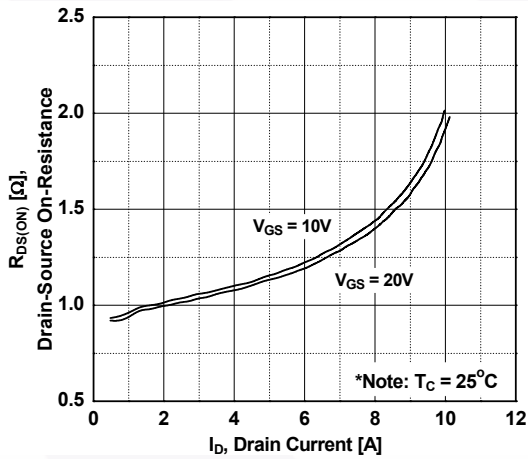


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

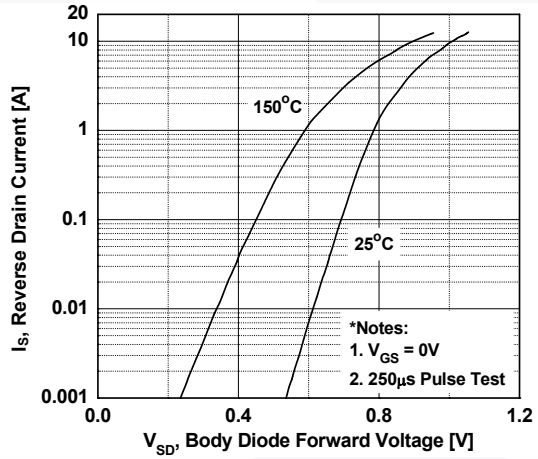


Figure 5. Capacitance Characteristics

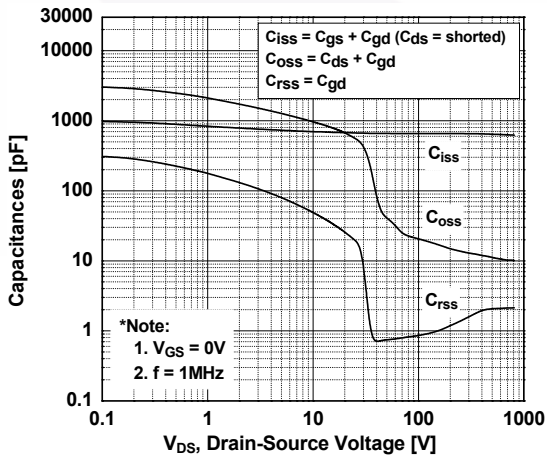
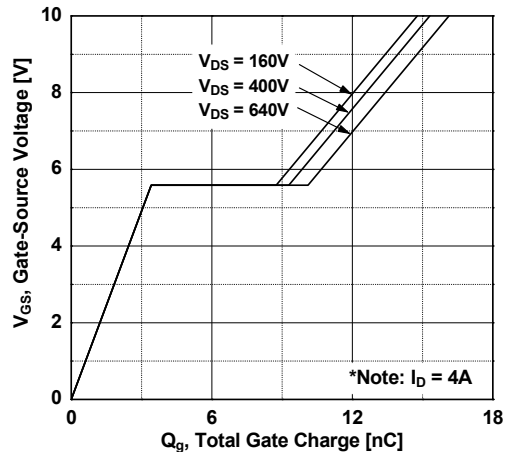


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

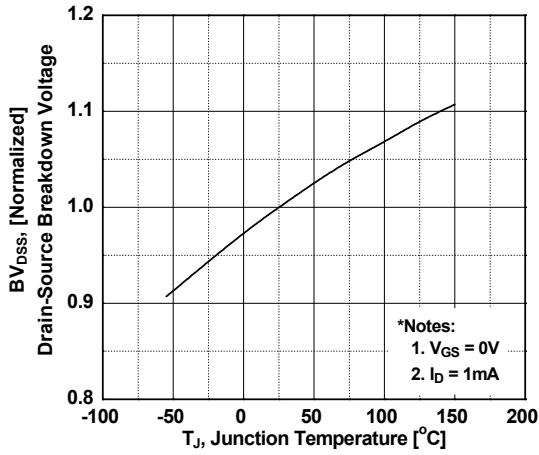


Figure 8. On-Resistance Variation vs. Temperature

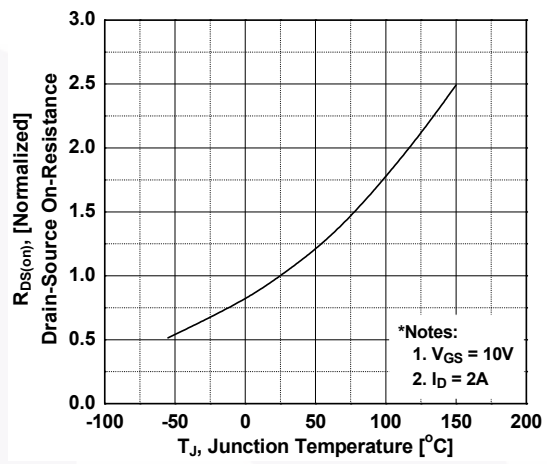


Figure 9. Maximum Safe Operating Area

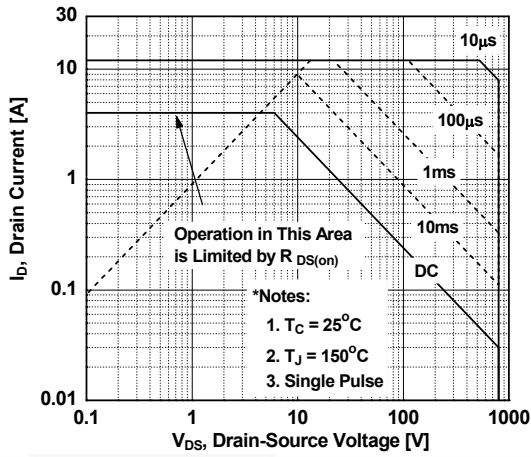


Figure 10. Maximum Drain Current vs. Case Temperature

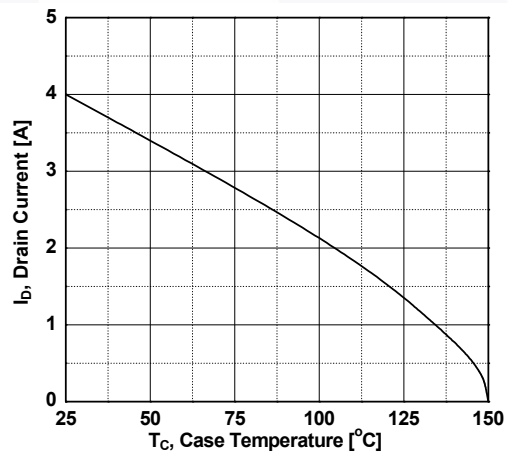
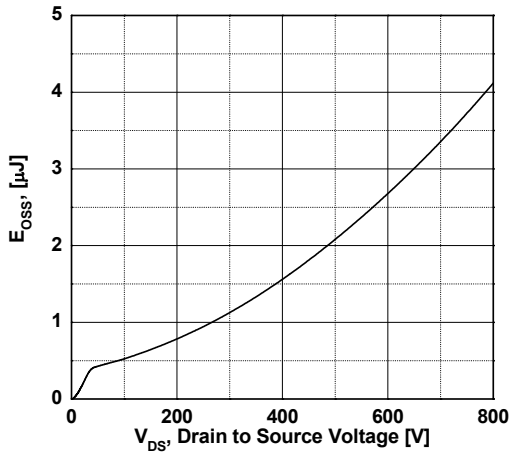


Figure 11. E_oss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve

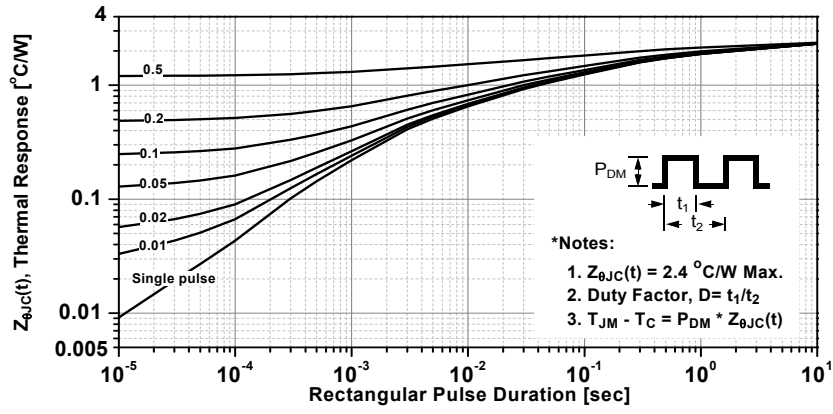




Figure 13. Gate Charge Test Circuit & Waveform



Figure 14. Resistive Switching Test Circuit & Waveforms

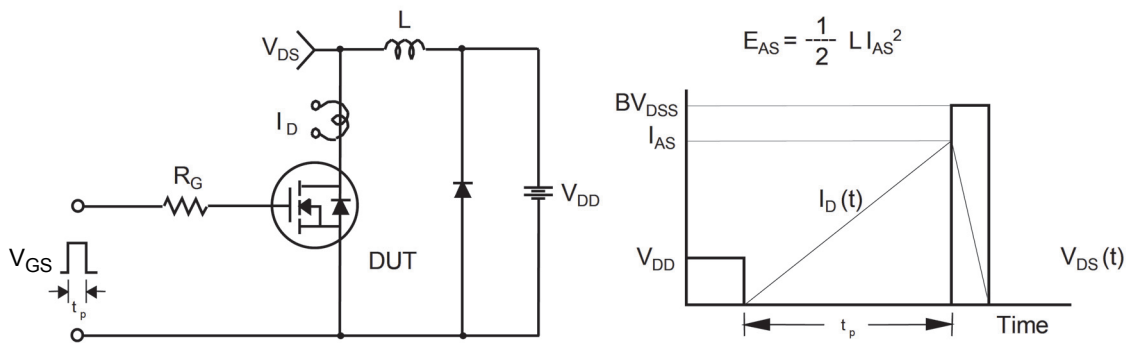
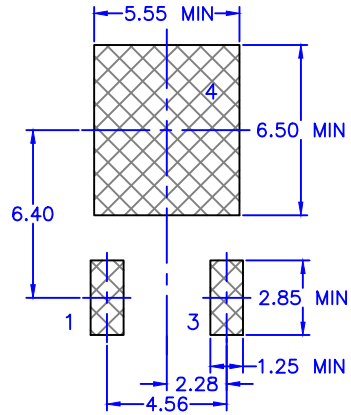
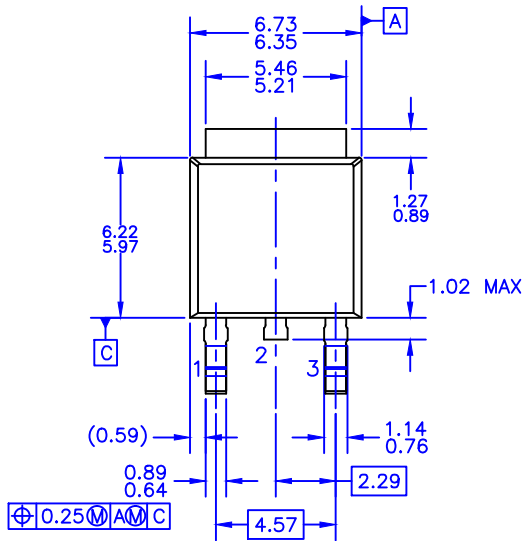


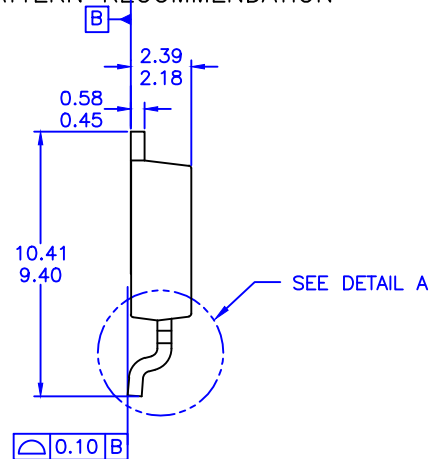
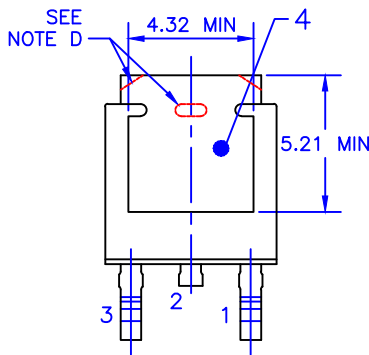
Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

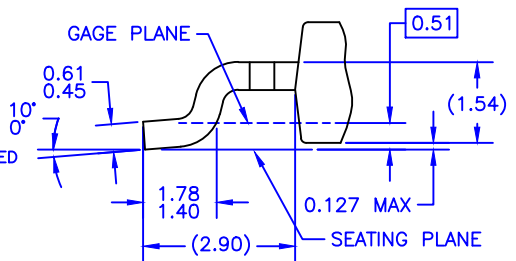


LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
- F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV9.
- I) FAIRCHILD SEMICONDUCTOR.



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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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