LOW VOLTAGE SINGLE-CHIP MICROCOMPUTER WITH BUILT-IN PRESCALER PLL FREQUENCY SYNTHESIZER AND LCD DRIVER

DESCRIPTION

The μPD1715 is a 1-chip digital tuning 4-bit CMOS microcomputer that includes a prescaler operative up to 130 MHz, a PLL frequency synthesizer, and an LCD driver (1/3 duty, 1/2 bias).

The CPU includes 4-bit parallel add and subtract functions (AD, SU, etc.), logical operations (EXL, etc.), a multi-bit test function (TMT, etc.), carry F/F set and reset functions (STC, etc.), and a timer function. The μPD1715 is manufactured in a 52-pin flat package provided with various ports. These ports include a 4-bit input/output (I/O) port controlled by input/output instructions (IN, OUT, etc.), a 1 kHz/3 kHz modulated signal output port for alarms, a variable duty port (VDP) available as a simplified D/A converter, an input port dedicated to key switch inputs, and others.

FEATURES

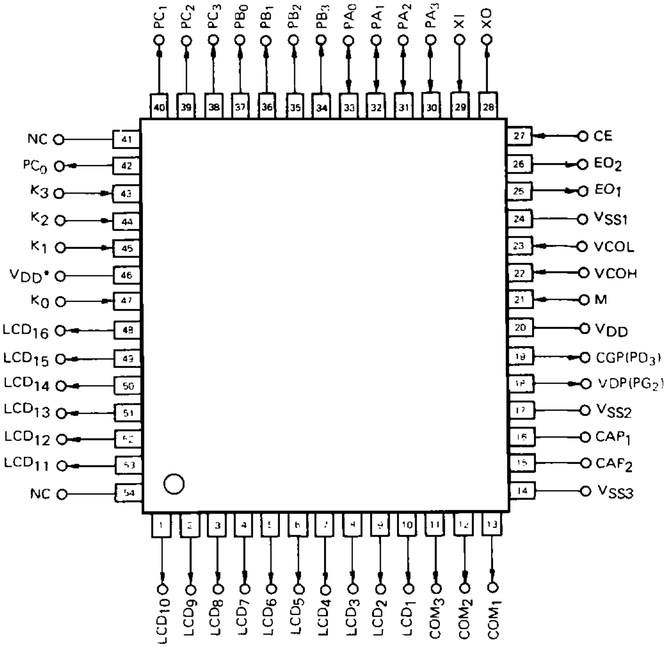
- Digital tuning 4-bit microcomputer
- Integrated prescaler (fixed 1/2 divider or 1/4 divider + two modulus prescaler: MAX. 130 MHz)
- 2.0 to 3.6 V single power source (when PLL operation)
- CMOS with low power requirement (maximum 30 μA when only CPU is resonator)
- Easy data memory (RAM) backup (via CE pin)
- Program memory (ROM): 16 bits x 1528 steps
- Data memory (RAM): 4 bits x 96 words
- 76 powerful instructions (each occupying one word)
- Instruction execution time of 40 μs (when connected to 75 kHz crystal resonator)
- Versatile add and subtract instructions (12 add and subtract instructions, respectively)
- Strong composite judge instructions (TMT ⟷ TMF, etc.)
- Storage-to-storage data transfer possible in the same row address
- Indirect register transfer (MVRD, MVRS, etc.)
- 16 useful general registers (in the RAM space)
- Stack level: 1 level
- Integrated LCD driver (1/3 duty, 1/2 bias, driven with 3.1 V, frame frequency: 100 Hz)
- Integrated Programmable Logic Array (PLA) to display LCD patterns.
- Clock can be stopped with an instruction (CKSTP).
- 14 powerful I/O ports (PA_3 to PA_0: Available for bit-unit input/output; PB_3 to PB_0, PC_3 to PC_0, VDP, CGP: Dedicated to output)
- Input ports K_3 to K_0 dedicated to key inputs
- Output ports LCD_9 to LCD_{16} dedicated to key source
- 1 kHz or 3 kHz modulated signal output port (CGP)
- Variable Duty Port (VDP) available as a simplified D/A converter
- Powerful I/O instructions (IN and OUT instructions)
- Input and output port states can be tested with TPT and TPF instructions.
- Integrated timer F/F (to be set at 125 ms intervals. The timer function can be easily executed.)
- Integrated interval pulse output (internal output): 200 Hz, duty 60 %, output at 5 ms intervals, can be tested with TIP instruction.

- PLL lock state can be tested with TUL instruetion.
- Dividing factor, dividing method, and reference frequency data can be transferred to the PLL section with a PLL instruction.
- The AM and FM frequency input pins are provided separately (maximum input frequencies: 40 MHz for VCOL pin in HF mode and 130 MHz for VCOH pin in VHF mode).
- Pulse swallowing method and direct dividing method can be selected by the program (VHF, HF, and MF modes).
- Two independent error outputs (EO_1 and EO_2 pins)
- Six reference frequencies can be selected by the program (1, 3, 5, 6.25, 12.5, and 25 kHz).

ORDERING INFORMATION

Order Code	Package
µPD1715G-XXX-22	54-pin plastic QFP
µPD1715G-XXX-21	54-pin plastic QFP (Straight lead type)
µPD1715G-XXX-24	54-pin plastic QFP (Reverse bent type)

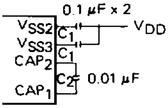
PIN CONFIGURATION (Top View)



This pin is internally connected to Pin 20.

NC No connection.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME	DESCRIPTION	OUTPUT TYPE
14 15 16 17	V_{SS3} CAP_2 CAP_1 V_{SS2}	Doubler Capacitor Connecting Pin	Used to connect the capacitors for the doubler circuit to generate the LCD drive voltage (3.1 V TYP.). Connect them as follows:  0.1 μF x 2 V_{SS2} C_1 V_{DD} V_{SS3} C_1 CAP_2 C_2 0.01 μF CAP_1	–
18	VDP	Variable Duty Port Output	Variable duty port or 1-bit output port (Port G_2). The port specification can be selected by the program. When used as the VDP, 1.12 kHz pulses are output successively. The pulse duty cycle can be changed: 64 steps as follows: $\left(\text{duty} = \frac{26.7\ \mu s}{893\ \mu s} \text{ to } \frac{867\ \mu s}{893\ \mu s} = \frac{2}{67} \text{ to } \frac{5}{67} \right)$ It can be used as a D/A converter by adding an integration circuit.	CMOS Push-pull
19	CGP	Clock Generator Output	Clock generator port or 1-bit output port (Port D_3). The port specification can be selected by the program. When used as the CGP, 1 kHz (duty 46.6 %) or 3 kHz (duty 60 %) pulses can be output successively. (See Note 2)	CMOS Push-pull
20 46	V_{DD}	Power Supply	Power source pin of the device for supplying 2.0 V to 3.5 V during PLL operation and for supplying 1.7 V to 3.6 V during CPU operation only. The voltage can be reduced up to 1.5 V for holding the internal data memory (RAM) by executing a CKSTP instruction. When the potential of this pin is changed from 0 V to 1.7 V, the power-on reset circuit of the device is activated, thereby starting the program from address 0. Note: Since pins 20 and 46 are connected in the chip, the voltage need not be supplied to both pins. The device operates with only one of these pins supplied with voltage. Note that pin 46 is not connected (NC: No Connection) for the engineering sample product (ceramic package).	–
21	M	Dividing Ratio Switching Control Signal Input	This pin is used to switch the dividing ratio of the dividing prescaler. When the VCOH pin is used, the dividing prescaler is used. When M pin is set to High level, then the frequency is divided by the 1/4 divider. Also, when M pin is set to low level, then the frequency is divided by the 1/2 divider.	Input

<table>
<tr><th>PIN NO.</th><th>SYMBOL</th><th>NAME</th><th>DESCRIPTION</th><th>OUTPUT TYPE</th></tr>
<tr><td>22</td><td>VCOH</td><td>VCO (High) Signal Input</td><td>This pin is used to input the 10 MHz to 130 MHz (M pin = High, 0.1 $V_{p\text{-}p}$ MIN.) or the 10 MHz to 100 MHz (M pin = Low, 0.1 $V_{p\text{-}p}$ MIN.) local oscillation output (VCO) and is internally connected to the programmable counter via the fixed 1/2 or 1/4 divider prescaler and 1/32 and 1/33 two-modulus prescaler.
If an HF instruction is executed in the direct dividing or pulse swallowing method, or in other words, if the VCOL pin is selected, the VCOH pin is set to the pull-down state (GND). Since an AC amplifier is included, the pertinent component must be suppressed with a capacitor before the signal is input.</td><td>Input</td></tr>
<tr><td>23</td><td>VCOL</td><td>VCO (Low) Signal Input</td><td>This pin is used to input the 0.5 MHz to 40 MHz (0.2 $V_{p\text{-}p}$ MIN.) local oscillation output (VCO).
This pin is selected when an HF instruction is executed in the direct dividing or pulse swallowing method.
Note that the different frequency upper limits and dividing factor ranges are used in these two systems.
<table>
<tr><th>Dividing method</th><th>Input voltage (min.)</th><th>Input frequency</th><th>Dividing factor</th></tr>
<tr><td>Direct dividing</td><td>0.1 $V_{p\text{-}p}$</td><td>0.5 to 15 MHz</td><td>16 to $(2^{12} - 1)$</td></tr>
<tr><td>Pulse Swallowing (HF instruction execution)</td><td>0.2 $V_{p\text{-}p}$</td><td>0.5 to 40 MHz</td><td>1024 to $(2^{17} - 1)$</td></tr>
</table>
When a VHF instruction is executed in the pulse swallowing method, which means that the VCOH pin is selected, the VCOL pin is set to the pull-down state (GND).
Since an AC amplifier is included, the pertinent component must be suppressed with a capacitor before the signal is input.</td><td>Input</td></tr>
<tr><td>24</td><td>V_{SS1}</td><td>Ground</td><td>Ground pin of the device</td><td>–</td></tr>
<tr><td>25
26</td><td>EO_1
EO_2</td><td>Error Output</td><td>PLL error output pins. If the frequency obtained by dividing the local oscillation frequency (VCO output) is higher than the reference frequency, high-level signals are output from these pins. If it is lower than the reference frequency, low-level signals are output. The floating state is set when the two frequencies are equal to each other. These outputs are delivered to an external low-pass filter (LPF), then they are applied to the varactor diode. Since the same waveform is output from EO_1 and EO_2, the user may arbitrarily select one of these pins.
When PLL disable (When setting by PLL instruction or CE pin is set to low level), EO_1 and EO_2 pins are floating state.</td><td>CMOS 3-states</td></tr>
<tr><td>27</td><td>CE</td><td>Chip Enable</td><td>Select signal input pin of the device.
Set CE to the high level to operate the device in the normal mode. Set CE to the low level in other cases. If this pin is at the low level, the PLL section is unconditionally disabled. However, a low-level signal less than 140 μs is not accepted.
If a CKSTP instruction used in a program is executed when the CE pin is at the low level (CKSTP is valid only for CE = Low; it is equivalent to NOP when CE = High), the internal clock generator and CPU stop their operations and the memory (RAM) hold state can be set with the low current requirement (MAX. 3 μA). The</td><td>Input</td></tr>
</table>

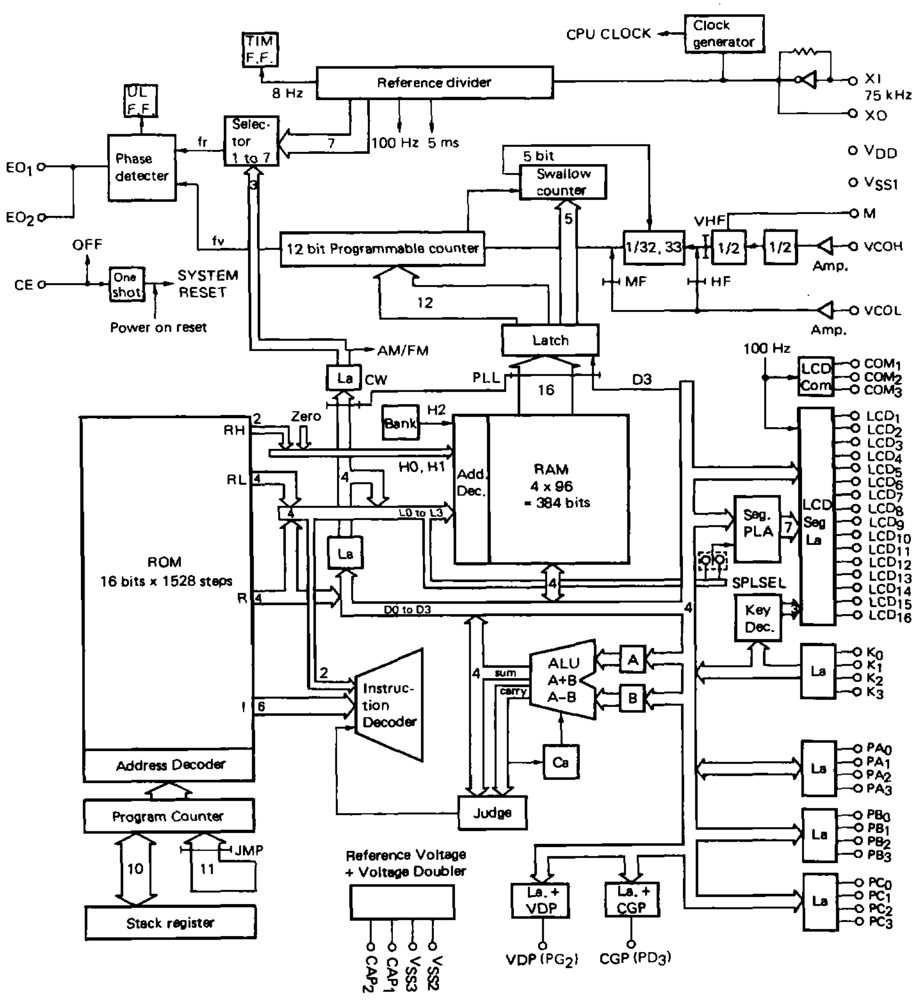
PIN NO.	SYMBOL	NAME	DESCRIPTION	OUTPUT TYPE
27	CE	Chip Enable	display outputs (LCD$_1$ to LCD$_{16}$ and COM$_1$ to COM$_3$) are set to the display off mode (low level). When the CE pin is changed from the low level to the high level, the device is reset and the program is started from address 0. In this case, port A is set to the input mode.	Input
28 29	XO XI	X'tal	Crystal resonator connecting pin. Oscillation frequency: 75 kHz.	CMOS (XO) Input (XI)
30 to 33	PA$_3$ to PA$_0$	Port A	4-bit input/output (I/O) port. The bit-unit I/O specification is possible depending on the data, PAIO word stored at address 1FH in BANK 0 of the data memory (RAM). This is used unconditionally as the input port when the device is powered, or the clock is stopped, or the CE pin is changed from the low level to the high level (at rise time). (Refer to Note 1 for details.)	CMOS Push-pull (when output)
34 to 37	PB$_3$ to PB$_0$	Port B	4-bit output dedicated port. Since the sink current is especially reduced due to the device configuration, it can be used as the key return signal source for the key matrix. This means the reverse-current preventive diode can be omitted by using this port as the key return signal source. When used as an ordinary output port, however, the correct low level may not be output because the sink current is insufficient depending on the drive circuits. Connect a pull-down resistor in this case. (See Notes 1 and 2 for details.)	CMOS Push-pull
41 54	NC	No Connection	This pin is not connected to the chip internally, that is, the user can arbitrarily connect this pin depending on his particular requirements.	–
38 to 40 42	PC$_3$ to PC$_0$	Port C	4-bit output dedicated port. Since the sink current is especially reduced due to the device configuration, it can be used as the key return signal source for the key matrix. This means the reverse-current preventive diode can be omitted by using this port as the key return signal source. When used as an ordinary output port, however, the correct low level may not be output because the sink current is insufficient depending on the drive circuits. Connect a pull-down resistor in this case. (See Notes 1 and 2 for details.)	CMOS Push-pull
43 to 45 47	K$_3$ to K$_0$	Key-return Signal Input	4-bit input dedicated port to be ordinarily used as the key matrix input. When a KIN or KI instruction is executed, the states of these pins are read in the data memory (RAM) specified by the operand field. The device configuration allows port C, PB$_0$, PB$_1$ and LCD$_9$ to LCD$_{16}$ to be used especially as the key return signal source. When LCD$_9$ to LCD$_{16}$ are used as the key source, the key source signal is output form these pins at 6.7 ms intervals while it is used for the display. Whether or not the key source signal is output can be determined with a TKLT or TKLF instruction. Therefore, a KI or KIN instruction must be executed after confirming that the key source signal has been output (TKLT or TKLF is exectued). (See Section 6 "KEY INPUT PROCEDURES" for details.)	Input

PIN NO.	SYMBOL	NAME	DESCRIPTION	OUTPUT TYPE
48 to 53 1 to 10	LCD_{16} to LCD_{11} LCD_{10} to LCD_1	LCD Segment Signal Output	Segment signal output pins for the LCD panel. Up to 48 dots can be displayed by forming a matrix with COM_1 to COM_3. Segment signal is output by the LCDD instruction executed. The LCD drive voltage is 3.1 V TYP. and drives the LCDs with 1/2 bias and 1/3 duty (frame frequency: 100 Hz). LCD_9 to LCD_{16} can be used as the display segment output pins and at the same time as the key source signal pins for the key matrix. These signals are output according to the time division and the key source signals are output at 6.7 ms intervals. Whether or not the key source signal is to be output while the display is taking place can be selected by a program. These pins are automatically set to the low level (display off mode) at power on reset (when V_{DD} is changed from the low level to the high level) or when the clock is stopped. The display mode is not changed at reset (when CE is changed from the low level to the high level).	CMOS Push-pull
11 to 13	COM_3 to COM_1	LCD Common Signal Output	Common signal output pins for the LCD panel. Up to 48 dots can be displayed by forming a matrix with LCD_1 to LCD_{16}. Three values, V_{SS3}, V_{SS2}, and V_{DD} are output at 50 Hz. These pins are set to the low level (display off mode) automatically at the power on reset (when V_{DD} is changed from the low level to the high level) or when the clock is stopped.	CMOS Push-pull

Note 1: For port operation instructions such as IN, OUT, SPB, and RPB, ports PA_0 and PA_3 correspond to the least-significant and most-significant bits of the register or operand data. This is also the case for ports B and C.

Note 2: Since the output dedicated ports (Port B, Port C, VDP and CGP) output undefined data when the device is powered on (that is when V_{DD} is changed from the low level to the high level), initialization must be performed by the program. The data output when the CE pin is changed from the low level to the high level, or vice versa, or when a CKSTP instruction is executed is the same as that previously output. For this reason, initialization is also required in some other cases as well.

BLOCK DIAGRAM



1. CPU

1.1 PROGRAM COUNTER (PC)

The program counter consists of an 11-bit binary counter for addressing a program in program memory (ROM) (Note 1)

PC_{10}	PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0

11 bits

The contents of the program counter are usually incremented by one each time an instruction is executed. When a jump or subroutine call instruction is executed, the address specified by the operand field is loaded(Note 2). When a skip instruction (ADS, TMT, RTS, etc.) is executed, the address of the instruction following the skip instruction is specified regardless of the skip condition. If the skip condition is satisfied, the instruction following the skip instruction is assumed to be NOP (No Operation). In this case, the NOP instruction is executed and the address of the next instruction is specified.

Note 1: The μPD1701, μPD1703, μPD1704, μPD1705, μPD1710, μPD1711, μPD1720 and μPD1730 (whose ROM capacity is less than 1 K step) have a 10-bit program counter.

Note 2: The JMP instruction has a 10-bit operand field and so PC_{10} is set or reset depending on the operation code since two kinds of JMP instructions are available for the μPD1715. A mnemonic code JMP is used for both of these JMP instructions but the assembler automatically determines which kind of JMP instruction is to be specified. (See Section 1.3 "Program Memory" for details). There exists only one kind of CAL instruction. PC_{10} is reset when a CAL instruction is executed.

1.2 STACK REGISTER (SR)

The stack register consists of 11 bits and is used to store the value obtained by adding one to the program counter contents. This is the 11-bit return address when a subroutine call instruction is executed. When a return instruction (RT or RTS) is executed, the stack register content is loaded back into the program counter, transferring control to the original program flow.

1.3 PROGRAM MEMORY (ROM)

The ROM includes 16 bits x 1528 steps and is used to store programs. The available ROM area extends from address 000H to address 5F7H (for 1528 steps).

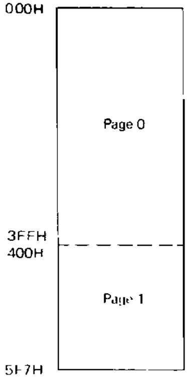


Fig. 1-1 ROM layout

The page concept is applicable to the μPD1715 ROM: Page 0 for ROM 000H to 3FFH and page 1 for ROM 400H to 5F7H.

When a program is written, the first address of a subroutine must exist in page 0. A subroutine whose first address is found in page 1 cannot be called from pages 0 and 1. (See Notes on CAL instruction usage for details).

A JMP instruction can be used in the assembler language without paying attention to the page specification. The same instruction format, JMP ADDR can be arbitrarily used for the addresses from 000H to 5F7H. The JMP instruction, however, for transferring control to an address in page 0 has a different operation code from the one for transferring control to an address in page 1.

The user must be careful to apply a patch modification during program debugging. (See Notes on JMP instruction usage for details.)

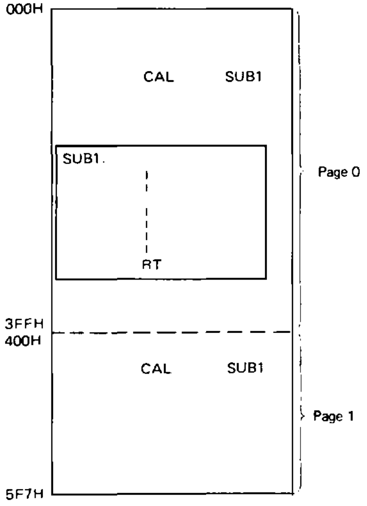
Please pay attention to the following notes when using the CAL and JMP instructions due to the different page concepts (pages 0 and 1) applicable on the μPD1715 ROM.

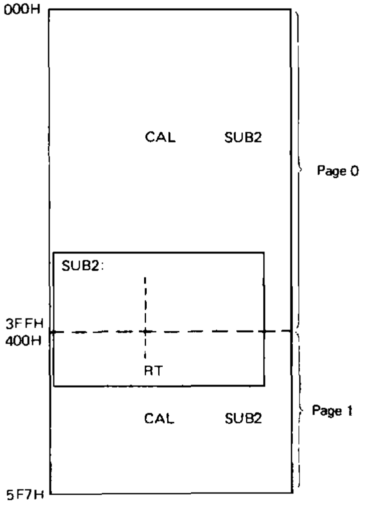
Notes on CAL instruction usage

When a CAL instruction is used, the call address, that is the first address of the subroutine to be called must exist in page 0 (000H to 3FFH). A subroutine whose first address is found in page 1 (400H to 5F7H) cannot be called.

The return address, however, may exist in page 1 because the stack register consists of 11 bits.

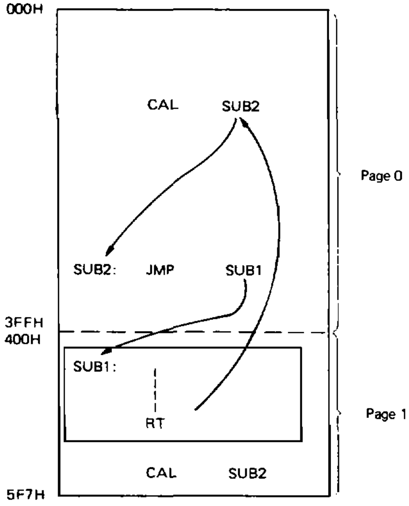
Example 1: When the first address of a subroutine exists in page 0.





As shown above, the return address (of RT or RTS) may exist in page 0 or 1 if the first address of the subroutine is found in page 0.

If the first address of the subroutine exists in page 0, a CAL instruction can be used without paying attention to the page designation. If the first address of a subroutine cannot be placed in page 0 due to a programming restriction, the following method can be used:



With this method, a JMP instruction is specified in page 0 and the subroutine SUB1 is called via the JMP instruction.

Notes on JMP instruction usage

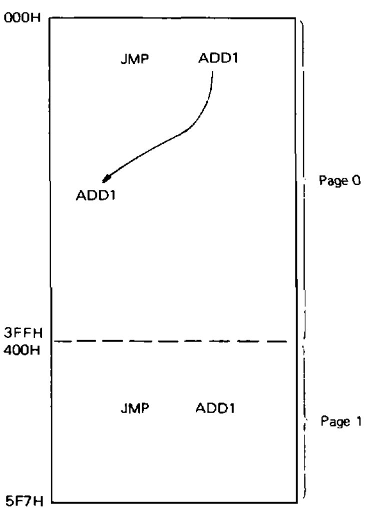
The page concept does not apply to a JMP instruction written in the assembler, that is, the same specification is possible for all ROM addresses 000H to 5F7H.

The operation code however, varies between a JMP instruction passing control to page 0 (addresses 000H to 3FFH) and one passing control to page 1 (addresses 400H to 5F7H).

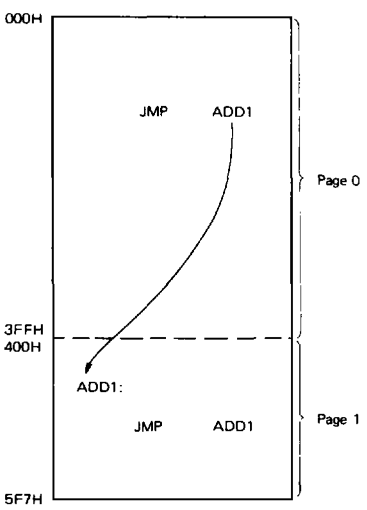
Operation code 06 is generated for the JMP instruction transferring control to page 0, while operation code 02 is used for the one transferring control to page 1.

These operation codes are automatically designated by the μPD1700 series assembler when the program is assembled.

Example cf operation code 06 (the jump destination address is found in page 0)

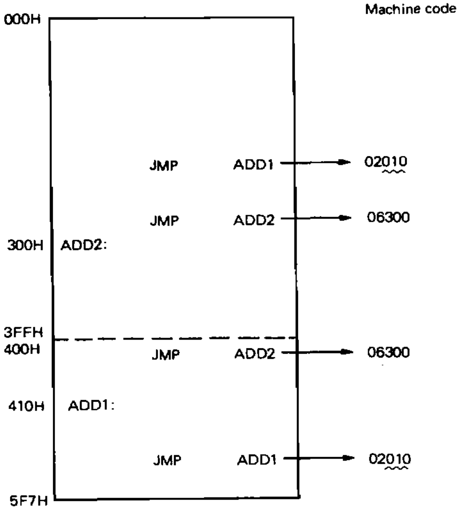


Example of operation code 02 (the jump destination address is found in page 1)



If a program patch is used for program modification during debugging, the programmer must use operation codes 02 and 06 properly. In addition, address conversion is necessary if the destination address of a JMP instruction exceeds 400H (use operation code 02). In this case, address 400H is assumed to be address 000H and other addresses are changed accordingly. For example, address 5F7H is converted to address 1F7H.

For JMP 400H, the user must input 02000 to apply a patch in the program. For JMP 000H, 06000 should be input.



1.4 DATA MEMORY (RAM)

RAM consists of 4 bits x 96 words and is used to store programs. The 96-word RAM is subdivided into BANK0 (64 words) and BANK1 (32 words). For any data processing, the bank specification of 0 or 1 is required.

Addresses 00H to 0FH in BANK0 are used as general registers for data operations and transfer using related memory. These registers can be also used as ordinary memory area. When memory is used as a general register, the bank specification is unnecessary and the address can be accessed regardless of the bank specification. When used as data memory, however, BANK0 must be specified in advance(Note).

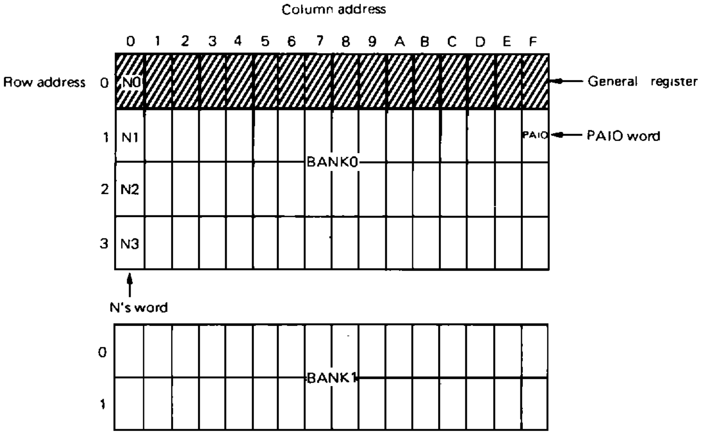


Fig. 1-2 RAM layout

Information necessary for controlling the PLL, that is, the dividing value, reference frequency, or dividing system can also be set via the RAM. For setting the dividing value, 4 bits x 4 words (N's words) at addresses 00H, 10H, 20H, and 30H and the most-significant bit of an arbitrary general register; a total of 17 bits are allocated. For the reference frequency and dividing system, an arbitrary one word (four bits) in RAM except for the N's words and the word including the N_F bits is assigned as the control word. The information in these bits is transferred to the PLL register with a PLL instruction.

Address 1FH in BANK0 is called the PAIO word and is used to specify the input or output for port A.

Note:
The most important point for general register operation in BANK1 is that the μPD1715 does not support any arithmetic instructions which perform operations between the data in a general register and the immediate data.

In a program in BANK0, "AI 00, 1" results in the incrementation of a general register at data memory address 00 by one. The AI instruction, however, is valid for an operation between data in the memory and immediate data, that is, the operation is not conducted between a register and the immediate data. If BANK1 is specified for the instruction above, the general register at address 00 is not incremented by one; instead, the contents of data memory address 00 in BANK1 are incremented by one.

1.5 TIMER F/F (TM F/F)

The timer F/F is set by the 8 Hz (125 ms) signal and is reset by the test timer (TTM) instruction.

Since the timer F/F is automatically set at 125 ms intervals, it can be used to measure ordinary time (8 counts/second) or to count the mute time.

The timer F/F is reset only by executing a TTM instruction so **the TTM instruction must be executed within the 125 ms interval.** If the TTM instruction is executed in a period equal to or greater than 125 ms, count errors occur and correct time management cannot be performed.

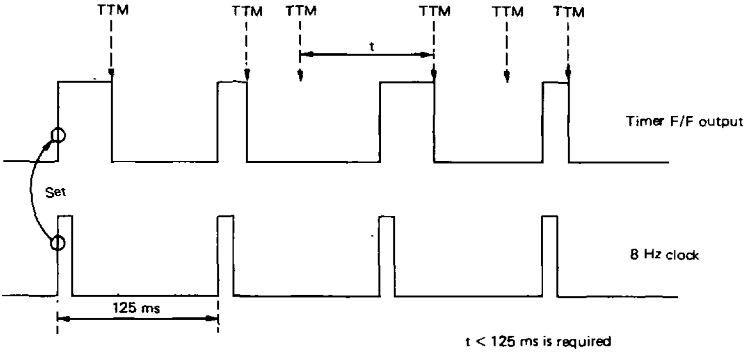
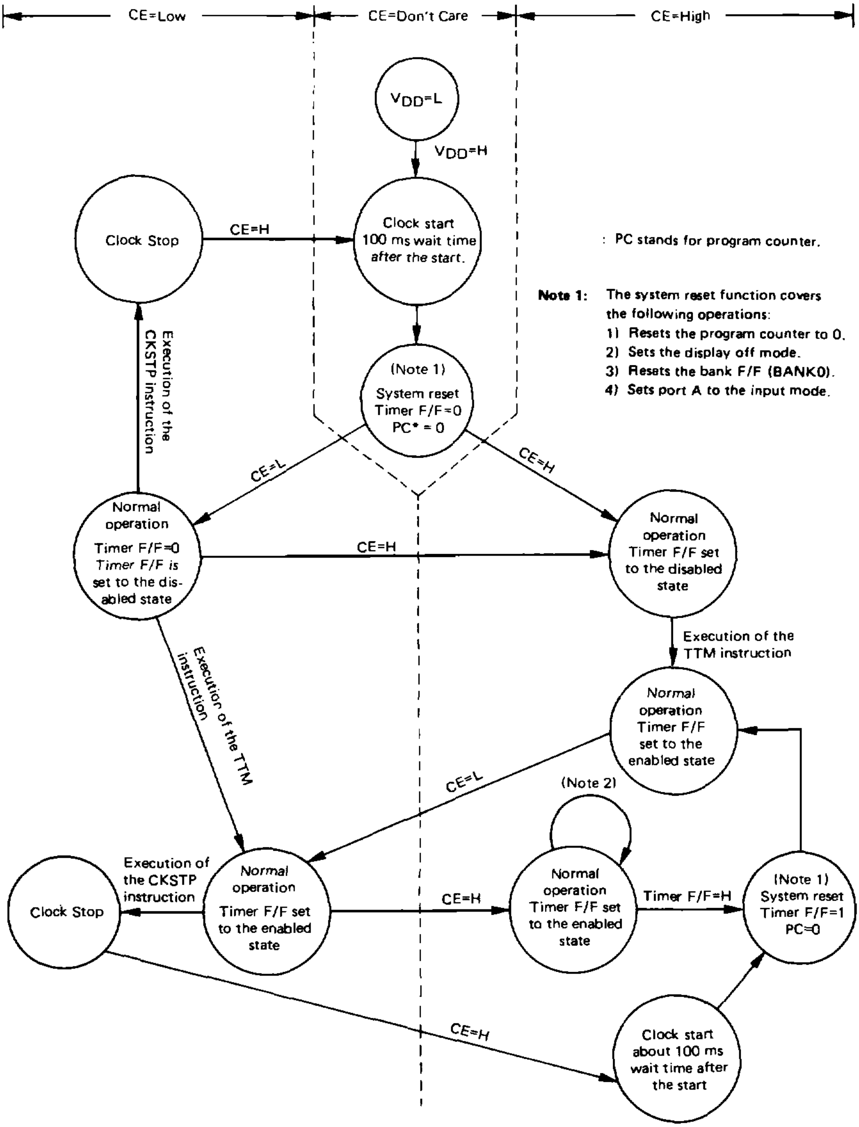


Fig. 1-3 TTM instruction execution timing

Furthermore, the timer F/F can also be used to check for a power failure. The timer F/F is reset when V_{DD} is changed from the low level to the high level and it is reset when a CKSTP instruction is executed or when CE is changed from the low level to the high level(Note 3). Figure 1-4 shows the state transition diagram illustrating these relationships.



* : PC stands for program counter.

Note 1: The system reset function covers the following operations:

1) Resets the program counter to 0.
2) Sets the display off mode.
3) Resets the bank F/F (BANK0).
4) Sets port A to the input mode.

Note 2: If the TTM instruction is executed during the time when the timer F/F is being set, control cannot be passed to any other routine from this loop. At this time, the timer F/F is set to 1 following the next 125 ms interval and control is passed to address 0.
Caution must be exercised because if the TTM instruction execution is carried out periodically and if the interval of TTM execution happens to be equal to that of the timer F/F setting (125 ms), control cannot then be transferred to address 0.

Fig. 1-4 CPU state transition via CE pin

As shown in Fig. 1-4, the program starts from address 0 when the system is powered on (V_{DD} = Low → High) **with the timer F/F reset** regardless of the CE pin state. After this point, the timer F/F cannot be set unless the TTM instruction is executed once (timer F/F set to the disabled state). Once the TTM instruction is executed, the timer F/F enabled state is set and the timer F/F is set at 125 ms intervals.

If the CE pin is changed from the low level to the high level while the power is V_{DD} = High, program control jumps to address 0 as soon as the timer F/F is set(Note 4). Consequently, the program starts from address 0 **with the timer F/F kept in the set state.**

As explained above, the timer content is different between the state when it has been restored from a power failure (V_{DD} = Low → High) and when it has returned from other than a power failure, that is, in the backup state (V_{DD} = High, CE = Low → High). Therefore, whether the current state has been restored from a power failure or from other than a power failure can be determined by checking the timer F/F content with a TTM instruction.

If the program starts from address 0 and the TTM instruction is executed with 125 ms, the TTM instruction determines that the current state has been restored from a power failure when the result is 0 (false) and that it has been restored from other than a power failure when the result is 1 (true) (that is system backup has been conducted).

In a program having a timer function which operates also for CE = Low (that is CKSTP is not used), the following function is required when the system is restored from other than a power failure (V_{DD} = High, CE = Low → High). Program control is transferred to address 0 if the timer F/F is set, so the timer must be updated after a TTM instruction is executed to detect a power failure (the result is true). If this routine is not included, the timer will be delayed 125 ms each time the CE pin is changed from the low level to the high level.

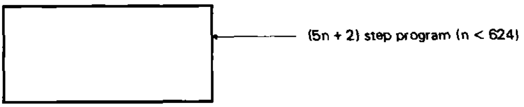
Note 3: The µPD1715 sets the timer F/F and passes program control to address 0 when CE is changed from the low level to the high level after a CKSTP instruction is executed. The µPD1701, µPD1704, µPD1710 and µPD1719 reset the timer F/F and pass program control to address 0.

The user must pay attention to the fact that the timer content varies between µPD1715 and µPD1701, µPD1704, µPD1710 and µPD1719 after a CKSTP execution.

Note 4: If the timer F/F setting and TTM execution take place simultaneously when CE is changed from the low level to the high level, program control is not passed to address 0. TTM execution shows that the timer F/F has been set, then the timer F/F is reset. This means that the user must be careful when a power failure is to be detected by a TTM instruction. When the timer F/F setting and TTM execution are initiated simultaneously, the TTM instruction takes precedence. This phenomenon does not affect the correct operation of the timer and a power failure may be determined by mistake. In the following program, however, control cannot be transferred to address 0 if the TTM execution and timer F/F setting take place at the same time (that is resetting cannot be performed).

```
ABC:
        TTM
        JMP     DEF
        AI      NEC1, 1
        AIC     NEC2, 0
        JMP     ABC

DEF:
```



```
        JMP             ABC
```

In this example, the TTM instruction is executed, the next "JMP DEF" is skipped because the timer F/F has been reset, then the next three instructions are executed. This means control is kept running in the loop. The loop time period is 200 μs (five steps). The timer F/F is set at 125 ms intervals and the DEF routine is executed. This routine consists of 5n + 5 steps (TTM + JMP + DEF routine: a multiple of 200 μs). When the CE pin is changed from the low level to the high level during a TTM execution in this program, the reset operation is not initiated as explained above. The TTM instruction checks that the timer F/F has been set, then the DEF routine is executed. However, since a multiple of 200 μs has elapsed from the time when the TTM instruction is executed to the next TTM execution, the timer F/F is next set (125 ms interval) at the same time when the TTM instruction is executed. Consequently, the reset operation is not carried out and control is kept running in the loop. This is the case for a program in which the TTM instruction is executed at 125 ms intervals. For this reason, the programmer must be careful not to create a routine in which the TTM execution interval is 125 ms.

1.6 INTERVAL PULSE (ITP)

The interval pulse is output with duty 60 % at 5 ms intervals and can be checked with a TIP instruction. Since a flip-flop (F/F) is not included, the pulse output is not reset even if the TIP instruction is executed. A correct timer (with a 5 ms interval) can be implemented by checking the interval pulse edge with successive TIP execution.

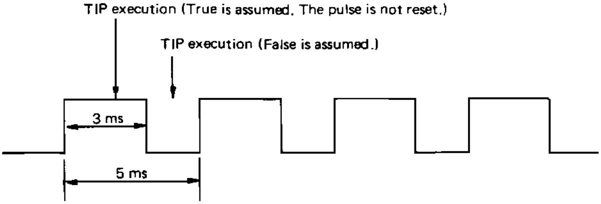

TIP execution (True is assumed. The pulse is not reset.)
TIP execution (False is assumed.)
3 ms
5 ms

Fig. 1-5 Interval pulse timing

1.7 UNLOCK F/F (UL F/F)

When the PLL system is not locked, that is, when the reference frequency, f_r is not equal to the VCO divided output frequency, pulses are output from the phase detector (ϕ-DET) at f_r intervals. The unlock F/F is set with this pulse and is reset when a TUL instruction is executed. For this reason, the interval at which **the TUL instruction is executed must be longer than f_r.** If it is less than f_r, the PLL system is assumed to be locked even if it is not actually locked, resulting in an error. For the first TUL instruction after a PLL execution, it is also necessary that a time period equal to or greater than f_r must have elapsed after the PLL execution.

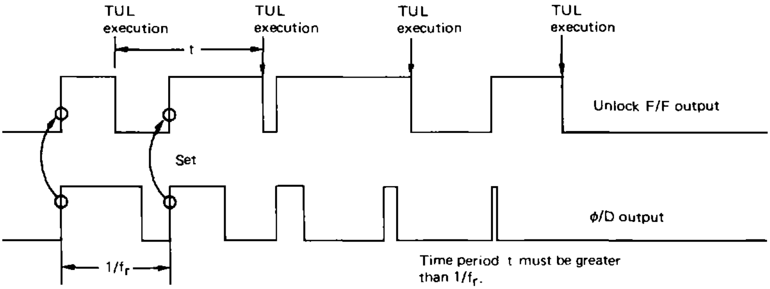


Fig. 1-6 TUL instruction execution timing

1.8 CARRY F/F (C F/F)

If a carry or borrow occurs as the result of the execution of an arithmetic instruction, the carry F/F is set; otherwise, it is reset. The carry F/F contents does not ordinarily change unless an arithmetic instruction is executed.

In addition, the carry F/F can be directly set or reset with a carry F/F set/reset instruction (STC, RSC) or a status word manipulation instruction (SS, RS).

1.9 BANK F/F (B F/F)

The BANK F/F is used for specifying a bank of data memory (RAM) and for addressing a port. The 96-ward RAM is subdivided into BANK0 (64 words) and BANK1 (32 words). Before starting data processing in a given bank, the BANK0 or BANK1 instruction must be executed to specify the bank. Data processing between banks is carried out through the general registers (addresses 00H to 0FH in BANK0). If addresses 00H to 0FH in BANK0 are used as general registers, the bank specification is not necessary and these registers can be accessed from both BANK0 and 1. When these addresses are used as memory area, BANK0 must be specified.

The BANK F/F is also used for addressing a port. Port addressing is specified by the use of two bits in the operand field of the instruction and the contents of the BANK F/F. (See 3. Section explanation of ports for details.)

The BANK F/F is reset and BANK0 is automatically specified when the system is first powered on (V$_{DD}$ = Low → High) and CE is changed from the low level to the high level. This means the device is reset.

1.10 KEY LATCH F/F (KL F/F)

When LCD pins (LCD$_9$ to LCD$_{16}$) are used as the key matrix key source, key source signals are asynchronously output from these pins according to the program (at 6.7 ms intervals). Thus the program must obtain information about whether or not the key source data has already been output via ports J and K and whether the key return signal has been latched by the key latch. The key latch F/F has been provided for this purpose.

The key latch F/F is reset when data is written through ports J or K or when a TKLT or TKLF instruction is executed and is set when the key source signal is output from pins LCD$_9$ to LCD$_{16}$ with a 200 μs setup time and the key return signal is latched by the key latch (at 6.7 ms intervals). The F/F content can be checked by the TKLT or TKLF instructions.

Moreover, the key latch F/F is valid only when the LCD control digit KLE is "1" and is not changed when it is "1". The key latch F/F is reset when the device is powered on or when the clock is stopped.

1.11 STATUS WORD

A status word consists of four bits indicating internal device states. These bits can be set or reset by program control. The following F/F inputs are connected to the status word:

Status word 1 (Write only word)

Manipulation instruction: SS, RS, etc.

#3	#2	#1	#0
BANK F/F2	BANK F/F1	Carry F/F	0

Status word 1 is a write only word and can be set or reset by instructions such as SS and RS.

Note: A read only word (Status Word 2) is provided as the status word in some systems of the μPD1700 series. When this is the case, the F/F state can be tested.

2. PLL

2.1 REFERENCE FREQUENCY GENERATOR (RFG)

The PLL is used to generate six reference frequencies 1, 3, 5, 6.25, 12.5 and 25 kHz by dividing the 75 kHz signal from an external crystal resonator. The reference frequency can be selected by a program (according to the control word data).

2.2 PHASE DETECTOR (φ-DET)

The phase detector is used to detect the phase difference between the reference frequency (f_r) and the frequency obtained by dividing the VCO output with a programmable divider. The phase detector output is input to the internal charge pump circuit and the resulting pulses are output to pins EO_1 and EO_2:

(1) $f_r > f_{OSC}/N$: Low-level signal
(2) $f_r < f_{OSC}/N$: High-level signal
(3) $f_r = f_{OSC}/N$: Floating state

Where, f_{OSC} is the VCO oscillation frequency and N is the dividing factor of the programmable divider.

2.3 PROGRAMMABLE DIVIDER (P/D)

The programmable divider is a binary down counter consisting of a swallow counter and a programmable counter.

The swallow counter is a 5-bit presettable down counter in which the contents of the NR0 (4 bits) and the N_F register (one bit) are preset with the period of the reference signal.

The programmable counter consists of 12 bits in which the contents of registers NR1 to NR3 are preset. The countdown takes place simultaneously for the programmable divider and the swallow counter.

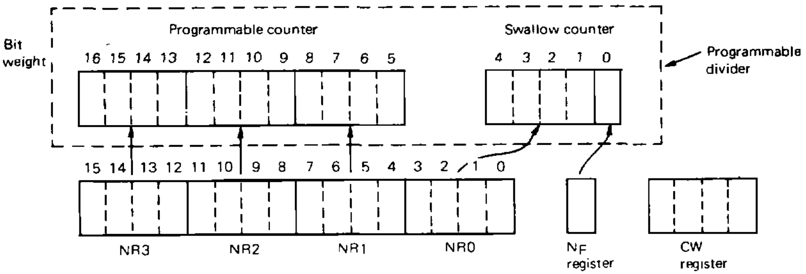


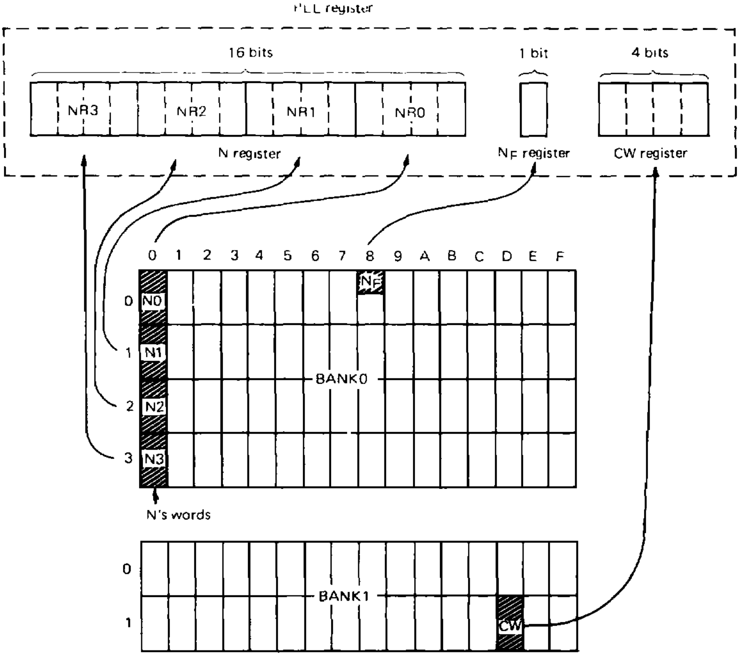
Fig. 2-1 Programmable divider configuration

2.4 PLL REGISTER

The following information is necessary for controlling the PLL in μPD1715:

(1) Dividing ratio (N)
(2) Reference frequency (f_r)
(3) Dividing method (direct or pulse swallowing method)

The PLL register is used to store these items. The PLL register consists of the N register (16 bits) and the N_F register (1 bit) for storing the dividing factor and the control word register (4 bits) for storing the reference frequency and dividing method information. They correspond to the N's word, the N_F bit, and the control word (CW) in data memory (RAM) and **are transferred by a PLL instruction.**



Note: Since the CW is in BANK1 in this example, BANK1 must be specified before the PLL instruction is executed.

Fig. 2-2 PLL register operation at PLL execution

The N's words are allocated to addresses 00H, 10H, 20H, and 30H in RAM, the N_F bit to the most-significant bit of an arbitrary general register, and CW to any RAM are except for the N's words and the word that includes the N_F bit.

The control word data codes are specified to select six reference frequencies (Table 2-1). The most significant bit (#3) of the control words specifies the dividing method: 0 for the direct dividing method and 1 for the pulse swallowing method.

When the direct dividing method is specified, the VCOL pin is selected and a 0.5 MHz to 15 MHz signal (V_{in} = 0.1 V_{p-p} MIN.) can be input to the VCOL pin. The input frequency is directly divided by the value set tin the programmable divider.

Table 2-1 Control word codes

Control word

#3	#2	#1	#0

0	Direct dividing method
1	Pulse swallowing method

#2	#1	#0	f_r (kHz)
0	0	0	1
0	0	1	6.25
0	1	0	5
0	1	1	3
1	0	1	12.5
1	1	0	25
1	1	1	Disable PLL*

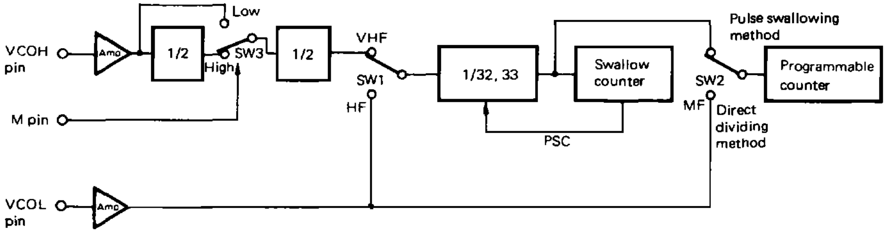
*: Bit 3 may be 0 or 1 in the PLL disable mode.

When the pulse swallowing method is specified, the pin to be selected varies between the VHF instruction and the HF instruction. When a VHF instruction is executed in the pulse swallowing method, the VCOH pin is selected and when the M pin is set to high level and used the 1/4 divider, a 10 MHz to 130 MHz signal (V_{in} = 0.1 V_{p-p} MIN.) can be input to the VCOH pin. If this is the case, the frequency of signal input to the VCOH pin is divided by the 1/4 divider, then it is delivered to the programmable counter via the 1/32 and 1/33 two-modulus prescaler. Also, if this is the case, when the M pin is set to low level, the frequency is divided by 1/2 divider. This is, the frequency of signal input to the VCOH pin is divided by the 1/2 divider, then it is delivered to the programmable counter via the two-modulus prescaler. If this is the case, a 10 MHz to 100 MHz signal (V_{in}= 0.1 Vp-p MIN.) can be input to the VCOH pin. When an HF instruction is executed in the pulse swallowing method, the VCOL pin is selected and a 0.6 MHz to 40 MHz signal (V_{in} = 0.1 V_{p-p} MIN.) can be input to the VCOL pin. In this case, the signal input to the VCOL pin is transferred to the programmable counter via the 1/32 and 1/33 two-modulus prescaler.

As explained above, a VHF instruction or an HF instruction must be executed if the pulse swallowing method is specified. Figure 2-3 depicts an equivalent internal circuit for showing these operations. In the diagram, SW1 is set to the other side by executing VHF or HF, whereas SW2 operates according to the PLL instruction.

If a VHF or HF instruction is executed when the direct dividing method is selected, the SW1 state changes according to the executed instruction, but the PLL operation in the direct dividing method is not affected at all.

Ordinarily, the direct dividing method is selected to receive the MW or LW band, while the pulse swallowing method (VHF) is selected to receive the FM band and the pulse swallowing method (HF) is selected to receive the SW band.



Note: The SW1 and SW2 states are undefined when the device is powered on (V_{DD} = Low → High).

Fig. 2-3 Equivalent internal circuit

Table 2-2 VCOL and VCOH pin states by dividing methods

CW#3	Dividing method	VCOL, VCOH pin state	Condition of the M pin	Input frequency	Dividing ratio
0	Direct dividing method	VCOL pin = Active (VCOH pin = Pull-down)	Don't care	0.5 to 15 MHz	16 to (2^{12} – 1)
1	Pulse swallowing method (HF instruction execution)			0.5 to 40 MHz	1024 to (2^{17} – 1)
	Pulse swallowing method (VHF instruction execution)	VCOH pin = Active (VCOL pin = Pull-down)	High (1/4)	10 to 130 MHz	4096 to (2^{17} – 2)
			Low (1/2)	10 to 100 MHz	2048 to (2^{17} – 4)

2.5 PLL INFORMATION SETTING

The PLL information (dividing ratio, dividing method, and reference frequency) can be set by a program. The dividing ratio of the programmable divider is set as follows.

1. Direct dividing method

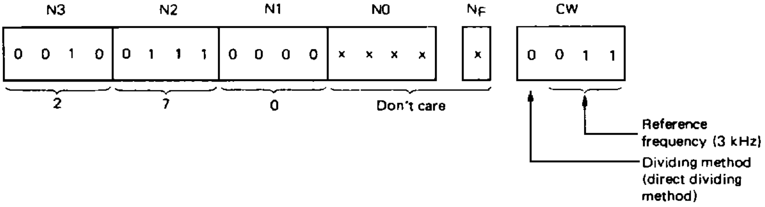
$$N = \frac{f_{VCOL}}{f_r}$$

f_{VCOL}: VCOL pin input frequency
f_r : Reference frequency

Example: When the MW band is received
(Receive frequency: 1422 kHz, reference frequency: 3 kHz, IF frequency: 450 kHz)

$$N = \frac{1422 + 450}{3} = 624$$

= 270H (H indicates hexadecimal notation)



N3	N2	N1	N0	N_F	CW
0 0 1 0	0 1 1 1	0 0 0 0	x x x x	x	0 0 1 1
2	7	0	Don't care		

Reference frequency (3 kHz)
Dividing method (direct dividing method)

In the direct dividing method, the N0 and N_F contents are ignored.

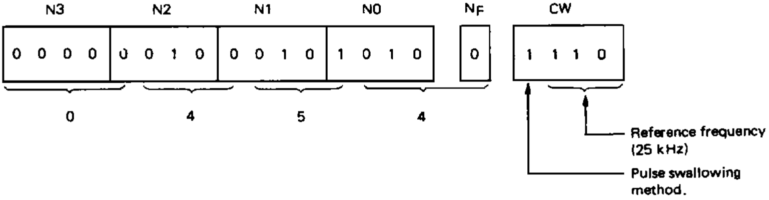
2. Pulse swallowing method (VHF instruction execution)

$$N = \frac{f_{VCOH}}{P \times f_r}$$

f_{VCOH} : VCOH pin input frequency
f_r : Reference frequency
P : Divider dividing value (= 2 or 4, selected by M pin)

Example: When the FM (U.S.A.) band is received (M pin = High)
(Receive frequency: 100.1 MHz, reference frequency: 25 kHz, IF frequency: 10.7 MHz)

$$N = \frac{(100.1 + 10.7) \times 10^6}{4 \times 25 \times 10^3} = 1108$$
$$= 454H \text{ (H indicates hexadecimal notation)}$$



N3	N2	N1	N0	N_F	CW
0 0 0 0	0 0 1 0	0 0 1 0	1 0 1 0	0	1 1 1 0
0	4	5	4		

In this example, the least-significant bit is the N_F bit. When the value is changed by one, the VCO oscillation frequency changes by 100 kHz. To change the frequency in steps of 200 kHz, 400 kHz, and 800 kHz, the value relative to N0 must be changed by one, two, and four, respectively.

In the example above, value N is determined by assuming that the N_F bit is the least-significant bit; however, programming will be facilitated by setting a value in 4-bit groups beginning from N0. That is, the reference frequency is assumed to be 50 kHz for calculation.

$$N = \frac{(100.1 + 10.7) \times 10^6}{4 \times 50 \times 10^3} = 554$$
$$= 22AH$$

N3	N2	N1	N0	NF	CW
0 0 0 0	0 0 1 0	0 0 1 0	1 0 1 0	0	1 1 1 0
0	2	2	A		

As explained above, the same value is obtained as in the case where the reference frequency is assumed to be 25 kHz.

3. Pulse swallowing method (HF instruction execution)

$$N = \frac{f_{VCOL}}{f_r}$$

f_{VCOL}: VCOL pin input frequency
f_r : Reference frequency

Example: When the SW band is received
(Receive frequency: 25.50 MHz, reference frequency: 5 kHz, IF frequency: 450 kHz)

$$N = \frac{25.5 \times 10^6 + 450 \times 10^3}{5 \times 10^3} = 5190$$
$$= 1446H$$

N3	N2	N1	N0	N_F	CW
0 0 0 0	1 0 1 0	0 0 1 0	0 0 1 1	0	1 0 1 0
1	4	4	6		

Reference frequency (5 kHz)
Pulse swallowing method

In this example, the N_F bit is assumed to be the least significant bit. When the value is changed by one, the VCO oscillation frequency is changed by 5 kHz. To change the frequency in steps of 10 kHz, 20 kHz, and 40 kHz, the value relative to N0 must be changed by one, two, and four, respectively.

As is clear from these three examples, 17 bits beginning from the N_F bit are valid when the pulse swallowing method is selected, whereas 12 bits beginning from the N1 word become valid when the direct dividing system is specified.

3. PORTS

The μPD1715 uses port A (PA_3 to PA_0) as the input/output port and port B (PB_3 to PB_0), port C (PC_3 to PC_0), CGP (PD_3), and VDP (PG_2) as output dedicated ports. Furthermore, it has internal ports: Port D (PD_2), port G (PG_1 to PG_3), port H (PH_3 to PH_0), port J (PJ_2 to PJ_0), and port K (PK_1 and PK_0). Internal ports are used to set data for the CGP and VDP and to set ports when LCD pins (LCD_9 to LCD_{16}) are used as the key source.

A port is addressed by the use of direct addressing with two bits in the operand field of an instruction and the BANK F/F. Table 3-1 lists the correspondence between direct addressing and the BANK F/F specification.

Table 3-1 Port addresses

Direct Add.		BANK		
#1	#0	BANK0	BANK1	BANK2
0	0	PA	–	PJ
0	1	PB	–	PK
1	0	PC	PG	–
1	1	PD	PH	–

Note: The BANK F/F is commonly used for port and RAM operations. If BANK0 (RAM) is used after the ports of BANKs1 and 2 have been operated, the BANK F/F must be returned to BANK0 before BANK0 is used.

3.1 PORT A

For port A (PA_3 to PA_0), bit-unit input/output can be specified. Input/output is specified according to the data stored at address 1 FH of BANK0 (called the PAIO word) in data memory (RAM). To set a port as an input port, specify 0 in the bit of the PAIO word corresponding to the port. To set a port as an output port, specify 1 in the corresponding bit of the PAIO word.

	#3	#2	#1	#0
PAIO word (address 1FH of BANK0)	PA_3	PA_2	PA_1	PA_0

Example 1: When PA_3 and PA_2 are set as output ports and PA_1 and PA_0 are set as input ports.

	#3	#2	#1	#0
PAIO word	1	1	0	0

Example 2: When port A (PA_3 to PA_0) is set as an output port.

	#3	#2	#1	#0
PAIO word	1	1	1	1

For port A, an input/output instruction must be executed after the input/output specification is set in the PAIO word. The input/output mode once set remains unchanged until the PAIO word contents (at address IF of BANK0) are changed.

The input mode however, is automatically set when the device is powered on (V_{DD} = Low → High), and the CKSTP instruction is executed, or when CE is changed from the low level to the high level.

It should be noted that the PAIO word contents are not necessarily reflected on the port A input/output state. The device operates in the input mode for port A from this point on until the PAIO word is set.

Example:

```
BANK0

MVI    1FH, 1111B ;  Set all bits of port A for output ports.
 :
MVI    08H, 1100B ;  Set ports as follows: PA3 and PA2 to the high level, and PA1 and PA0 to the low level.

OUT    0,  08 H   ;  Set ports as follows: PA3 and PA2 to the high level, and PA1 and PA0 to the low level.
 :
 :
```

3.2 PORT B AND PORT C

Port B (PB_3 to PB_0) and port C (PC_3 to PC_0) of the µPD1715 are CMOS-type output dedicated ports. Ordinarily, they are used by output instructions such as OUT, SPB, and RPB. If an input (IN) instruction is executed, the data being output is read in the register specified by the operand field of the IN instruction. The output data is not changed by the IN execution.

If "1" is output when an output instruction is executed, the high-level signal (V_{DD} potential) is output; if "0" is output, the low-level signal (GND potential) is output.

Note 1: Since data output from port B and port C is undefined when the device is powered on (V_{DD} = Low → High), these ports must be initialized by a program when the device is powered on.

Note 2: Data output from port B and port C is not changed for a CE change (High to low, or vice versa) with V_{DD} = High. That is, the previous state remains unchanged. This is also the case when a CKSTP instruction is executed.

Example 1: Port initialization at device power on

```
 START:
         RPB     0    , 1111B  ;  Port A (PA3 to PA0) = All low
         MVI     1FH,  1111B   ;  Set all bits of port A for output ports.
         RPB     1    , 1111B  ;  Port B (PB3 to PB0) = All low
         RPB     2    , 1111B  ;  Port C (PC3 to PC0) = All low
         RPB     3    , 1111B  ;  CGP (PD3) = Low
         TTM                   ;  If the timer F/F has been set, the RAM
         JMP     BACKUP        ;  initialization is not carried out.
         MVI     00H, 0        ; |
         MVI     01H, 0        ; } RAM initialization
          :                      |
          :                      |
          :                      |
BACKUP:
```

Example 2: Port reset at clock stop

For port B, port C, and CGP (PD_3), the previous states are retained even if a clock stop (CKSTP) instruction is executed in the μPD1715. Consequently, if it is necessary to prevent current from flowing out of a port when the clock is stopped (that is if the port is to be set to the low level), the port must be reset before the clock stop instruction is executed as follows.

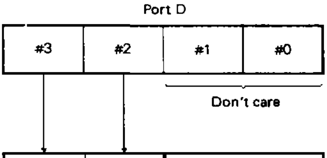
```
①   TCET           ;  Do not skip if pin CE is at the low level for more than 120 μs before ① .
②   TCEF           ;  Skip if pin CE is at the low level for more than 160 μs before ② .
③   JMP   NOTSTP   ;  Jump to NOTSTP if pin CE is found to be at the high level during ① or ② (CKSTP
                      is not executed).
④  ⎧RPB   1, 1111B ;  Reset port B completely.
   ⎨RPB   2, 1111B ;  Reset port C completely.
   ⎩RPB   3, 1111B ;  Reset CGP.
⑤   CKSTP          ;  The branch to address 0 is synchronized with the 8 Hz signal if pin CE is set to the
⑥   JMP   $-1         high level after ③ (the reset operation is initiated).
                      If this is the case, the loop formed by ⑤ and ⑥ is executed until the 8 Hz signal
                      rises up. If pin CE continues to be at the low level at ⑤ , the clock is stopped.
```

Note: Even if a low-level signal not exceeding 140 μs is input to pin CE, the reset operation is not initiated; so ① and ② are provided to prevent wrong operation. The low-level signal must continue for at least 120 μs (three instruction cycles) for a TCET or TCEF instruction to determine the low-level state. If pin CE is at the low level for more than 160 μs (four instruction cycles) before a CKSTP instruction is issued, the CKSTP instruction stops the clock.

3.3 CLOCK GENERATOR PORT (CGP)

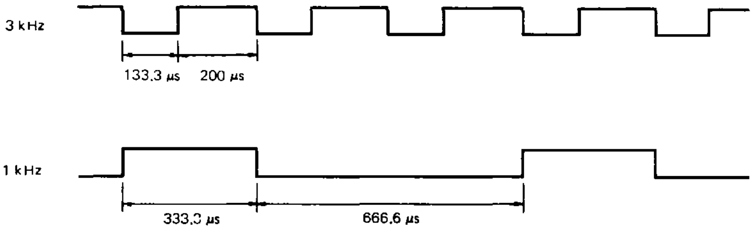
The CGP is used as the modulated signal output port for outputting the 1 kHz or 3 kHz pulse. It can also be used to output bit-unit data. Port usage can be specified by the use of an internal port, port D. An internal port has no *pins, but it can be operated with the same port manipulation instructions as the ordinary ports.*

The CGP pin output is set when port D is specified as follows:



#3	#2	CGP pin
0	0	Low
1	0	High
0	1	3 kHz
1	1	1 kHz

The 3 kHz and 1 kHz pulses are output respectively with the following waveforms.



Example: The 3 kHz pulse is output from CGP.

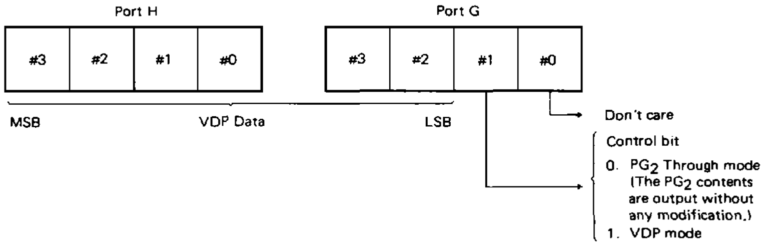
```
BANK0                 ;  Specify BANK0.
MVI    00H,0100B      ;  Set the 3 kHz output data at address 00H.
OUT    3, 00H         ;  Output the 3 kHz pulse from CGP.
  .
  .
  .
```

3.4 VARIABLE DUTY PORT (VDP)

The VDP can be used as a variable-duty port for outputting a 1.12 kHz pulse repeatedly and it is also used as a bit-unit output port.

The VDP can vary duty of a 1.12 kHz pulse in 64 steps: from 2/67 to 65/67. These operations can be specified by use of internal ports, port G and port H. An internal port has no pins but it can be used in the same way as the ordinary ports. This means that all port manipulation instructions are applicable. Since the addresses of ports G and H are allocated to BANK1, it must be specified before the port operation is started.

Bits are related to each other for ports G and H as follows:


Port H
#3
#2
#1
#0
Port G
#3
#2
#1
#0
MSB
VDP Data
LSB
Don't care
Control bit
0. PG2 Through mode (The PG2 contents are output without any modification.)
1. VDP mode

The duty value is obtained by the following expression in the VDP mode:

$$\text{duty} = \frac{\text{Time period of High}}{\text{Period}} = \frac{(\text{VDP data}) + 2}{67}$$

The duty variable range is expressed as follows:

$$\text{duty} = \frac{26.7\ \mu s}{893\ \mu s} \text{ to } \frac{867\ \mu s}{893\ \mu s}$$

If PG_1 of the control bit is set to 0, the PG_2 through mode is set and the VDP can be used as a bit-unit output port. In this case, the PG_2 contents are output.

The VDP pin is at the low level at power-on reset (V_{DD} = Low → High) or when the clock is stopped. The VDP pin state is not affected by the states of port G and port H and the reset state is released when a write instruction (OUT, SPB, or RPB) to port G is executed. The previous state is retained at reset (CE = Low → High).

3.5 PORT J AND PORT K

PJ_2 to PJ_0, PK_1 and PK_0 are internal ports for setting the input data of the key source decoder. In other words, the input data of the key source decoder is set via these ports. The difference between these ports and the general-purpose output port is that the output of port J and port K is not delivered to any external pins so all port manipulation instructions can be used for port J and port K. The contents of port J and port K are retained even when the clock is stopped with a CKSTP instruction.

If IN, TPT, or TPF is executed for port J and port K, the instruction is executed on the data which is being output from port J and port K to the key source decoder. Since only the two low-order bits are valid on port K, the two high-order bits are read as "0" if an IN instruction is executed for port K.

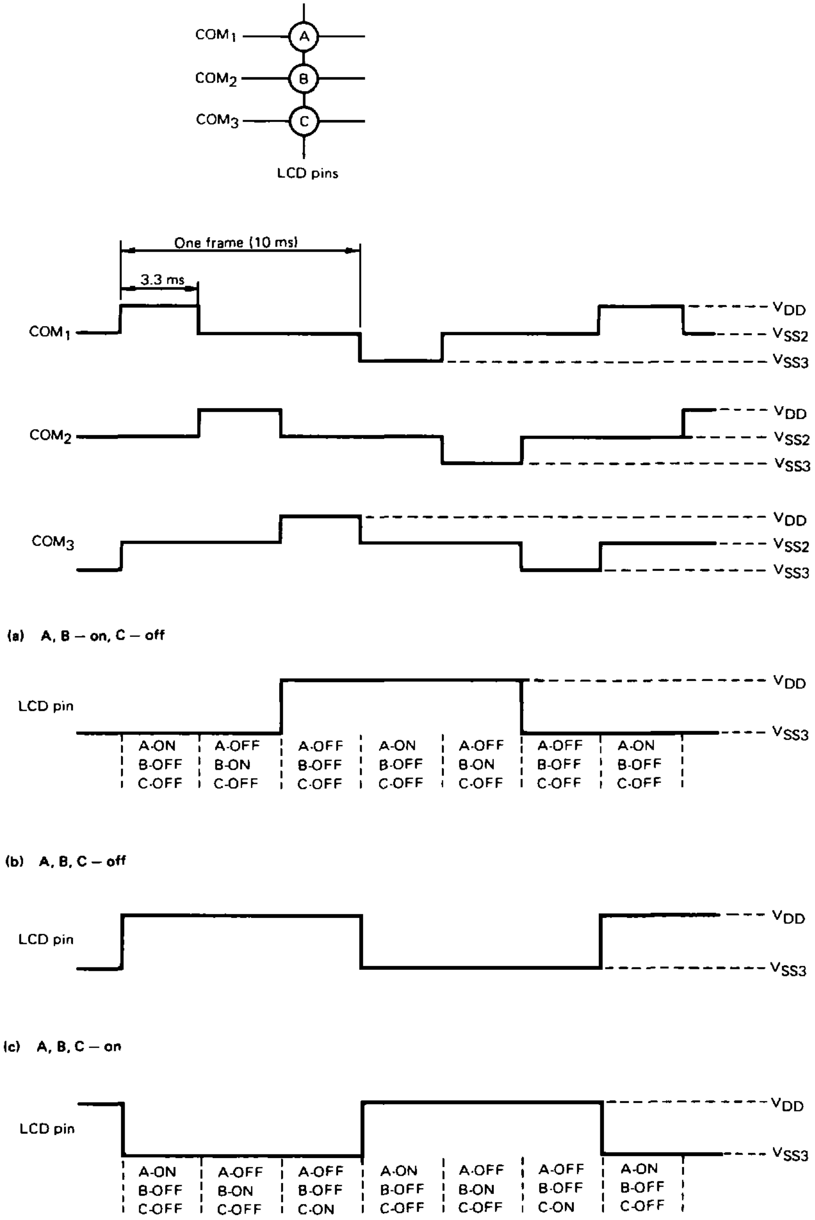
4. LCD DRIVER

The μPD1715 includes a 1/3 duty, 1/2 bias driving (voltage average method) LCD driver (frame frequency: 100 Hz, driving voltage: 3.1 V). Figure 4-1 shows the timing chart for the LCD driver operation. As can be seen from Fig. 4-1, the common signal outputs three kinds of voltages: V_{DD}, V_{SS3}, and intermediate voltage V_{SS2}. That is, the common signal voltage changes $\pm \frac{V_{DD} - V_{SS3}}{2}$ relative to V_{SS2}.

Consequently, three segments (A, B, and C) can be driven by a segment output. The segment for which the potential difference from the common signal ($V_{DD} - V_{SS3}$) becomes the greatest is turned on.

Eight pins (LCD_9 to LCD_{16}) among the segment output pins are configured to be used as the key source of the key matrix while they are used for display. Figure 4-2 depicts the LCD driving signal waveform for this operation. Figure 4-1 shows the LCD driving signal waveform when segment output pins are not used as the key source (in the key input through mode). As shown in Fig. 4-2, the LCD display and key source signals are output according to the time division. The key source signal has an interval of 6.7 ms and is output for 133 μs. Since the key source signal is not synchronized with the program, it is impossible to input the key state as it is with a KIN or KI instruction.

To overcome this difficulty, when segment pins are used as key source signals, the data on key input pins (K_3 to K_0) is latched when the key source signal is output, then the latched data is read with a KIN or KI instruction. However, if the key latch F/F is in the reset state, the data is automatically latched at intervals of 6.7 ms of the key source signal. Therefore, when the LCD pin is used as the key source, a quick key response cannot be expected; however, it is sufficient for ordinary usage. Ports can be effectively used when the LCD pin is assigned as the key source of the key matrix.

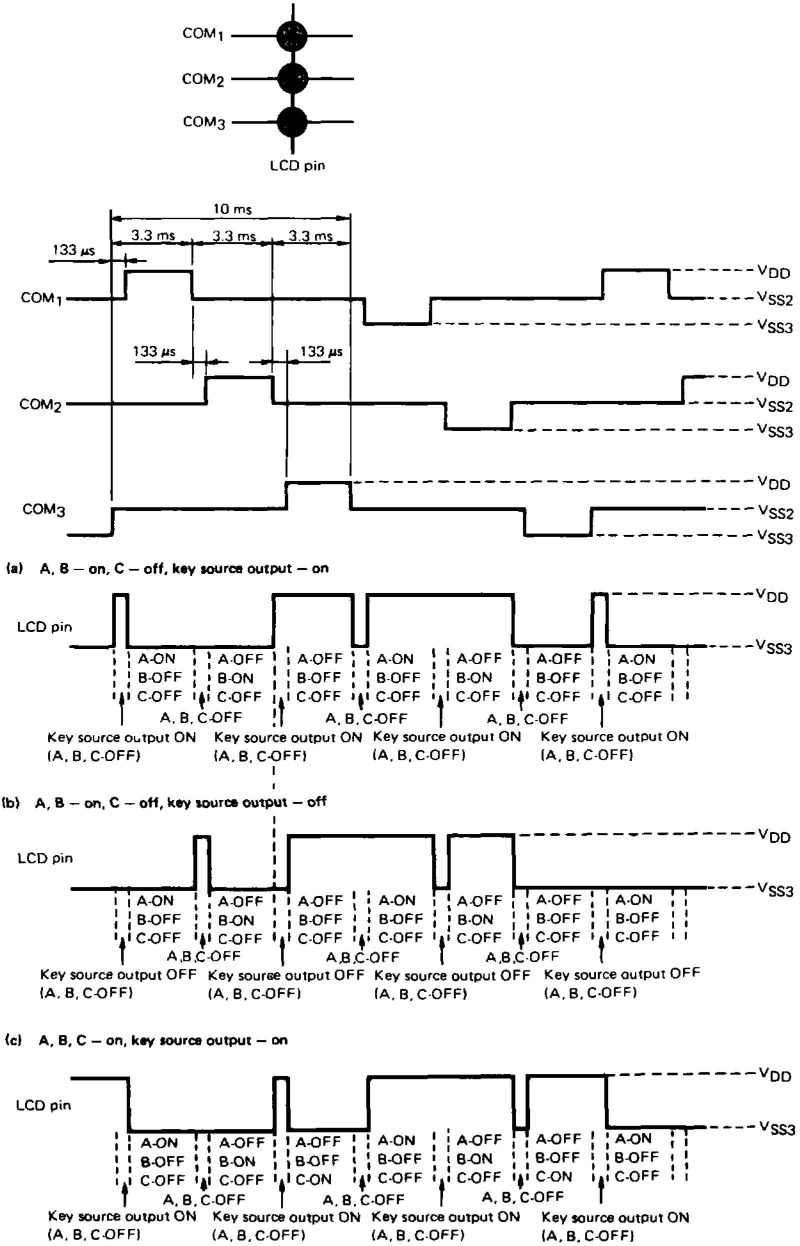


(a) A, B – on, C – off

(b) A, B, C – off

(c) A, B, C – on

Fig. 4-1 LCD driving signal waveform (key input through mode)



(a) A, B — on, C — off, key source output — on

(b) A, B — on, C — off, key source output — off

(c) A, B, C — on, key source output — on

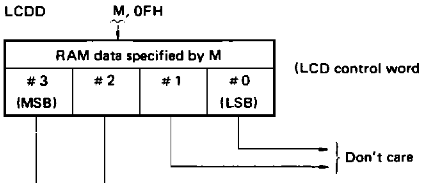
Fig. 4-2 LCD driving signal waveform (key source output mode)

4.1 DIGIT

The 48 dots that can be displayed on the LCD are controlled in 12 groups: 0 to B. Each group is called a digit. In addition to these 12 digits, there is a control digit F, which corresponds to the LCD control word for controlling the LCD driver and not to any dots on the LCD panel. This means that a data transfer to digit F indicates a transfer of data to the LCD control word.

Bit #3 of the LCD control word is called the LCD Enable bit and is used to control the display mode state (on/off). Bit #2 is the Latch Enable bit for controlling whether or not LCD pins (LCD$_9$ to LCD$_{16}$) are to be used as the key source. Two low-order bits (#1 and #0) are assigned as "Don't care".

The LCD control word has the following functions:



Bit name	Function	At reset
KLE (Key latch Enable bit)	0: The key source signal is not output from the LCD pins. The key latch remains open, so the key input pin state can be directly read with a KI or KIN instruction (key input through mode). 1: The key source signal is output from the LCD pins. The key latch is opened only when the key source signal is output from the LCD pins. In this case, the key latch state can be read with KI or KIN instruction (key source output mode).	0
LCDE (LCD Enable bit)	0: Display off state (Display off mode). LCD and common pins are set to the low level. 1: Display on state (Display on mode). Data stored in the LCD segment latch is displayed, that is, the ordinary LCD display operation is carried out.	0

Note;
Reset time indicates the time when the device is powered on or the clock is stopped.

Figure 4-3 shows the digit configuration.

For dots placed at the even-numbered positions, Dig-0, Dig-2, Dig-4, Dig-6, Dig-8, and Dig-A, the data transferred with an LCDD instruction is stored in the segment PLA and the data output from the PLA is displayed. For dots placed at the odd-numbered positions, Dig-1, Dig-3, Dig-5, Dig-7, Dig-9, and Dig-B, the data transferred by an LCDD instruction is displayed. Table 4-1 lists the correspondence between the data and dots to be displayed.

Some dots belong to two kinds of digits. These dots can be displayed in two ways: The pertinent even-numbered position is specified at LCDD execution to display the dot via the PLA, or the odd-numbered position is specified as data output directly from the RAM for the dot display.

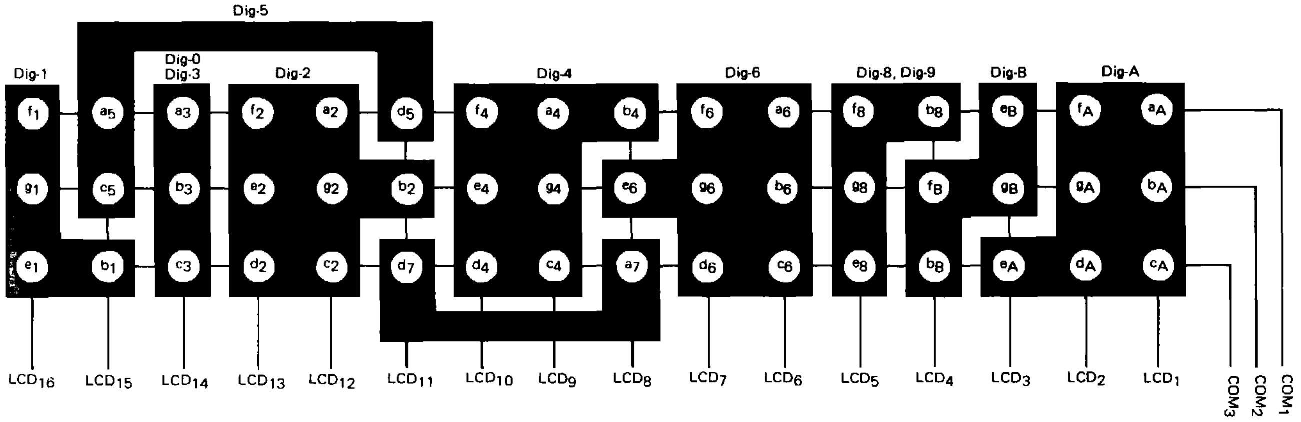


Fig. 4-3 LCD matrix

Table 4-1 Bit correspondence for add-numbered positions (to be displayed without using the PLA)

MSB			LSB	
# 3	# 2	# 1	# 0	← RAM bits
	c	d	a	
b	f	g	e	

D

4.2 DISPLAY PROCEDURE

In the μPD1715 system, data is displayed by executing the following instruction to an external LCD panel:

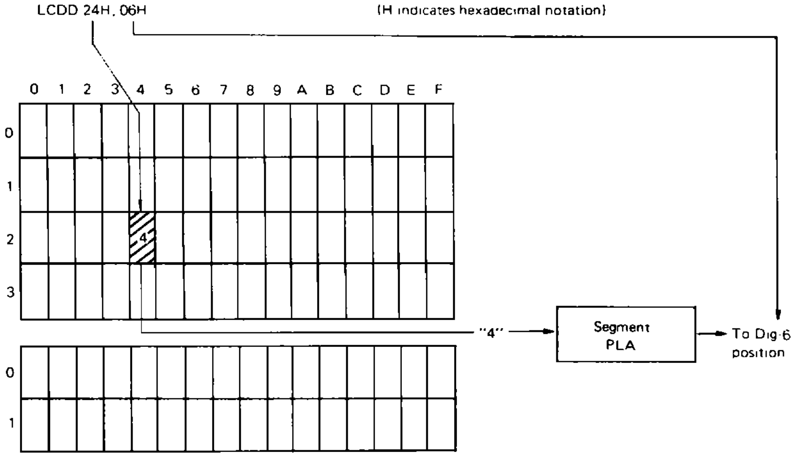
```
LCDD  M, D
```

M indicates an arbitrary address in the data memory (RAM) and D specifies the digit number of the digit to be displayed. Value D has one of the following 13 values: 12 values for Dig-0, Dig-B (00H to 0DH) and the dislay on/off and key source signal output assignment (0FH) as shown in the LCD matrix in Fig. 4-3.

If value D contains one of the values 00H to 0D for the even-numbered positions (Dig-0, Dig-2, Dig-4, Dig-6, Dig-8, and Dig-A). The content of the data memory (RAM) specified by value M is unconditionally output to the character position specified by value D through the programmable logic array (PLA) for the display.

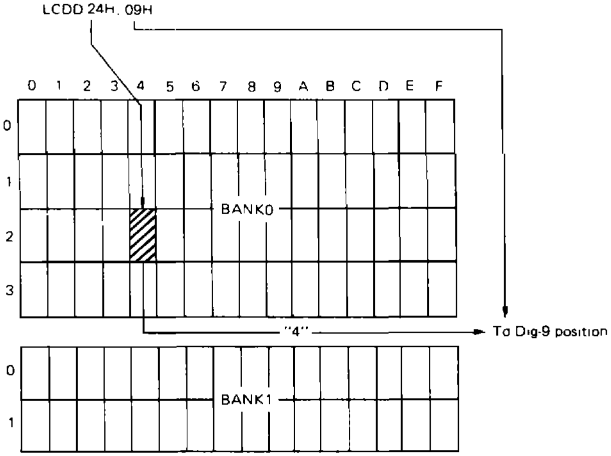
If value D indicates one of the odd-numbered positions (Dig-1, Dig-3, Dig-5, Dig-7, Dig-9, and Dig-B), the contents of data memory (RAM) specified by value M are directly output (for the display) to the character position specified by value D without using the PLA. Tabel 4-1 lists the correspondence between the RAM data bits to be output to odd-numbered positions and the segments arranged at the odd-numbered positions.

The following is an example of the operations at LCDD execution:


LCDD 24H, 06H
(H indicates hexadecimal notation)
0 1 2 3 4 5 6 7 8 9 A B C D E F
0
1
2
3
4
0
1
"4"
Segment PLA
To Dig-6 position

Data "4" at address 24H in data memory (RAM) is delivered to the PLA, then the PLA content is output to the Dig-6 position. If SPLSEL contains "3", the content at address 4 in pattern group 0 is output to the Dig-6 position. If SPLSEL contains "2", the content at address 4 in pattern group 1 is output.

Example: Digit display at odd-numbered positon



Data "4" at address 24H in data memory (RAM) is directly output to the Dig-9 position. Four segments, b_8, e_8, f_8, and g_8, are arranged at the Dig-9 position. When value 4 = 0100B is output, only segment f_8 turns on. (See Table 4-1 for details.) Similarly, when value 5 = 0101B is output to the Dig-9 position, segments f_8 and e_8 turn on.

As can be seen from the LCD matrix in Fig. 4-3, the Dig-8 position (even-numbered position) can be used as the Dig-9 position (odd-numbered position). For example,

```
LCDD 10H, 08H
```

results in the Dig-8 position being displayed via the PLA. For the following instruction, however,

```
LCDD 10H, 09H
```

the Dig-8 position is displayed without using the PLA. Similarly, the Dig-3 position (odd-numbered position) can be used as the Dig-0 position (even-numbered position). That is, data can be displayed at these positions via the PLA or without using the PLA.

When the device is powered on (V_{DD} = Low → High) or when a CKSTP instruction is executed, the μPD1715 automatically sets the LCD segment pins (LCD_1 to LCD_{16}) and LCD common pins (COM_1 to COM_3) to the low level (**that is display off mode**). This means that all segments on the LCD panel are turned off in the display off mode.

In the display off mode, the display is not turned on even if LCDD M, D (where, $0 \leqq D \leqq 0DH$) is executed. This LCDD instruction only causes the latch data in the LCD segment latch circuit to be rewritten.

Consequently, **the display on mode must be set** to display any segment on the LCD panel.

The following instruction is used to change the device from the display off mode to the display on mode:

```
MVI   M, 1XXXB
LCDD  M, 0FH
```

As listed above, 0FH is specified for the second operand (D) of the LCDD instruction and 1XXXB (X = 0 or 1) is specified as the contents of the data memory (RAM) addressed by value M. In order to set the device from the display on mode to the display off mode by a program, value 0XXXB (X = 0 or 1) is output to the Dig-F position.

The latch data in the LCD segment is not changed when the display off mode is set unless LCDD M, D (where, 0 ≤ D ≤ 0DH) is executed, that is, the previous data (stored in the display on mode) is retained.

A program for blinking all segments on the LCD panel at a predetermined interval can be implemented by using LCDD instructions which set the display on mode an display off mode in succession as explanined above.

The following is an example of such a program:

```
          .
          .
          .
          .
       LCDD   12H, 0AH   ;  Output data to Dig-A position.
       LCDD   11H, 0BH   ;  Output data to Dig-B position.
       MVI    CONT, 8    ;  Set the 5-second timer.
       ANI    34H, 0100B ;  Set the display off mode data.
  FLASH:
       LCDD   34H, 0FH   ;  Display off mode (all segments off)
       CAL    WT500M     ;  Call subroutine for 500 ms wait.
       ORI    34H, 1000B ;  Reverse display.
       SIS    CONT, 1    ;  Skip after 5-time operation, that is, five seconds.
       JMP    FLASH      ;  Return to FLASH again if five seconds have not elapsed.
          .
          .
          .
          .
```

In this program example, each digit positions on the LCD panel is turned on, then all segments, that is, the entire LCD panel is blinked at 500 ms intervals for five seconds (500 ms off, 500 ms on).

Note: The contents of the LCD segment latch are undefined when the device is powered on (V_{DD} = Low → High). If the display on mode is set immediately after the power is turned on, undefined data may be displayed in some cases. To prevent this from occurring, the data to be displayed in the display off mode must be output in advance to the respective character positions before the display on mode is set.

5. KEY INPUT PROCEDURE

The μPD1715 supports three key matrix configurations.

The first uses only the general-purpose ports (PA_3 to PA_0, PB_3 to PB_0, PC_3 to PC_0, VDP, and CGP) for the key matrix source signals. The second configuration uses only the LCD pins (LCD_9 to LCD_{16}) and the third uses the general-purpose ports and LCD pins (LCD_9 to LCD_{16}) for the key source signals.

The following are examples of these three key matrix configurations:

5.1 GENERAL-PURPOSE POSTS USED FOR KEY SOURCE

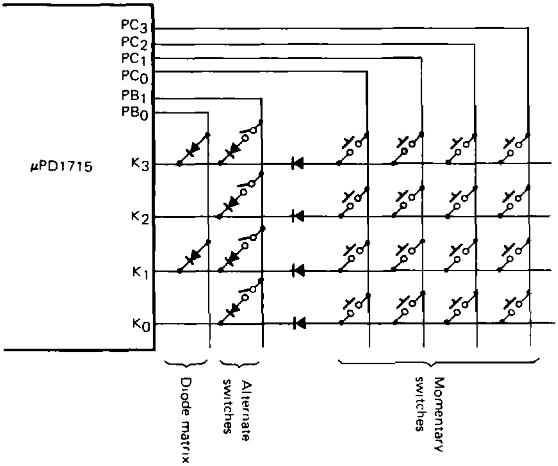


Fig. 5-1. Example of the key matrix configuration which uses the general purpose ports for its key source

Since the μPD1715 is driven with a low voltage, V_{DD} = 2.0 V to 3.6 V, the reverse current preventive diode must be carefully inserted when configuring the key matrix. This means that since the voltage of the signal output from the key source is low, only the voltage drop corresponding to a diode stage is allowed to determine the high-level condition at the key input pin. Because of this, the sink current of port C (PC_3 to PC_0) is set lower than other ports. For this reason, even if the momentary switch is repeatedly pressed as in Fig. 5-1, the high-level condition of the key input pin is guaranteed because the sink current of port C is low. The above explanation also applies to the other two key matrix configurations.

When the above configuration is used, the program must reset the LCD control digit, KLE (key latch enable F/F) to set the key input through mode. (The device is set to this mode when it is powered on or when the clock is stopped). When this operation is complete, the contents of key input pins (K_3 to K_0) can be directly read with a KI or KIN instruction.

5.2 LCD PINS USED FOR KEY SOURCE

To output key source signals from the LCD pins, the KLE of the LCD control digit must be set to allow the device to enter the key source output mode. When this occurs, the LCD display data and key source signals are output form the LCD pins according to the time division. Since the program is asynchronous with the key source signal output, the key latch data can be read by the program by executing a KI or KIN instruction after a TKLT or TKLF instruction. The state of the key input pin (K_3 to K_0) when the key source signal is output from the LCD pin is latched in the key latch. Figure 5-2 illustrates the concept behind these operations.

5.3 GENERAL-POUPOSE PORTS AND THE LCD PINS USED AS THE KEY SOURCE

In the third key matrix configuration, both general-purpose ports and LCD pins are used for the key source.

This is a combination of the first and second key matrix configurations. In this configuration, the general-purpose ports (port C) and the LCD pins are used for the key source of the key matrix. In this usage, momentary switches must be provided for port C and the other switches must be provided for the LCD pins.

Figure 5-4 shows an example of this key matrix configuration.

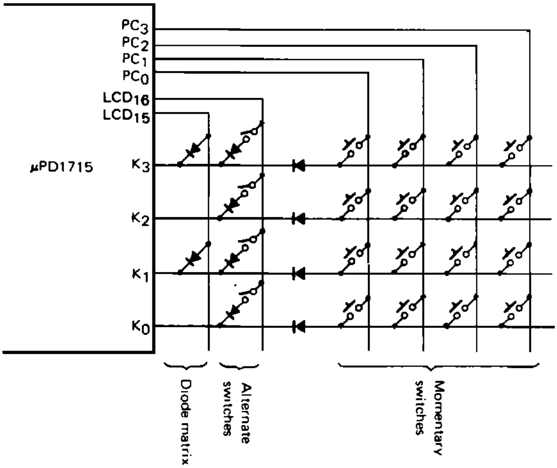


Fig. 5.4 Example of a key matrix configuration using general-purpose ports and LCD pins for the key source

When reading the key input signal of the momentary key, LCD pins must be set to low level for preventing that the input signal of diode and alternate key is read.

In Fig. 5-4, using the following program for reading key input signal of the momentary key.

Example:

```
        :
    BANK0
    MVI      01H, 1100B ; }  LCD pins are used as key source signal outputs
    LCDD     01H, 0FH   ; }
   *SPB      2, 1111B   ;    Port C is output
    MVI      02H, 0011B ; ]
    MVI      03H, 0111B ; |
    BANK2               ; |  Key source signal is output from LCD pins
    OUT      0, 03H     ; |  Key source signal of LCD9 to LCD16 pin is all low level
    OUT      1, 02H     ; |
    BANK0               ; ]
    TKLT                ; }  Remain in the wait state during key source signal latch time.
    JMP      $-1        ; }
    KI       04H        ;    Read the momentary key return signal
        :
```

* Port C must be output befor key source signal of LCD pin is output.
If port C is output after key source signal of LCD pin is output, the key source signal is not exactly read.

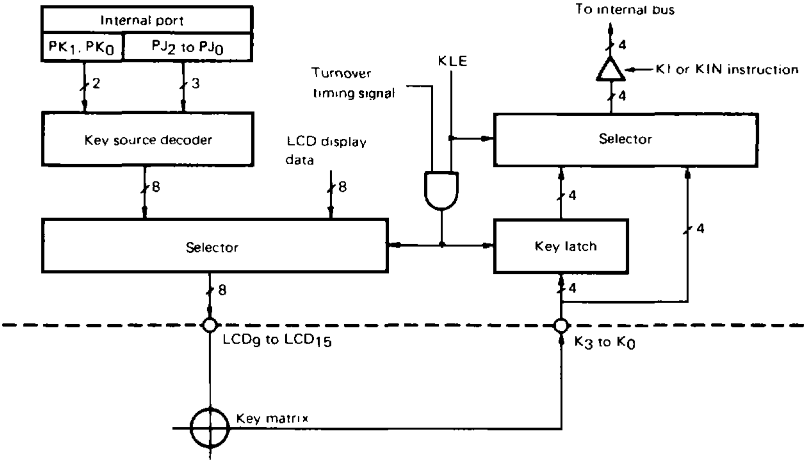


Fig. 5-2 Concept of key input operations using LCD pins for key source

The key source signal is output at a high level for 133 μs every 6.7 ms. The key source signal output from the LCD pin is specified for internal ports: Port J (address 00B in BANK2) and port K (address 01B in BANK2).

Figure 5-3 shows an example of the key matrix configuration when only the LCD pins are used for the key source.

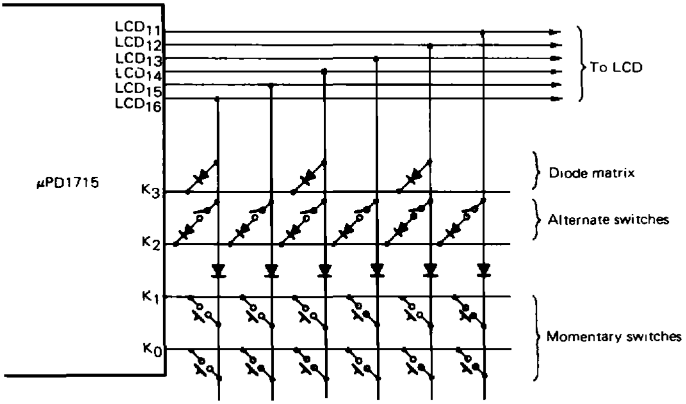


Fig. 5-3 Example of the key matrix configuration using the LCD pins as the key source

With this key matrix configuration, it must be remembered that the signal output when a key is pressed should not be transferred to the other LCD pins. If the signal output when a key is pressed is transferred to other LCD pins, the LCD driving signal waveform is disturbed and an erroneous display may result.

For this reason, stage diodes for preventing such a roundabout signal are necessary between the LCD pins and the key matrix when the key matrix is configured as shown in Fig. 5-1. Since only a voltage drop corresponding to a stage of the diode is allowed in the μPD1715, the key matrix cannot be configured as shown in Fig. 5-1.

Figure 5-3 shows the key matrix configuration obtained when the facts explained above are considered.

The data input to the two high-order bits of the key source decoder via PK_1 and PK_0 is called phase, whereas the bit input to each of the three low-order bits of the key source decoder, PJ_2 to PJ_0 is called the key source bit. The data output from the key source decoder is specified by the phase and key source bits. The phase is used especially to indicate the key scanning stage for the binary search method.

In the following key search program example, the key source decoder operates using the binary search method by using LCD_9 to LCD_{16} as the key source.

5-4 KEY SOURCE DECODER

The μPD1715 allows the use of the LCD pins (LCD_9 to LCD_{16}) for the key source. In this case, the key source signal is output at 6.7 ms intervals for 133 μs. In all the keys on these eight key source lines are assumed to be scanned during this timing, a maximum of 53.6 ms is required to detect the key position after a key is pressed.

The μPD1715 has an integrated key source decoder to minimize the key position detecting time. The key source decoder permits detecting of the key position by use of the binary search method.

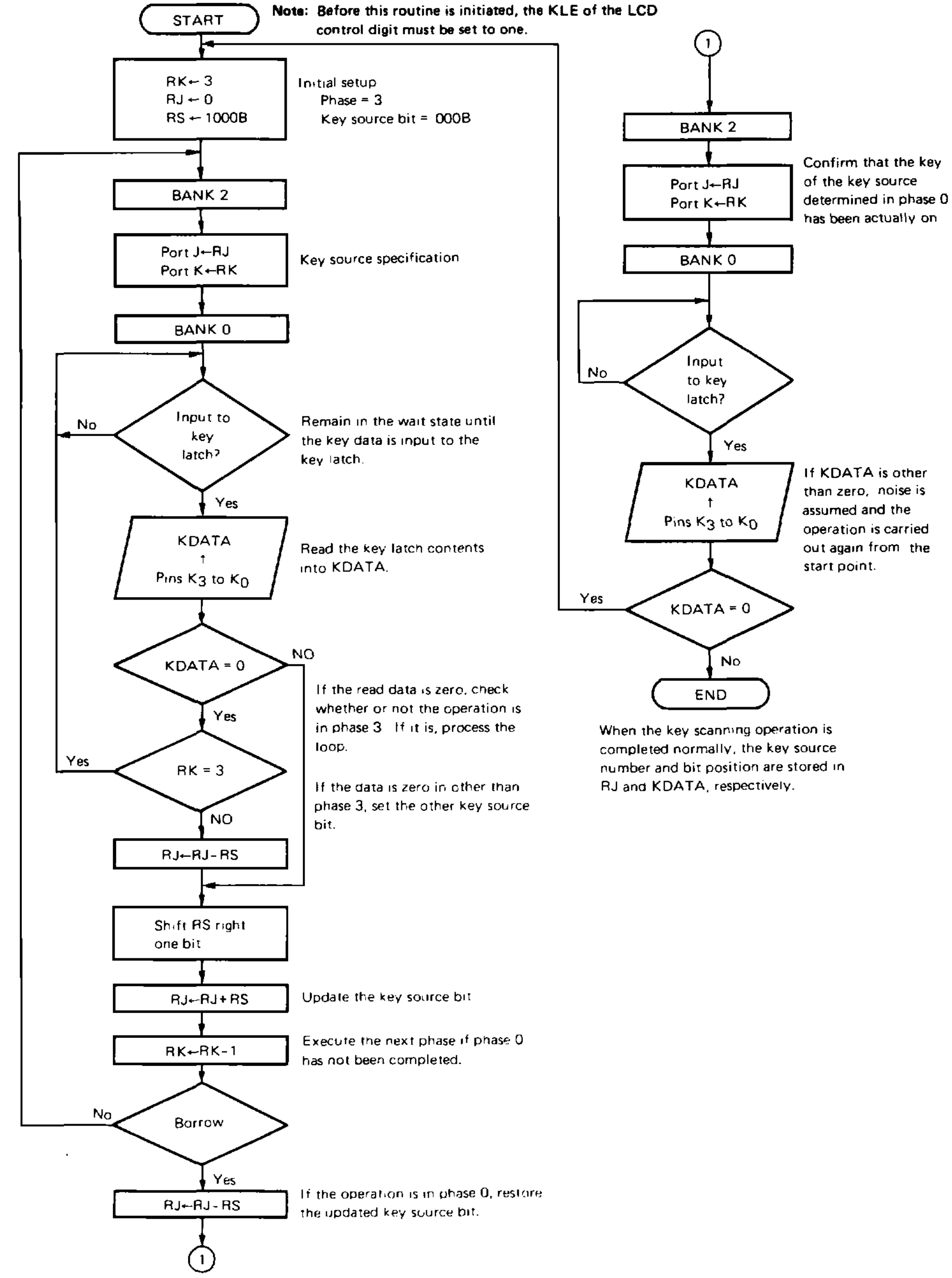
The key source decoder has 5-bit input and 8-bit output. The two high-order bits of the input are connected to the internal ports, PK_1 and PK_0; and the three low-order bits are connected to PJ_2, PJ_1, and PJ_0. Table 5-1 outlines the decode table of the key source decoder.

Table 5-1 Key source (LCD pin) decode table

Decoder input				LCD pins							
PK	PJ			16	15	14	13	12	11	10	9
11	0	0	0	▨	▨	▨	▨	▨	▨	▨	▨
	1	1	1								
10	0	0	0					▨	▨	▨	▨
	1	0	0	▨	▨	▨	▨				
01	0	0	0							▨	▨
	0	1	0					▨	▨		
	1	0	0			▨	▨				
	1	1	0	▨	▨						
00	0	0	0								▨
	0	0	1							▨	
	0	1	0						▨		
	0	1	1					▨			
	1	0	0				▨				
	1	0	1			▨					
	1	1	0		▨						
	1	1	1	▨							

Note: The shading indicates that the key source signal is output to the pertinent pin.

5.5 KEY SEARCH PROGRAM EXAMPLE (Binary Search Method)



Note: Before this routine is initiated, the KLE of the LCD control digit must be set to one.

Initial setup
Phase = 3
Key source bit = 000B

Key source specification

Remain in the wait state until the key data is input to the key latch.

Read the key latch contents into KDATA.

If the read data is zero, check whether or not the operation is in phase 3 If it is, process the loop.

If the data is zero in other than phase 3, set the other key source bit.

Update the key source bit

Execute the next phase if phase 0 has not been completed.

If the operation is in phase 0, restore the updated key source bit.

Confirm that the key of the key source determined in phase 0 has been actually on

If KDATA is other than zero, noise is assumed and the operation is carried out again from the start point.

When the key scanning operation is completed normally, the key source number and bit position are stored in RJ and KDATA, respectively.

6. PROGRAMMABLE LOGIC ARRAY (PLA)

The µPD1715 includes the segment PLA to be controlled by a user program. Ordinarily, the display patterns of the LCD panel are programmed in the segment PLA. Up to 32 patterns (16 x 2) can be generated. As explained before, the segment PLA is selected only when an even-numbered position is specified by an LCDD instruction. (See Section 4 "LCD Driver" for details.)

6-1 SEGMENT PLA CONFIGURATION

Figure 6-1 shows the segment PLA configuration.

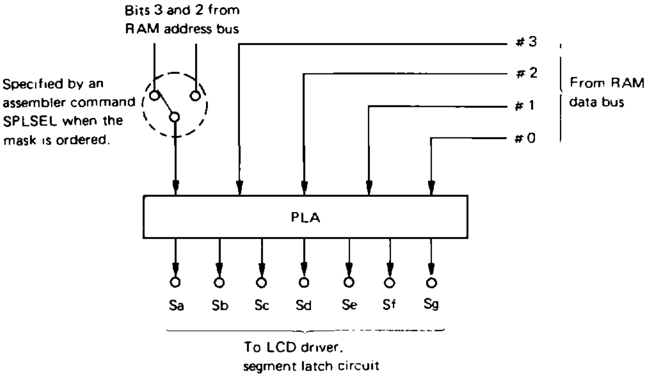
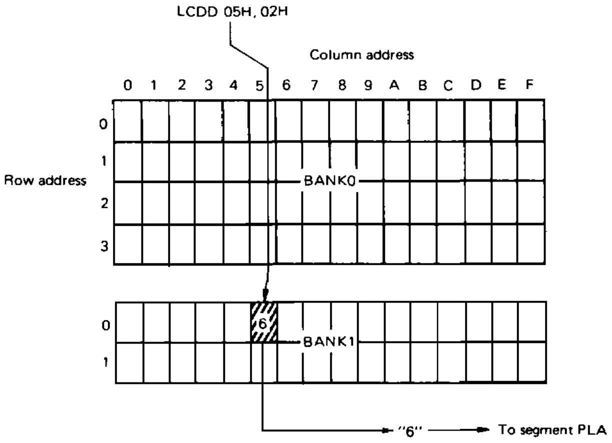

Bits 3 and 2 from
RAM address bus
Specified by an assembler command SPLSEL when the mask is ordered.
#3
#2
#1
#0
From RAM data bus
PLA
Sa
Sb
Sc
Sd
Se
Sf
Sg
To LCD driver, segment latch circuit

Fig. 6-1 Segment PLA configuration

The contents of data memory (RAM) addressed by the first operand of the LCDD instruction are input to the four low-order bits of segment PLA. For example, when an LCDD instruction is executed with the following RAM contents, the data at address 05H of BANK1 in the data memory (RAM), that is, value 6 is input.



Note: Since the RAM address in BANK1 is accessed, the BANK1 instruction must be executed before the LCDD instruction.

CODING EXAMPLE

```
KEYSCAN:
            MVI      RK, 3       ;  RK = Phase Data
            MVI      RJ, 0
            MVI      RS, 1000B   ;  RS = Key Source bit
KSOUT1:
            BANK2
            OUT      PJ, RJ      ;  Key source specification
            OUT      PK, RK
            BANK0
WAIT:
            TKLT                 ;  Remain in the wait state until the key data is input to the key latch.
            JMP      WAIT

            KIN      KDATA       ;  KDATA ← Key Latch Data
            JMP      RSHIFT      ;  Go to RSHIFT if the key data is input.
            SNEI     RK, 3       ;  If PHASE's data is 3, process the loop until the key data is input.
            JMP      WAIT

            SU       RJ, RS      ;  Key source bit is set just before, it is reset.
RSHIFT:
            MVI      RC, 2       ;  Shift contents of RS left 3 bits.
SFTLOOP:
            ADN      RS, RS
            ORI      RS, 1
            SIS      RC, 1
            JMP      SFTLOOP

            AD       RJ, RS      ;  OR the shifted bit at key source bit.

            SIS      RK, 1       ;  Update the PHASE and go to KSOUT1,
            JMP      KSOUT1      ;  if PHASE0 has not been completed.

            SU       RJ, RS

            BANK2                ;  Confirm that the key of the key source determined  in phase 0 has
            RPB      PK, 0FH     ;  been actually on.
            OUT      PJ, RJ
            BANK0

            TKLT                 ;  Wait until the data is latched at key latch.
            JMP      $-1

            KIN      KDATA
            JMP      SCNEND      ;  Scan operation is completed if KDATA is not 0.
                                 ;  The segment number of pressed the key is input to KDATA.
            JMP      KEYSCAN     ;  If KDATA is ZERO, noise is assumed and the operation is carried
                                 ;  out again from the start point.
```

The contents of bit 3 or 2 at the RAM column address specified by the LCDD instruction is latched in the most-significant bit of the segment PLA circuit. The bit to be latched must be specified when the device mask is ordered. (See Section 6-4 PLA program example for details.) When bit 3 is specified, "0" is input to the most-significant bit of the segment PLA if the RAM at column address 00H to 07H is specified by the LCDD instruction and "1" is input if address 08H to 0FH is specified. When bit 2 is specified, "0" is input to the most-significant bit of the segment PLA if address 00H to 03H or 08H to 0BH is specified and "1" is input if address 04H to 07H or 0CH to 0FH is specified.

The 32 segment PLA patterns are classified into two pattern groups, each consisting of 16 patterns according to the data input to the most-significant bit of the segment PLA. Consequently, even if the RAM data contents are the same, two types of display patterns can be generated by changing the RAM column address contained in the LCDD instruction.

The 16 patterns that can be generated when the most-significant bit of segment PLA is "0" are called pattern group 0, whereas those generated when the most-significant bit is "1" are called pattern group 1.

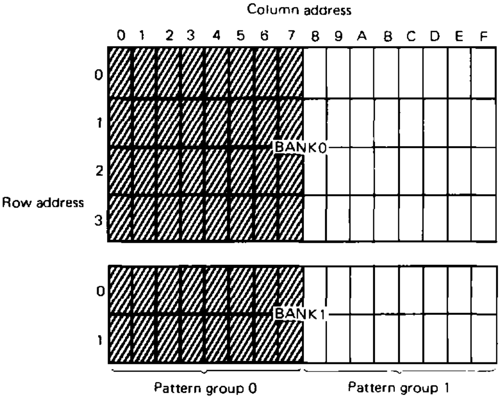


Fig. 6-2 Pattern groups when SPLSEL is specified for bit 3

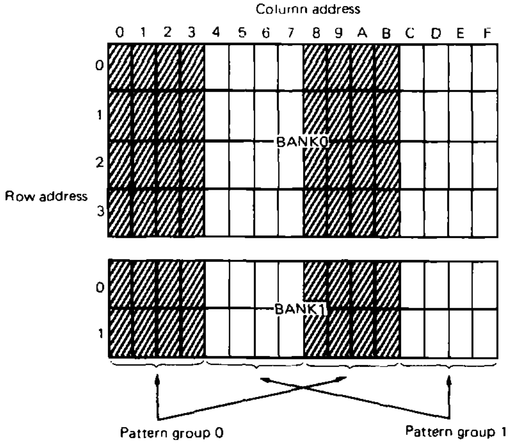


Fig. 6-3 Pattern groups when SPLSEL is specified for bit 2

These pattern group divisions are determined by considering RAM or program efficiency when a program is created.

An SPLSEL pseudo instruction is used to specify bit 3 or 2 to be input to the most-significant bit of the segment PLA:

SPLSEL 3 or, SPLSEL 2

(See Section 6.4 PLA program example for details.)

6.2 SEGMENT PLA PATTERN EXAMPLES

Tables 6-1 and 6-2 outline examples of pattern groups 0 and 1, respectively.

Table 6-1 Example of pattern group 0

Segment PLA input					Segment output							Output pattern
					g	f	e	d	c	b	a	
0	0	0	0	0	0	1	1	1	1	1	1	0
	0	0	0	1	0	0	0	0	1	1	0	1
	0	0	1	0	1	0	1	1	0	1	1	2
	0	0	1	1	1	0	0	1	1	1	1	3
	0	1	0	0	1	1	0	0	1	1	0	4
	0	1	0	1	1	1	0	1	1	0	1	5
	0	1	1	0	1	1	1	1	1	0	1	6
	0	1	1	1	0	1	0	0	1	1	1	7
	1	0	0	0	1	1	1	1	1	1	1	8
	1	0	0	1	1	1	0	1	1	1	1	9
	1	0	1	0	0	0	0	0	0	0	0	Blank (display off)
	1	0	1	1	1	1	1	1	0	0	1	E
	1	1	0	0	0	1	1	1	0	0	1	C
	1	1	0	1	1	1	1	0	1	1	0	H
	1	1	1	0	1	1	1	0	0	1	1	P
	1	1	1	1	1	0	0	0	0	0	0	-

Table 6-2 Example of pattern group 1

Segment PLA input					Segment output							Output pattern
					g	f	e	d	c	b	a	
1	0	0	0	0	1	0	0	0	0	1	0	0 SEC OFF
	0	0	0	1	0	1	0	0	0	1	0	5 SEC OFF
	0	0	1	0	0	0	1	0	0	0	0	SEC
	0	0	1	1	0	0	0	0	0	0	0	NO USE
	0	1	0	0	0	0	0	0	0	0	0	NO USE
	0	1	0	1	0	0	0	0	0	0	0	NO USE
	0	1	1	0	0	0	0	0	0	0	0	NO USE
	0	1	1	1	0	0	0	0	0	0	0	NO USE
	1	0	0	0	0	0	0	0	0	0	0	NO USE
	1	0	0	1	0	0	0	0	0	0	0	NO USE
	1	0	1	0	0	0	0	0	0	0	0	NO USE
	1	0	1	1	0	0	0	0	0	0	0	NO USE
	1	1	0	0	0	0	0	0	0	0	0	NO USE
	1	1	0	1	0	0	0	0	0	0	0	NO USE
	1	1	1	0	0	0	0	0	0	0	0	NO USE
	1	1	1	1	0	0	0	0	0	0	0	NO USE

6.3 DISPLAY PROGRAM EXAMPLE

In the following program example, the LCD panel shown in Fig. 6-4 is used to display PLA patterns listed in Tables 6-1 and 6-2. It is assumed that bit 2 (SPLSEL 2) is specified as the most-significant bit of the segment latch.

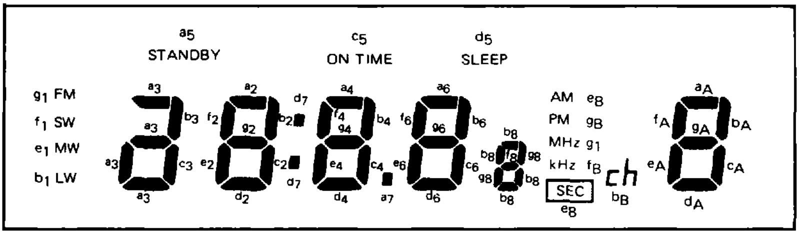
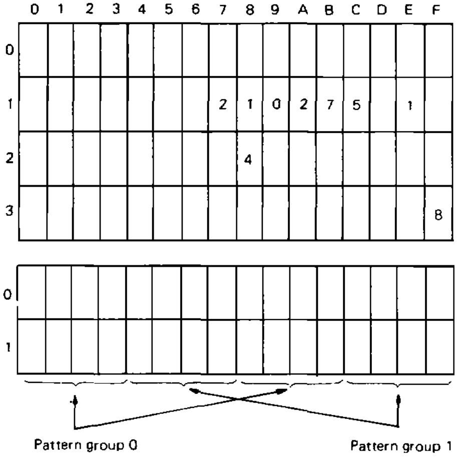


Fig. 6-4 LCD panel example



	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1								2	1	0	2	7	5		1	
2									4							
3																8

0																
1																

Pattern group 0

Pattern group 1

```
LCDD    17H, 01H    ;  "FM", "MHz" Display data set
LCDD    18H, 00H    ;  "1" Frequency data set
LCDD    19H, 02H    ;  "0" Frequency data set
LCDD    1AH, 04H    ;  "2" Frequency data set
LCDD    1BH, 06H    ;  "7" Frequency data set
LCDD    1CH, 08H    ;  "5" Frequency data set
LCDD    1DH, 03H    ;  "ch" Display data set
LCDD    1EH, 07H    ;  DECIMAL POINT Display data set
LCDD    18H, 0AH    ;  "4" PRESET STATION NO. Display data set
LCDD    3FH, 0FH    ;  ALL DIGITS ON
```

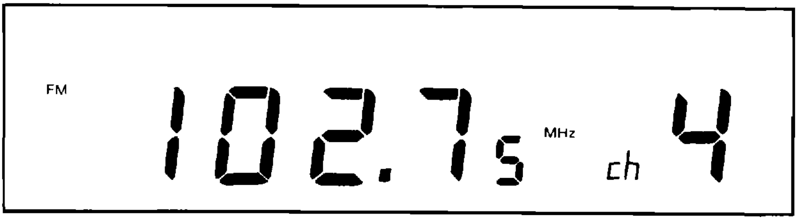
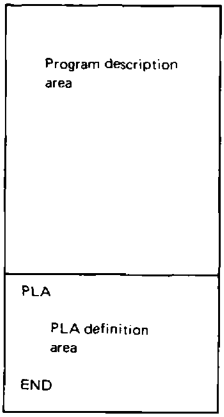


Fig. 6-5 Display example

6.4 PLA PROGRAM EXAMPLE

The PLA definition is required for all μPD1700 series devices. If the PLA section is not defined, the tape order cannot be accepted. The PLA definition is placed at the end of an assembler source program and contains the following items. All of these items are required, that is, none of the items can be dispensed with.



(1) PLA pseudo instruction

Indicates the beginning of the PLA definition area immediately after the end of the program description area.

(2) Segment PLA Select (SPLSEL) pseudo instruction

Selects the RAM address division for generating segment pattern groups 0 and 1. The following two instruction formats are available:

SPLSEL 3 and SPLSEL 2

(3) Define Segment PLA (DSP) pseudo instruction

Defines 32 segment PLA patterns. The patterns must be defined beginning with the 16 patterns in pattern group 0. The following is an example of a pattern definition. The first specified bit corresponds to segment g and the subsequent bits correspond to segments f, e, d, c, b, and a in this order.

```
DSP      1 1 1 1 0 0 1 B
         \           \
          g           a
```

(4) END

Indicates the end of the source program immediately after the PLA definition area has ended. If this instruction is omitted, the program is not assembled.

Note 1: The digit PLA definition is also required for the μPD1700 series devices having the digit PLA. These include the μPD1701, μPD1703, μPD1704, μPD1705, μPD1707, μPD1710, μPD1711, and the μPD1712.

A define Digit PLA (DDP) pseudo instruction is used to define the digit PLA.

Similarly, the MTDIG definition is required for devices having the digit pin. These include the μPD1701, μPD1703, μPD1704, μPD1705, μPD1707, μPD1709, μPD1710, μPD1711, and μPD1712.

Note 2: The PLA definition begins with PLA and ends with END. The user may specify SPLSEL, DSP, DDP, and MTDIG between PLA and END in an arbitrary order.

PLA program example

```
;*****PLA DEFINITION*****
PLA
;
SPLSEL 2
;
;***SEGMENT PATTERN 0***
;
;          gfedcba
DSP        0111111B              ;0
DSP        0000110B              ;1
DSP        1011011B              ;2
DSP        1001111B              ;3
DSP        1100110B              ;4
DSP        1101101B              ;5
DSP        1111101B              ;6
DSP        0100111B              ;7
DSP        1111111B              ;8
DSP        1101111B              ;9
DSP        0000000B              ;BLANK
DSP        1111001B              ;E
DSP        0111001B              ;C
DSP        1110110B              ;H
DSP        1110011B              ;P
DSP        1000000B              ;-
;
;***SEGMENT PATTERN 1***
;
DSP        1000010B              ;0 (FM 50 kHz), ' SEC ' - OFF
DSP        0100010B              ;5 (FM 50 kHz), ' SEC ' - OFF
DSP        0010000B              ; SEC
DSP        0000000B              ;NO USE
DSP        0000000B              ;NO USE
DSP        0000000B              ;NO USE
DSP        0000000B              ;NO USE
DSP        0000000B              ;NO USE
DSP        0000000B              ;NO USE
DSP        0000000B              ;NO USE
DSP        0000000B              ;BLANK
DSP        0000000B              ;NO USE
DSP        0000000B              ;NO USE
DSP        0000000B              ;NO USE
DSP        0000000B              ;NO USE
DSP        0000000B              ;NO USE
;
;
END
```

7. INSTRUCTION

7.1 µPD1715 INSTRUCTION SET

b_{15} b_{14}		0 0	0 1	1 0	1 1
b_{13} b_{12} b_{11} b_{10}		0	1	2	3
0 0 0 0	0	NOP VHF HF	KIN M KI M	————	ST M, r
0 0 0 1	1	SPB P, N SS N_1 BANK1 BANK2 STC	ORI M, I	————	MVRS M, r
0 0 1 0	2	JMP ADDR (page 1)	MVI M, I	OUT P, r	IN r, P
0 0 1 1	3	RPB P, N RS N_1 BANK0 RSC	ANI M, I	CKSTP	MVRD r, M
0 1 0 0	4	RT	AI M, I	MVSR M_1, M_2	AD r, M
0 1 0 1	5	RTS	SI M, I	EXL r, M	SU r, M
0 1 1 0	6	JMP ADDR (page 0)	AIC M, I	LD r, M	AC r, M
0 1 1 1	7	CAL ADDR (page 0)	SIB M, I	LCDD M, D	SB r, M
1 0 0 0	8	TPF P, N TCEF	AIN M, I	TKLF TKLT	ADN r, M
1 0 0 1	9	TPT P, N TCET	SIN M, I	TTM TIP	SUN r, M
1 0 1 0	A	TMF M, N	AICN M, I	TUL	ACN r, M
1 0 1 1	B	TMT M, N	SIBN M, I	PLL M, r	SBN r, M
1 1 0 0	C	SLTI M, I	AIS M, I	SLT r, M	ADS r, M
1 1 0 1	D	SGEI M, I	SIS M, I	SGE r, M	SUS r, M
1 1 1 0	E	SEQI M, I	AICS M, I	SEQ r, M	ACS r, M
1 1 1 1	F	SNEI M, I	SIBS M, I	SNE r, M	SBS r, M

7.2 INSTRUCTIONS

NOTE : D_H : Data memory address high (row address) (2 bits
D_L : Data memory address low (column address) (4 bits)
Rn : Register number (4 bits)
I : Immediate data (4 bits)
N : Bit position (4 bits)
ADDR : Program memory address (10 bits)
—— : All "1"
r : General register
One of addresses 00−0FH of BANK0

M : Data memory address
One of 00−3FH of BANK0 and address 00−1FH of BANK1
P : Port, $0 \leq P \leq 3$
N_1 : Bit position of status word 1 $0 \leq N_1 \leq 7$
( ) : Contents of register or memory
c : Carry
b : Borrow
( )n : Contents on bit n of register or memory
h : Halt release conditions $0 \leq h \leq 7$

	Mnemonic	Operand		Function	Operation	Machine code			
		1ST	2ND			Operation code			
Addition	AD	r	M	Add memory to register	r ← (r) + (M)	1 1 0 1 0 0	D_H	D_L	Rn
	ADS	r	M	Add memory to register, then skip if carry	r ← (r) + (M) skip if carry	1 1 1 1 0 0	D_H	D_L	Rn
	ADN	r	M	Add memory to register, then skip if not carry	r ← (r) + (M) skip if not carry	1 1 1 0 0 0	D_H	D_L	Rn
	AC	r	M	Add memory to register with carry	r ← (r) + (M) + c	1 1 0 1 1 0	D_H	D_L	Rn
	ACS	r	M	Add memory to register with carry, then skip if carry	r ← (r) + (M) + c skip if carry	1 1 1 1 1 0	D_H	D_L	Rn
	ACN	r	M	Add memory to register with carry, then skip if not carry	r ← (r) + (M) + c skip if not carry	1 1 1 0 1 0	D_H	D_L	Rn
	AI	M	I	Add immediate data to memory	M ← (M) + I	0 1 0 1 0 0	D_H	D_L	I
	AIS	M	I	Add immediate data to memory, then skip if carry	M ← (M) + I skip if carry	0 1 1 1 0 0	D_H	D_L	I
	AIN	M	I	Add immediate data to memory, then skip if not carry	M ← (M) + I skip if not carry	0 1 1 0 0 0	D_H	D_L	I
	AIC	M	I	Add immediate data to memory with carry	M ← (M) + I + c	0 1 0 1 1 0	D_H	D_L	I
	AICS	M	I	Add immediate data to memory with carry, then skip if carry	M ← (M) + I + c skip if carry	0 1 1 1 1 0	D_H	D_L	I
	AICN	M	I	Add immediate data to memory with carry, then skip if not carry	M ← (M) + I + c skip if not carry	0 1 1 0 1 0	D_H	D_L	I
Subtraction	SU	r	M	Subtract memory from register	r ← (r) − (M)	1 1 0 1 0 1	D_H	D_L	Rn
	SUS	r	M	Subtract memory from register, then skip if borrow	r ← (r) − (M) skip if borrow	1 1 1 1 0 1	D_H	D_L	Rn
	SUN	r	M	Subtract memory from register, then skip if not borrow	r ← (r) − (M) skip if not borrow	1 1 1 0 0 1	D_H	D_L	Rn
	SB	r	M	Subtract memory from register with borrow	r ← (r) − (M) − b	1 1 0 1 1 1	D_H	D_L	Rn
	SBS	r	M	Subtract memory from register with borrow, then skip if borrow	r ← (r) − (M) − b skip if borrow	1 1 1 1 1 1	D_H	D_L	Rn
	SBN	r	M	Subtract memory from register with borrow, skip if not borrow	r ← (r) − (M) − b skip if not borrow	1 1 1 0 1 1	D_H	D_L	Rn
	SI	M	I	Subtract immediate data from memory	M ← (M) − I	0 1 0 1 0 1	D_H	D_L	I
	SIS	M	I	Subtract immediate data from memory, then skip if borrow	M ← (M) − I skip if borrow	0 1 1 1 0 1	D_H	D_L	I
	SIN	M	I	Subtract immediate data from memory, then skip if not borrow	M ← (M) − I skip if not borrow	0 1 1 0 0 1	D_H	D_L	I
	SIB	M	I	Subtract immediate data from memory with borrow	M ← (M) − I − b	0 1 0 1 1 1	D_H	D_L	I
	SIBS	M	I	Subtract immediate data from memory with borrow, then skip if borrow	M ← (M) − I − b skip if borrow	0 1 1 1 1 1	D_H	D_L	I
	SIBN	M	I	Subtract immediate data from memory with borrow, then skip if not borrow	M ← (M) − I − b skip if not borrow	0 1 1 0 1 1	D_H	D_L	I

	Mnemonic	Operand		Function	Operation	Machine code			
		1ST	2ND			Operation code			
Comparison	SEQ	r	M	Skip if register equals memory	r − M skip if zero	1 0 1 1 1 0	D_H	D_L	Rn
	SNE	r	M	Skip if register not equals memory	r − M skip if not zero	1 0 1 1 1 1	D_H	D_L	Rn
	SGE	r	M	Skip if register is greater than or equal to memory	r − M skip if not borrow (r) ≧ (M)	1 0 1 1 0 1	D_H	D_L	Rn
	SLT	r	M	Skip if register is less than memory	r − M skip if borrow (r) < (M)	1 0 1 1 0 0	D_H	D_L	Rn
	SEQI	M	I	Skip if memory equals immediate data	M − I skip if zero	0 0 1 1 1 0	D_H	D_L	I
	SNEI	M	I	Skip if memory not equals immediate data	M − I skip if not zero	0 0 1 1 1 1	D_H	D_L	I
	SGEI	M	I	Skip if memory is greater than or equal to immediate data	M − I skip if not borrow (M) ≧ I	0 0 1 1 0 1	D_H	D_L	I
	SLTI	M	I	Skip if memory is less than immediate data	M − I skip if borrow (M) < I	0 0 1 1 0 0	D_H	D_L	I
Logical operation	ANI	M	I	Logic AND of memory and immediate data	$M \leftarrow (M) \wedge I$	0 1 0 0 1 1	D_H	D_L	I
	ORI	M	I	Logic OR of memory and immediate data	$M \leftarrow (M) \vee I$	0 1 0 0 0 1	D_H	D_L	I
	EXL	r	M	Exclusive OR Logic of memory and register	r ← (r)/+ (M)	1 0 0 1 0 1	D_H	D_L	Rn
Transfer	LD	r	M	Load memory to register	r ← (M)	1 0 0 1 1 0	D_H	D_L	Rn
	ST	M	r	Store register to memory	M ← (r)	1 1 0 0 0 0	D_H	D_L	Rn
	MVRD	r	M	Move memory to destination memory referring to register in the same row	$\{D_H, Rn\} \leftarrow (M)$	1 1 0 0 1 1	D_H	D_L	Rn
	MVRS	M	r	Move source memory referring to register to memory in the same row	$M \leftarrow \{D_H, Rn\}$	1 1 0 0 0 1	D_H	D_L	Rn
	MVSR	M_1	M_2	Move memory to memory in the same row	$\{D_H, DL_1\} \leftarrow \{D_H, DL_2\}$	1 0 0 1 0 0	D_H	D_{L1}	D_{L2}
	MVI	M	I	Move immediate data to memory	M ← I	0 1 0 0 1 0	D_H	D_L	I
	PLL	M	r	Load N0 ~ N3, N_F & memory to PLL registers	PLLR ← (N0 ~ N3), N_F & (M)	1 0 1 0 1 1	D_H	D_L	Rn
Bit test	TMT	M	N	Test memory bits, then skip if all bits specified are true	if M(N) = all "1", then skip	0 0 1 0 1 1	D_H	D_L	N
	TMF	M	N	Test memory bits, then skip if all bits specified are false	if M(N) = all "0", then skip	0 0 1 0 1 0	D_H	D_L	N
Jump	JMP	ADDR		Jump to the address specified in page 0	PC←ADDR in page 0	0 0 0 1 1 0	ADDR(10 bits)		
				Jump to the address specified in page 1	PC←ADDR in page 1	0 0 0 0 1 0			
Subroutine	CAL	ADDR		Call subroutine in page 0	Stack←[(PC)+1, PAGE], PC←ADDR PAGE←0	0 0 0 1 1 1	ADDR(10 bits)		
	RT			Return to main routine	PC←(stack)	0 0 0 1 0 0	–	–	–
	RTS			Return to main routine, then skip unconditionary	PC←(stack), and skip	0 0 0 1 0 1	–	–	–

F/F test	TTM			Test and reset timer F/F, then skip if it has not been set	if Timer F/F = 1, then Timer F/F←0
					if Timer F/F = 0, then skip
						1 0 1 0 0 1	–	–	–

	TUL			Test and reset unlock F/F, then skip if it has not been set	if UL F/F = 1, then UL F/F←0
					if UL F/F = 0, then skip
						1 0 1 0 1 0	–	–	–

	TKLT			Test and reset key latch F/F, then skip if true	if KL F/F = 1, then skip and KL F/F←0	1 0 1 0 0 0	1 1	0 0 0 1	–

	TKLF			Test and reset key latch F/F, then skip if false	if KL F/F = 1, then KL F/F←0
					if KL F/F = 0, then skip
						1 0 1 0 0 0	0 1	0 0 0 1	–

Timer test	TIP			Test interval pulse, then skip if low	if IPG = 0, then skip	1 0 1 0 0 1	–	0 0 0 0	0 0 0 0

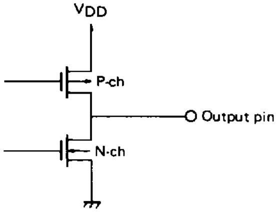
	Mnemonic	Operand		Function	Operation	Machine code			
		1ST	2ND			Operation code			
Status word and terminal test	SS	N_1		Set status word 1	(STATUS WORD 1)$_N$←1	0 0 0 0 0 1	–	0 N_1	–
	RS	N_1		Reset status word 1	(STATUS WORD 1)$_N$←0	0 0 0 0 1 1	–	0 N_1	–
	STC			Set carry F/F	carry F/F←1	0 0 0 0 0 1	–	0 0 1 0	–
	RSC			Reset carry F/F	carry F/F←0	0 0 0 0 1 1	–	0 0 1 0	–
	BANK0			Select BANK0	BANK F/F1←0, BANK F/F2←0	0 0 0 0 1 1	–	1 1 0 0	–
	BANK1			Select BANK1	BANK F/F1←1, BANK F/F2←0	0 0 0 0 0 1	–	0 1 0 0	–
	BANK2			Select BANK2	BANK F/F1←0, BANK F/F2←1	0 0 0 0 0 1	–	1 0 0 0	–
	TCET			Test CE, skip if true	if CE=1, then skip	0 0 1 0 0 1	–	0 0 1 0	–
	TCEF			Test CE, skip if false	if CE=0, then skip	0 0 1 0 0 0	–	0 0 1 0	–
Input / output	LCDD	M	D	Output memory to LCD DIG "D" directly	LCD(D)←SEGPLA←(M) or LCD(D)←(M)	1 0 0 1 1 1	D_H	D	D_L
	KI	M		Input key data to memory	M←K_{0-3}	0 1 0 0 0 0	D_H	D_L	0 0 0 0
	KIN	M		Input key data to memory, then skip if data are zero	M←K_{0-3}, skip if (M)=0	0 1 0 0 0 0	D_H	D_L	–
	IN	r	P	Input data on port to register	r←(Port (P))	1 1 0 0 1 0	P	–	Rn
	OUT	P	r	Output contents of register to port	(Port(P))←(r)	1 0 0 0 1 0	P	–	Rn
	SPB	P	N	Set port bits	(Port(P))$_N$←1	0 0 0 0 0 1	P	0 0 0 0	N
	RPB	P	N	Reset port bits	(Port(P))$_N$←0	0 0 0 0 1 1	P	0 0 0 0	N
	TPT	P	N	Test port bits, then skip if all bits specified are true	if (Port(P))$_N$=all 1s, then skip	0 0 1 0 0 1	P	0 0 0 0	N
	TPF	P	N	Test port bits, then skip if all bits specified are false	if (Port(P))$_N$=all 0s, then skip	0 0 1 0 0 0	P	0 0 0 0	N
Others	VHF			Connect FM terminal to prescaler via 1/2 divider	FM terminal → 1/2 → prescaler	0 0 0 0 0 0	0 0	0 0 0 0	0 0 0 1
	HF			Connect AM terminal to prescaler directly	AM terminal → prescaler	0 0 0 0 0 0	0 0	0 0 0 0	0 0 0 0
	CKSTP			Clock stop by CE	stop clock if CE=0	1 0 0 0 1 1	–	1 1 1 0	1 1 1 0
	HALT	h		Halt the CPU, Restart by condition h	Halt	1 0 0 0 1 1	0 0	–	h 1
	NOP			No operation		0 0 0 0 0 0	–	–	–

D

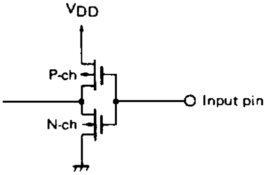
8. INPUT/OUTPUT CIRCUITS

Input/output circuit for different μPD1715 pin are outlined below in simplified format.

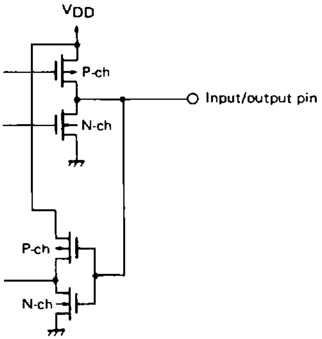
(1) LCD_1 to LCD_{16}, PB_0 to PB_3, PC_0 to PC_3, EO_1, EO_2, CGP and VDP



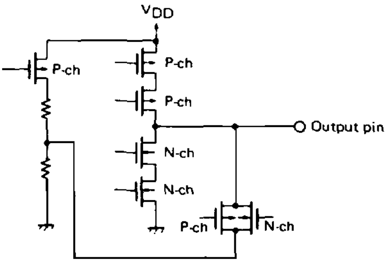
(2) M



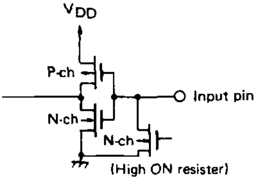
(3) PA_0 to PA_3



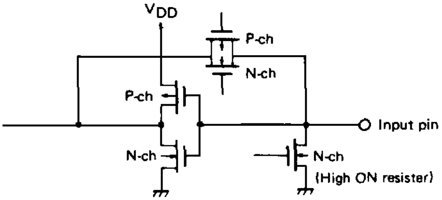
(4) COM$_1$, COM$_2$ and COM$_3$



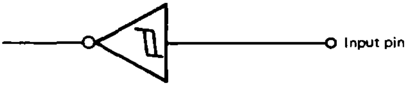
(5) K$_0$ to K$_3$



(6) VCOH and VCOL



(7) CE



Schmitt-Trigger

9. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{DD}	−0.3 to +4.0	V
Input Voltage	V_I	−0.3 to $+V_{DD}$ +0.3	V
Output Voltage	V_O	−0.3 to $+V_{DD}$ +0.3	V
Output Sink Current	I_O	10	mA
Operating Temperature	T_a	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD}	2.0	3.0	3.6	V	
Operating Temperature	T_a	−20		+75	°C	
Input Oscillation Voltage	V_{in}	0.2		V_{DD}	Vp-p	VCOL pin
Input Oscillation Voltage	V_{in}	0.1		V_{DD}	Vp-p	VCOH pin
Data Retention Voltage	V_{DR}	1.5		V_{DD}	V	When the detection of power failure is judged.
Supply Voltage Rising Time	T_{rise}			500	ms	V_{DD}=0 → 1.7 V

DC CHARACTERISTICS (V_{DD}= +1.7 to +3.6 V, T_a = –20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V_{DD1}	2.0	3.0	3.6	V	CPU and PLL operations
Supply Voltage	V_{DD2}	1.9	3.0	3.6	V	CPU and PLL operations, T_a=–20 to +50 °C
Supply Voltage	V_{DD3}	1.7	3.0	3.6	V	CPU operation
Supply Current	I_{DD1}		8	12	mA	VCOH pin, 120 MHz 0.2 Vp-p since wave signal input (V_{DD}=3 V)
Supply Current	I_{DD2}			30	μA	CPU operation (when excution HALT instruction) (V_{DD}=3 V, T_a=25 °C)
Minimum Data Retention Voltage	V_{DR}	1.5		V_{DD}	V	When the detection of power failure is judged by TTM instruction excution
Data Retention Current	I_{DR}			3	μA	When clock oscillation is stopped. V_{DD}=3 V
High Level Output Current	I_{OH1}	–0.5			mA	PA_0 to PA_3, PB_0 to PB_3, PC_0 to PC_3, CGP pins, V_{OH}=V_{DD}–1 V
High Level Output Current	I_{OH2}	–0.2			A	EO_1, EO_2, VDP pins, V_{OH}=V_{DD}–1 V
High Level Output Current	I_{OH3}	–50			μA	LCD_1 to LCD_{16} pins, V_{OH}=V_{DD}–1 V
Low Level Output Current	I_{OL1}	0.5			mA	PA_0 to PA_3, PB_2, PB_3, CGP pins, V_{OL}=1 V
Low Level Output Current	I_{OL2}	0.2			A	EO_1, EO_2, VDP pins, V_{OL}=1 V
Low Level Output Current	I_{OL3}	5			μA	LCD_1 to LCD_{16} pins, PB_0, PB_1, PC_0 to PC_3 pins, V_{OL}=1 V
High Level Input Current	I_{IH1}	3		30	μA	K_0 to K_3 pins, V_{IH}=V_{DD}=1.8 V
High Level Input Current	I_{IH2}	40			μA	VCOH, VCOL, XI pins, V_{IH}=V_{DD}=1.8 V
High Level Input Voltage	V_{IH1}	$0.5 \cdot V_{DD}$			V	K_0 to K_3, M pins
High Level Input Voltage	V_{IH2}	$0.8 \cdot V_{DD}$			V	CE, M, PA_0 to PA_3 pins
Low Level Input Voltage	V_{IL1}			$0.1 \cdot V_{DD}$	V	K_0 to K_3 pins
Low Level Input Voltage	V_{IL2}			$0.2 \cdot V_{DD}$	V	CE, M, PA_0 to PA_3 pins
LCD Drive Voltage	V_{DD}-V_{SS3}	3.0	3.1	3.3	V	T_a=25 °C, C_1=0.1 μF, C_2=0.01 μF, LCD pin open
LCD Drive Voltage (Note)	V_{DD}-V_{SS3}	2.8	3.0	3.1	V	T_a=25 °C, C_1=0.1 μF, C_2=0.001 μF, LCD pin open
Output Leakage Current	I_L			+1	μA	EO_1, EO_2 pins

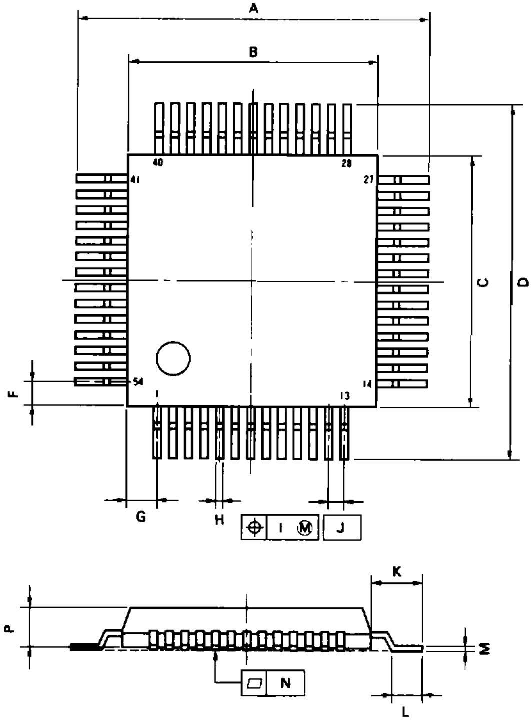
AC CHARACTERISTICS (V_{DD}= +2.0 to +3.6 V, T_a = –20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Operating Frequency	f_{in1}	0.5		15	MHz	VCOL pin, MF mode, Vi=0.1 Vp-p
Operating Frequency	f_{in2}	0.5		40	MHz	VCOL pin, HF mode, Vi=0.2 Vp-p
Operating Frequency	f_{in3}	10		100	MHz	VCOH pin, VHF mode, Vi=0.1 Vp-p, M pin=Low
Operating Frequency	f_{in4}	10		130	MHz	VCOH pin VHF mode, Vi=0.1 Vp-p, M pin=High

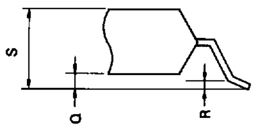
Note: Ratings listed above are subject to change due to provisional characteristics.

10. PACKAGE DIMENSIONS (UNIT: mm)

54-pin plastic QFP



detail of lead end



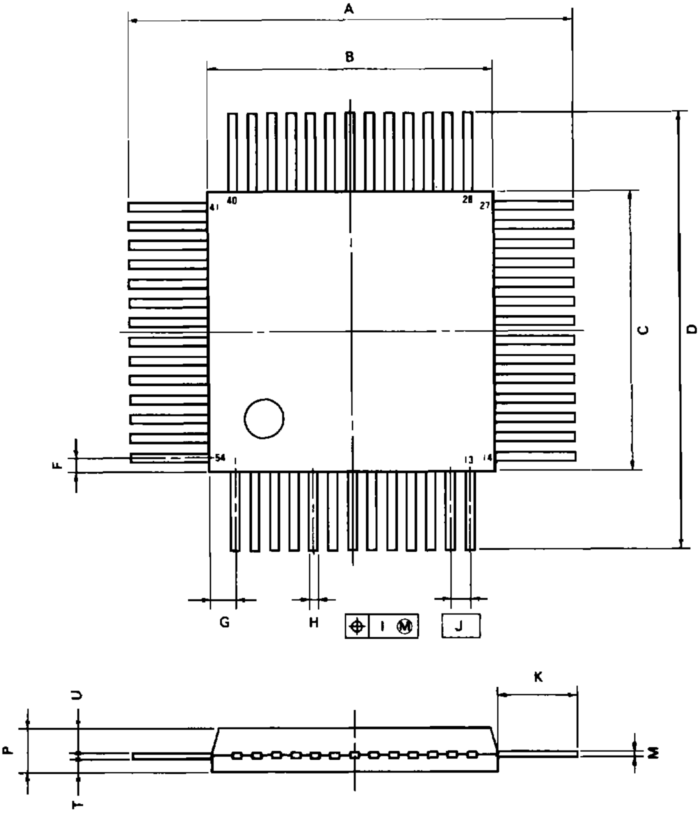
P54G-65-F

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$13.5^{\pm0.4}$	$0.531^{+0.017}_{-0.016}$
B	$9.5^{\pm0.2}$	$0.374^{\pm0.008}$
C	$9.5^{\pm0.2}$	$0.374^{\pm0.008}$
D	$13.5^{\pm0.4}$	$0.531^{+0.017}_{-0.016}$
F	0.5	0.020
G	0.85	0.033
H	$0.30^{\pm0.10}$	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	$2.0^{\pm0.2}$	$0.079^{+0.008}_{-0.009}$
L	$1.2^{\pm0.2}$	$0.047^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	$1.5^{\pm0.1}$	$0.059^{\pm0.004}$
Q	$0.1^{\pm0.1}$	$0.004^{\pm0.004}$
R	$0.1^{\pm0.1}$	$0.004^{\pm0.004}$
S	1.8 MAX	0.071 MAX.

54-pin plastic QFP (Straight lead type)



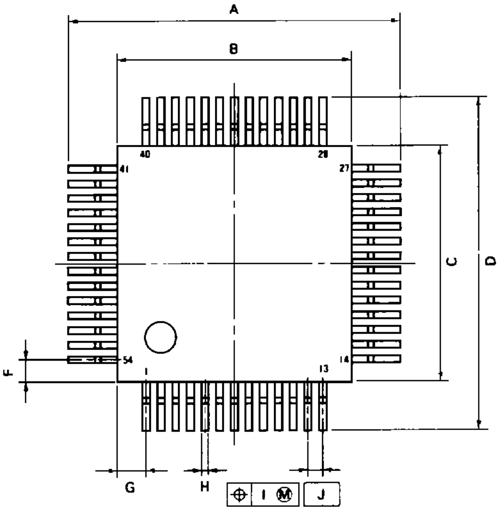
P54G-85-S

NOTE

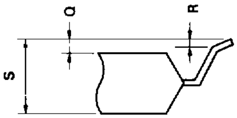
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition

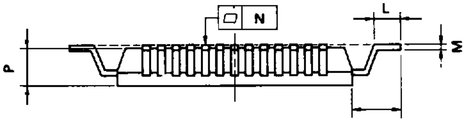
ITEM	MILLIMETERS	INCHES
A	$14.1^{\pm0.4}$	$0.555^{\pm0.016}$
B	$9.5^{\pm0.2}$	$0.374^{\pm0.008}$
C	$9.5^{\pm0.2}$	$0.374^{\pm0.008}$
D	$14.1^{\pm0.4}$	$0.555^{\pm0.016}$
F	0.5	0.020
G	0.85	0.033
H	$0.30^{\pm0.10}$	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	$2.3^{\pm0.2}$	$0.091^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
P	$1.5^{\pm0.1}$	$0.059^{\pm0.004}$
T	0.5	0.020
U	0.85	0.033

54-pin plastic QFP (Reverse bent type)



detail of lead end





P54G-65-R

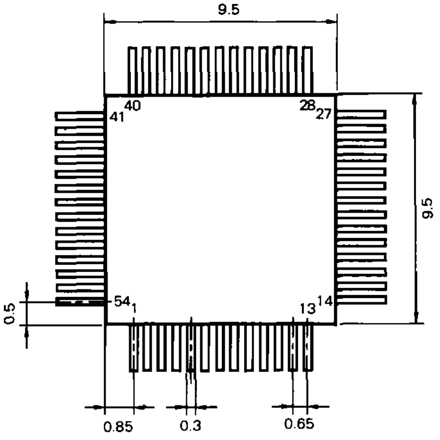
NOTE

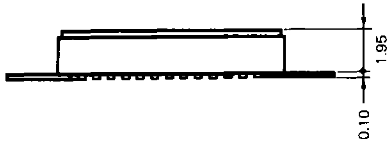
Each lead centerline is located within 0 15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

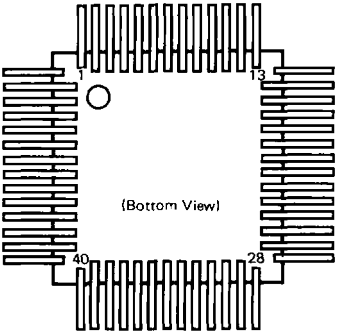
ITEM	MILLIMETERS	INCHES
A	13 9$^{\pm 0.4}$	0 547$^{\pm 0.016}$
B	9 5$^{\pm 0.2}$	0 374$^{\pm 0.008}$
C	9 5$^{\pm 0.2}$	0 374$^{\pm 0.008}$
D	13.9$^{\pm 0.4}$	0 547$^{\pm 0.016}$
F	0 5	0 020
G	0.85	0.033
H	0 30$^{\pm 0.10}$	0.012$^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T P)	0.026 (T.P.)
K	2.2$^{\pm 0.2}$	0.079$^{+0.009}_{-0.008}$
L	0.9$^{\pm 0.2}$	0 047$^{+0.008}_{-0.009}$
M	0.15$^{+0.10}_{-0.05}$	0.006$^{+0.004}_{-0.003}$
N	0.15	0.006
P	1.5$^{\pm 0.1}$	0.059$^{\pm 0.004}$
Q	0 1$^{\pm 0.1}$	0.004$^{\pm 0.004}$
R	0 1$^{\pm 0.1}$	0.004$^{\pm 0.004}$
S	1 8 MAX	0 071 MAX

PACKAGE DIMENSION FOR ENGINEERING SAMPLE (UNIT: mm)

54-pin Ceramic QFP







Note:

The length of lead is not fixed, because the tips of the leads are not managed cutting process