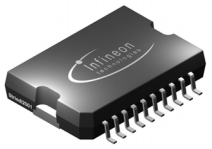
Smart Quad Channel Low-Side Switch

Features

- Shorted Circuit Protection
- Overtemperature Protection
- Overvoltage Protection
- Parallel Control of the Inputs (PWM Applications)
- Separate Diagnostic Pin for Each Channel
- Power - SO 20 - Package with integrated cooling area
- Standby mode with low current consumption
- µC compatible Input
- Electrostatic Discharge (ESD) Protection

Product Summary

Supply voltage	V_S	4.8 - 32	V
Drain source voltage	$V_{DS(AZ)max}$	60	V
On resistance	$R_{ON\ 1,2}$	0.2	Ω
	$R_{ON\ 3,4}$	0.35	Ω
Output current	$I_{D\ 1,2}$	2 x 5	A
	$I_{D\ 3,4}$	2 x 3	A



P-DSO-20-12

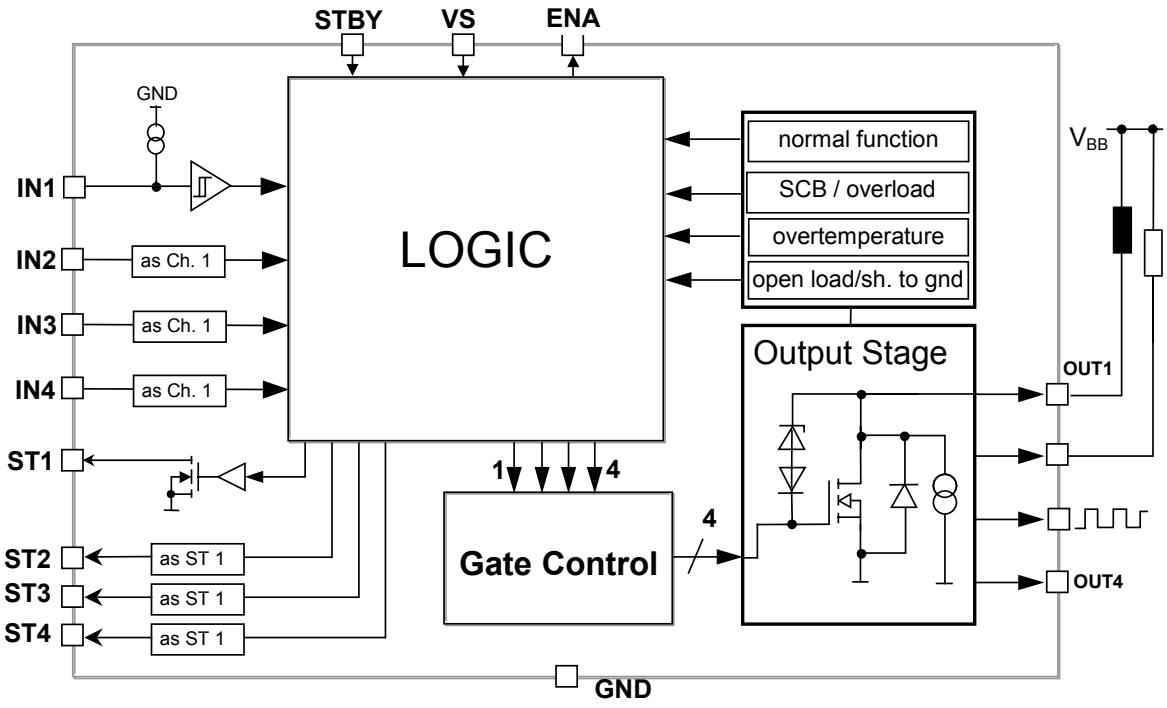
Application

- All kinds of resistive and inductive loads (relays, electromagnetic valves)
- µC compatible power switch for 12 and 24 V applications
- Solenoid control switch in automotive and industrial control systems
- Robotic Controls

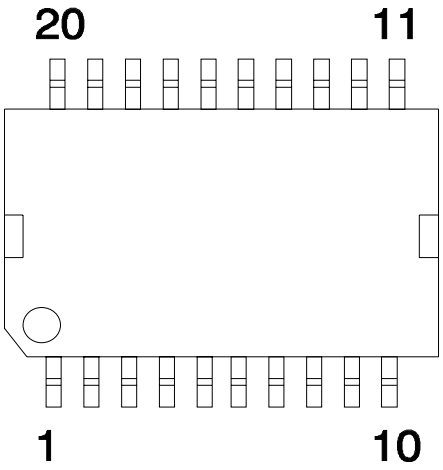
General description

Quad channel Low-Side-Switch (2x5A/2x3A) in Smart Power Technology (SPT) with four separate inputs and four open drain DMOS output stages. The TLE 6217 GP is fully protected by embedded protection functions and designed for automotive and industrial applications. Each channel has its own status signal for diagnostic feedback. Therefore the TLE 6217 GP is particularly suitable for ABS or Powertrain Systems.

Block Diagram



Pin Configuration (Top view)



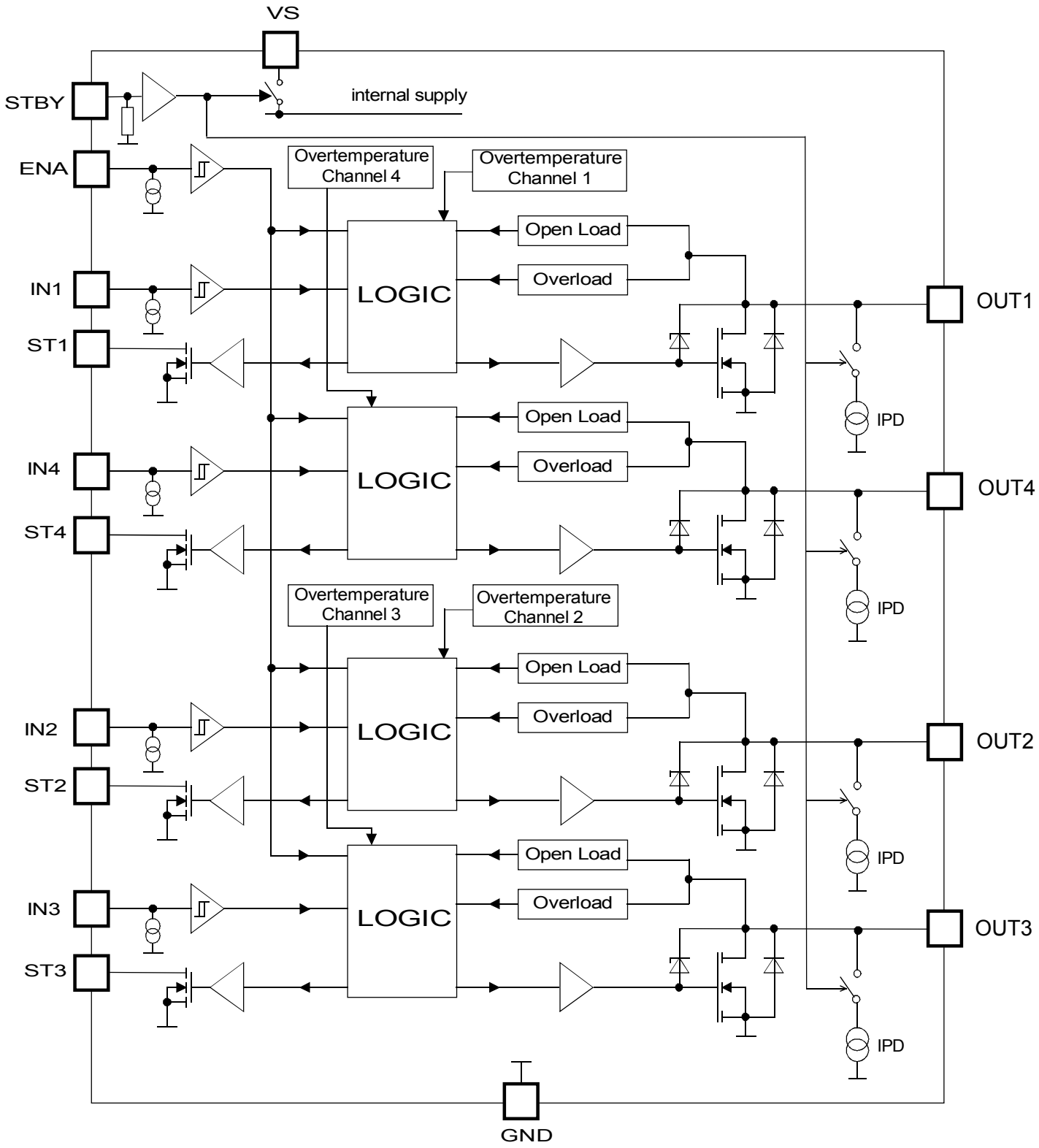
P - DSO - 20 - 12

Pin Description

Pin	Symbol	Function
1	GND	Ground
2	OUT1	Power Output channel 1
3	ST1	Status Output channel 1
4	IN4	Control Input channel 4
5	VS	Supply Voltage
6	STBY	Standby
7	IN3	Control Input channel 3
8	ST2	Status Output channel 2
9	OUT2	Power Output channel 2
10	GND	Ground
11	GND	Ground
12	OUT3	Power Output channel 3
13	ST3	Status Output channel 3
14	IN2	Control Input channel 2
15	GND	Ground Logic
16	ENA	Enable Input for all four channels
17	IN1	Control Input channel 1
18	ST4	Status Output channel 4
19	OUT4	Power Output channel 4
20	GND	Ground

Heat slug internally connected to ground pins

Detailed Block Diagram



Maximum Ratings for T_j = – 40°C to 150°C

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Parameter	Symbol	Values	Unit
Supply voltage	V_S	-0.3 ... + 40	V
Continuous drain source voltage (OUT1...OUT4)	V_{DS}	40	V
Input voltage IN1 to IN4, ENA	V_{IN} , V_{ENA}	- 1.5... + 6	V
Input voltage STBY	V_{STBY}	- 0.3 ... + 40	
Status output voltage	V_{ST}	- 0.3 ... + 32	V
Operating temperature range during clamping; Σt = 30 min during clamping; Σt = 15 min Storage temperature range	T_j T_j T_j T_{stg}	- 40 ... + 150 175 190 - 55 ... + 150	°C
Output current per channel	$I_{D(lim)}$	overload shutdown	A
Output current at reversal supply	$I_{D\ 1,2}$ $I_{D\ 3,4}$	- 4 - 2	A
Status output current	I_{ST}	- 5 ... + 5	mA
Inductive load switch off energy (single pulse) T_j = 25°C	E_{AS}	50	mJ
Electro**s**tatic **D**ischarge Voltage (HBM) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. Standard S5.1 – 1993 Output 1-4 Pins All other Pins	 V_{ESD} V_{ESD}	 4000 2000	V V V
Thermal resistance junction – case (die soldered on the frame)	R_{thJC}	2	K/W
Maximum operating lifetime (according to "Ambient thermal conditions")	t_b	10000	h

Ambient thermal conditions

$T_{Ambient}$ temperature range	operating periods
-40 °C	2 %
-20 °C	10 %
25 °C	24 %
60 °C	34 %
80 °C	24 %
100 °C	5 %
> 120 °C	1 %

Electrical Characteristics

Parameter and Conditions V_S = 4.8 to 18 V ; T_j = - 40 °C to + 150 °C (unless otherwise specified)		Symbol	Values			Unit
			min	typ	max	
1. Power Supply (V_S)						
Supply current (Outputs ON)		I_S			8	mA
Supply current (Outputs OFF) V_{ENA} = L, V_{STBY} = H		I_S			4	mA
Standby current	V_{STBY} = L	I_S			10	µA
Operating voltage		V_S	4.8		32	V
2. Power Outputs						
ON state resistance Channel 1,2 I_D = 1A; $V_S \geq$ 9.5 V	T_j = 25 ° C T_j = 150°C	$R_{DS(ON)}$		0.2	 0.5	Ω
ON state resistance Channel 3,4 I_D = 1A; $V_S \geq$ 9.5 V	T_j = 25 ° C T_j = 150°C	$R_{DS(ON)}$		0.35	 0.75	Ω
Z-Diode clamping voltage (OUT1...4)	$I_D \geq$ 100 mA	$V_{DS(AZ)}$	45		60	V
Pull down current	V_{STBY} = H, V_{IN} = L	I_{PD}	10	20	50	µA
Output Leakage Current	VSTBY = L Tj = -40°C...150°C wafer test at 25°C	I_{Dlk}			 5 1	 µA µA
Output turn on delay time [1]	I_D = 1 A	t_{on}	0	5	20	µs
Output turn off delay time [1]	I_D = 1 A	t_{off}	0	10	30	
Output on fall time [1]	I_D = 1 A	t_{fall}	3	10	30	
Output off rise time [1]	I_D = 1 A	t_{rise}	3	10	30	
Overload switch-off delay time [1]		t_{DSO}	20		100	
Output off status delay time [2]		t_D	500	1200	3000	
Failure extension Time for Status Report		$t_{D\text{-}failure}$	500	1200	3000	
Input Suppression Time		$t_{D\text{-}IN}$	500	1200	3000	
Open Load (off) filtering Time [2]		$t_{fOL(off)}$	10	30	100	
3. Digital Inputs (IN1, IN2, IN3, IN4, ENA)						
Input low voltage		V_{INL}	- 0.3		1.0	V
Input high voltage		V_{INH}	2.0		6.0	V
Input voltage hysteresis [2]		V_{INHys}	50	100		mV
Input pull down current	V_{IN} = 5 V; $V_S \geq$ 6.5 V	I_{IN}	10	30	60	µA
Enable pull down current	V_{ENA} = 5 V; $V_S \geq$ 6.5 V	I_{ENA}	10	20	40	µA
4. Digital Status Outputs (ST1 - ST4) Open Drain						
Output voltage low	I_{ST} = 2 mA	V_{STL}			0.5	V
Leakage current high		I_{STH}			2	µA

[1] See timing diagram, resistive load condition; $V_S \geq$ 9 V
[2] This parameter will not be tested but assured by design

Electrical Characteristics

Parameter and Conditions V_S = 4.8 to 18 V ; T_j = – 40 °C to + 150 °C (unless otherwise specified)		Symbol	Values			Unit
			min	typ	max	
5. Standby Input (STBY)						
Input low voltage		V_{STBY}	0		1	V
Input high voltage		V_{STBY}	3.5		V_S	V
Input current	V_{STBY} = 18 V	I_{STBY}			300	µA
6. Diagnostic Functions						
Open load detection voltage V_{ENA} = X, V_{IN} = L	$V_S \geq$ 6.5 V	$V_{DS(OL)}$	0.3*V_S	0.33*V_S	0.36*V_S	V
Open load detection current channel 1,2 V_{ENA} = V_{IN} = H	$V_S \geq$ 6.5 V	$I_{D(OL)\ 1,2}$	100		240	mA
Open load detection current channel 3,4 V_{ENA} = V_{IN} = H	$V_S \geq$ 6.5 V	$I_{D(OL)\ 3,4}$	100		240	mA
Overload Current channel 1, 2	Vs ≥ 6.5 V	$I_{D(lim)\ 1,2}$	5	7.5		A
Overload Current channel 3 , 4	Vs ≥ 6.5 V	$I_{D(lim)\ 3,4}$	3	5		A
Overtemperature shutdown threshold [2] Hysteresis		T_{th} T_{hys}	170	 10	200	°C K
Pulse Width for static diagnostic output		t_{IN}			500	µs

[2] This parameter will not be tested but assured by design

Application Description

This IC is especially designed to drive inductive loads (relays, electromagnetic valves).
Integrated clamp-diodes limit the output voltage when inductive loads are discharged.

Four open-drain logic outputs indicate the status of the integrated circuit. The following conditions are monitored and signalled:

- Overloading of output (also shorted load to supply) in active mode
- Open and shorted load to ground in active and inactive mode
- Overtemperature

Circuit Description

Input Circuits

The control and enable inputs, both active high, consist of schmitt triggers with hysteresis. All inputs are provided with pull-down current sources. Not connected inputs are interpreted as low and the respective output stages are switched off.

In standby mode (STBY = LOW) the current consumption is greatly reduced.
The circuit is active when STBY = HIGH.
If the standby function is not used, it is allowed to connect the standby pin directly to VS.
Status Signals: The status signals are undefined for 2ms after a power up event or a STBY low to high transition.

Output Stages

The four power outputs consist of DMOS-power transistors with open drains. The output stages are short circuit protected throughout the operating range. Each output has it's own zenerclamp. This causes a voltage limitation at the power transistor when inductive loads are switched off.
Parallel to the DMOS transistors there are internal pull down current sources. They are provided to detect an open load condition in the off state. They will be disconnected in the standby mode.
Due to EMI measures there is an internal zenerclamp in parallel to the output stage. It gets active above 33V drain source voltage. This leads to an increasing leakage current up to 1 mA @ V_{DS} = 40V.

Protective Circuits

The outputs are protected against current overload and overtemperature. If the output current increases above the overload detection threshold I_{QO} for a longer time then t_{DSO} or the temperature increases above T_{th}, then the power transistor is immediately switched off. It remains off until the control signal at the input is switched off and on again.

Fault Detection

The status outputs indicate the switching state of the output stage. Under normal conditions is: ST = low Output off; ST = high Output on. If an error occurs, the logic level of the status output is inverted, as listed in the diagnostic table.

If current overload or overtemperature occurs for a longer time than t_{DSO}, the fault condition is latched into an internal register and the output is shutdown. The reset is done by switching off the corresponding control input for a time longer than $t_{D\text{-}IN}$.

Open load is detected for all four channels in on and off mode.

In the on mode the load current is monitored. If it drops below the specified threshold value IQU then an open load condition is detected.

In the off mode, the output voltage is monitored. An open load condition is detected when the output voltage of a given channel is below the threshold $V_{DS(OL)}$, which is typ. 33 % of the supply voltage VS. To prevent an open load diagnosis in case of transient Voltages on the outputs the open load detection in off mode uses a filter of typ. 30µs.

Status output at pulse width operation

If the input is operated with a pulsed signal, the status does not follow each single pulse of the input signal. An internal delay t_D of typ. 1.2ms (min 500 µs) enables a continuous status output signal. See the timing diagrams on the following pages for further information.

This internal status delay simplifies diagnostic software for pwm applications.

Diagnostic Table

In general the status follows the input signal in normal operating conditions.

If any error is detected the status is inverted.

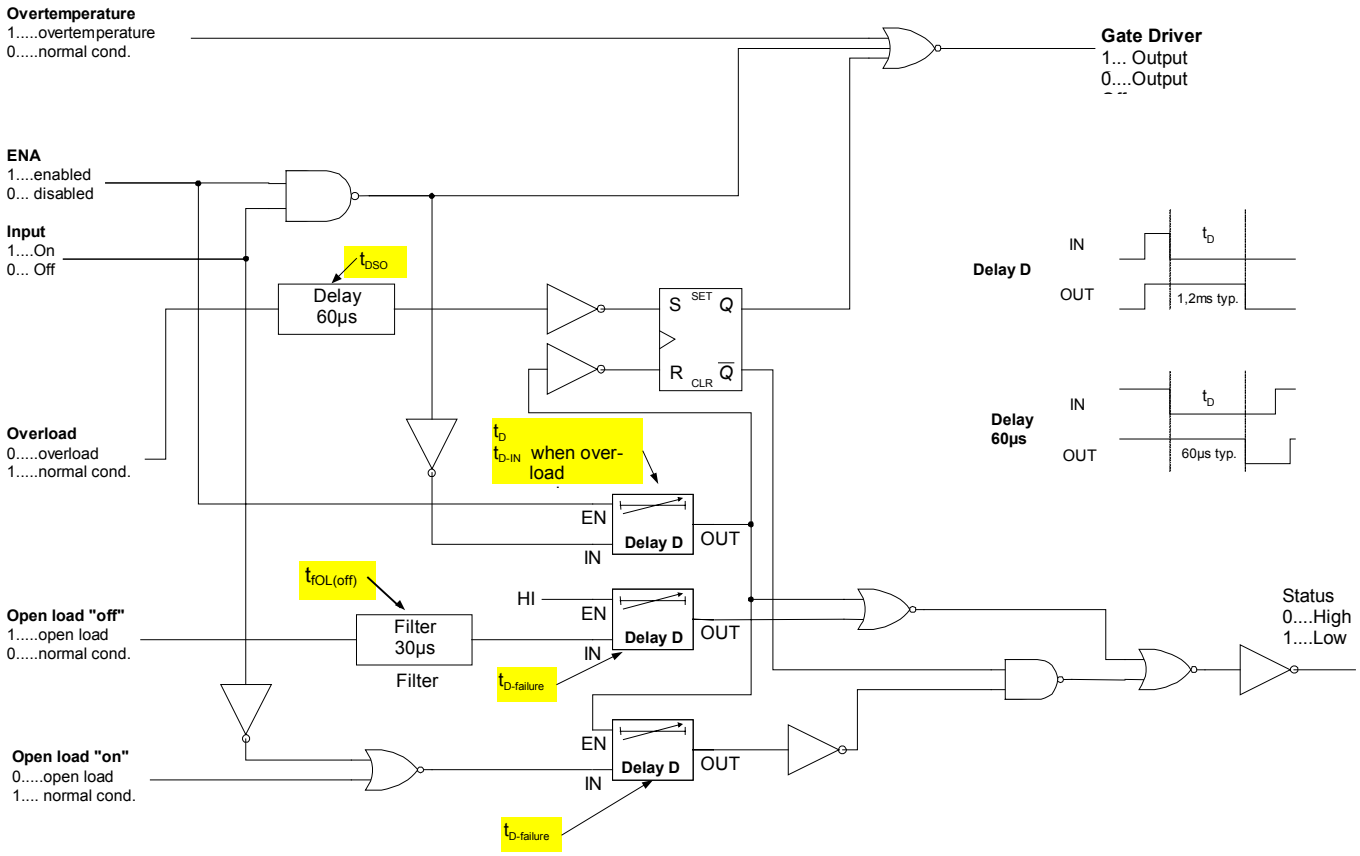
Operating Condition	Standby Input	Enable Input	Control Input	Power Output	Status Output
	STBY	**ENA**	**IN**	**Q**	**ST**
Standby	L	X	X	off	H
Normal function	H H H	L H H	X L H	off off ON	L L H
Open load or short to ground	H H H H	L L H H	L H L H	off off off ON	H H H L
Overload or short to supply[1)] reset latch [2)]	H H H	H H L	H H → L X	off off off	L L L
Overtemperature[1)] reset latch [2)]	H H H	H H L	H H → L X	off off off	L L L

Note 1) : overload/short-to-supply/overtemperature - events shorter than min. time t_{DSO} specified in 2.10 will not be latched and not reported at the status pin.

Note 2): to reset latched status-output in case of overload/short-to-supply/overtemperature the control input has to go low and stay low for longer than max. Input suppression time $t_{D\text{-}IN}$ specified in 2.13 of the characteristics

Failure Situations and Status Report

Logic Block Diagram



Timing Diagrams

Output Slope

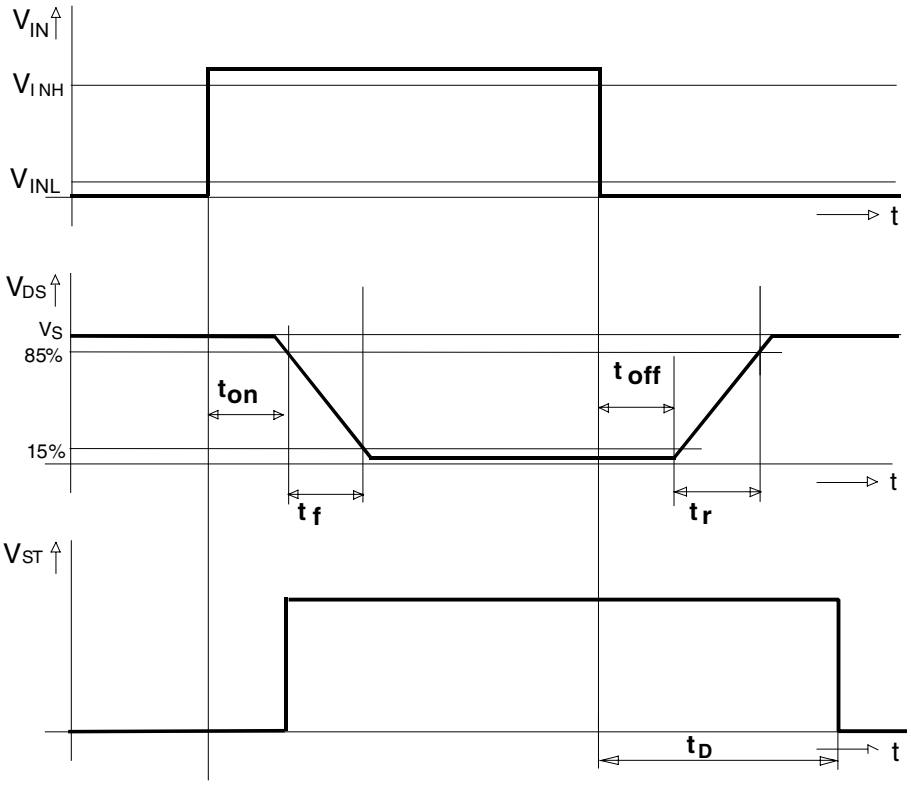


FIG. 1

Overload Switch OFF Delay

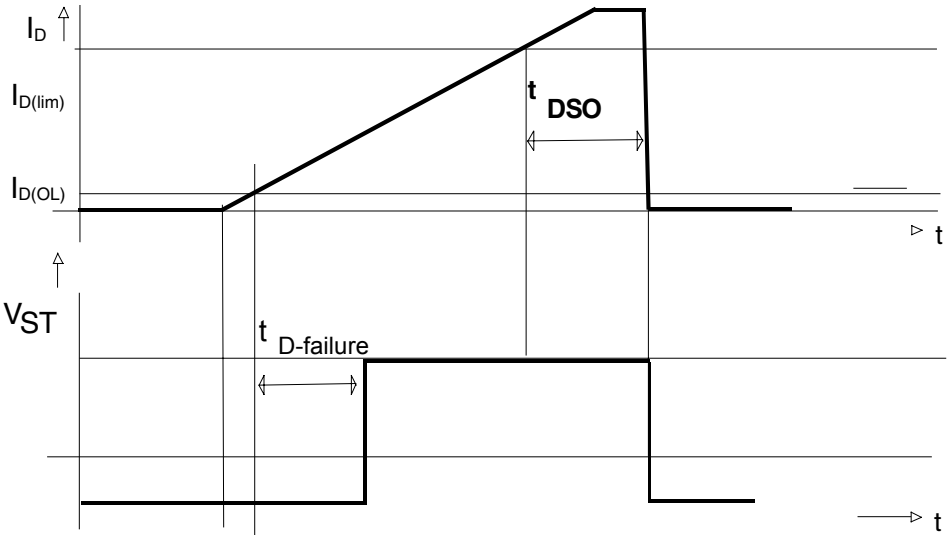
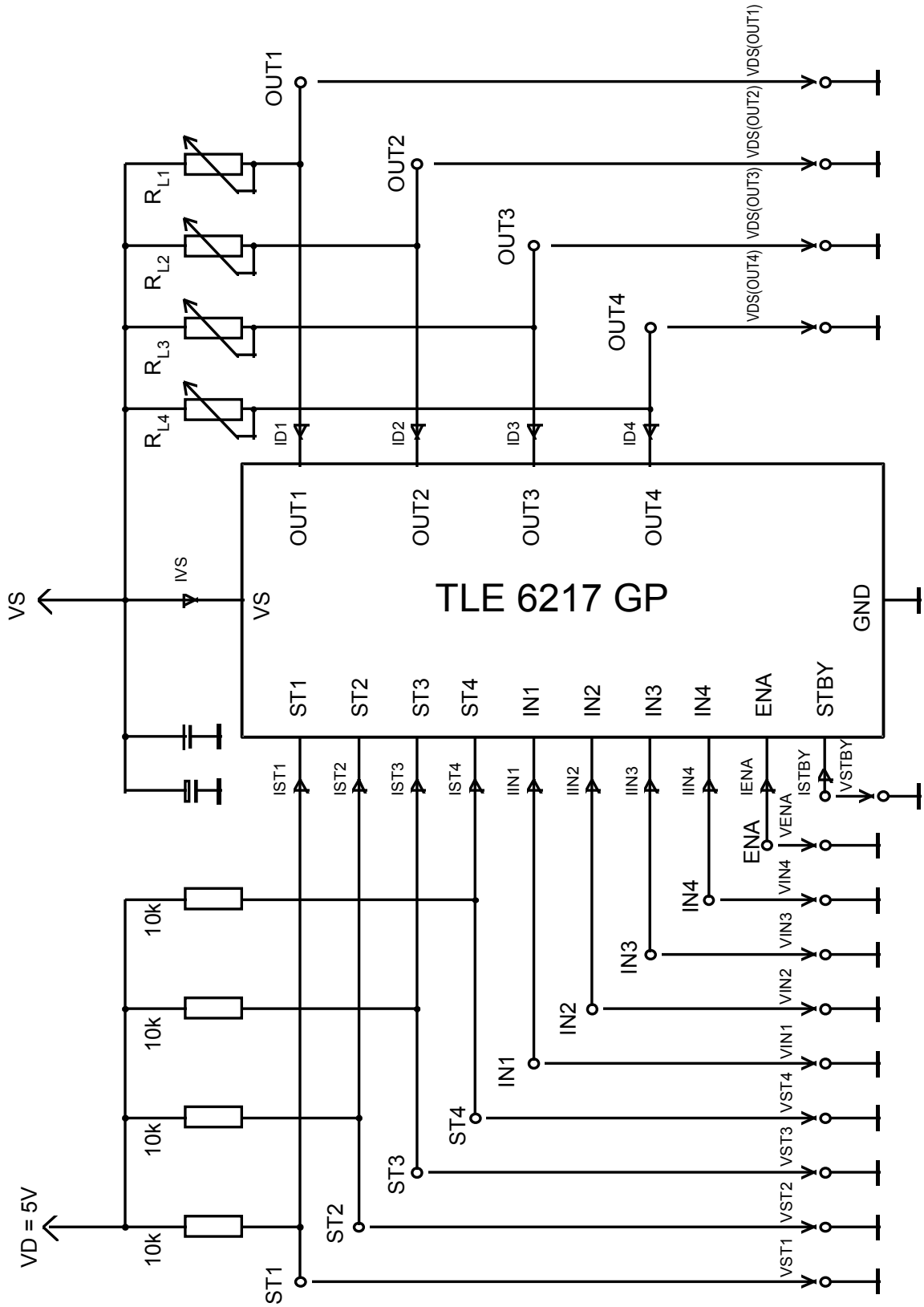
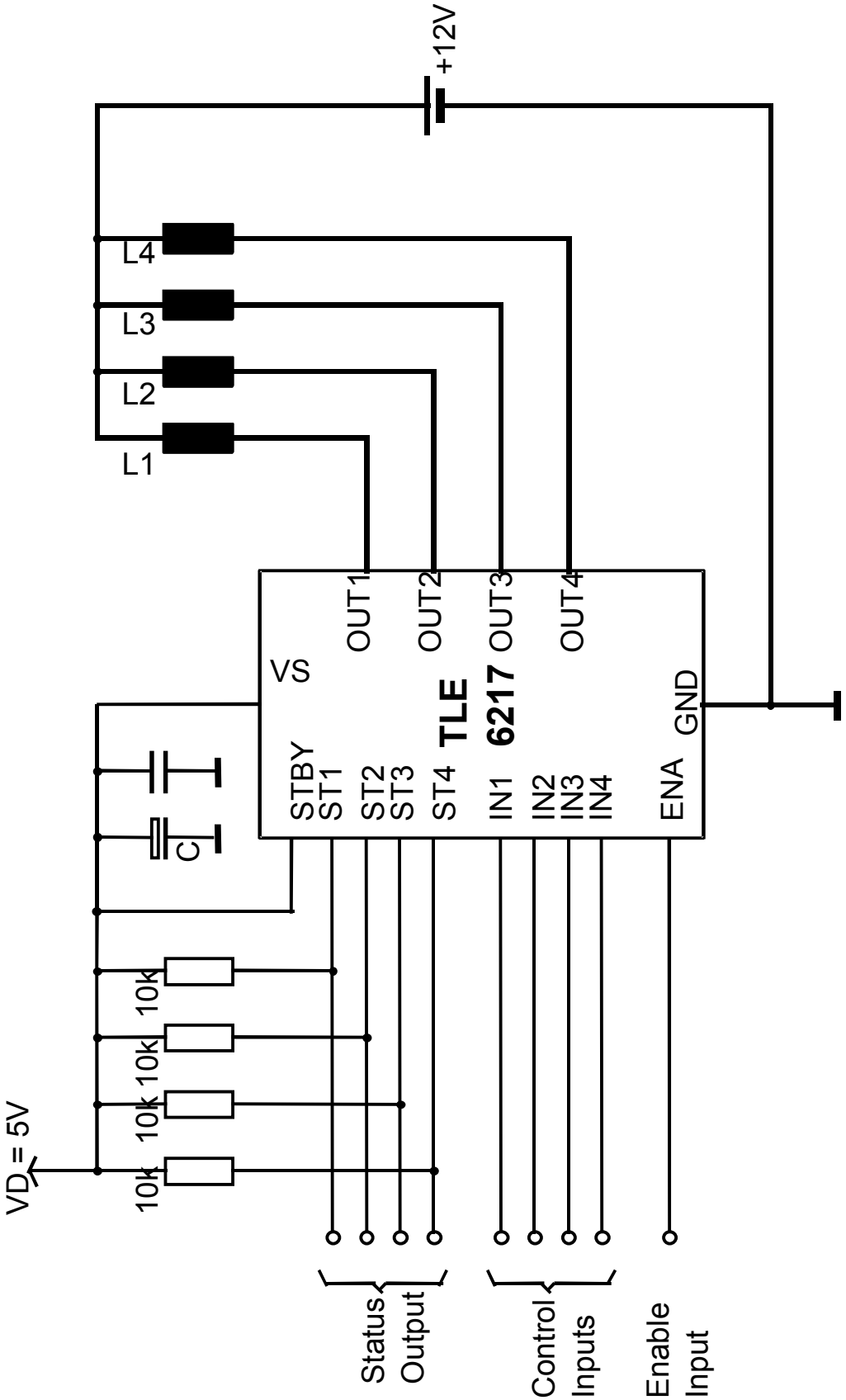


FIG. 2

Test Circuit



Application Circuit



The blocking capacitor C is recommended to avoid critical negative voltage spikes on VS in case of battery interruption during OFF-commutation.

Timing Diagrams of Diagnostic with Pulsed Input Signal

Normal condition, resistive load, pulsed input signal

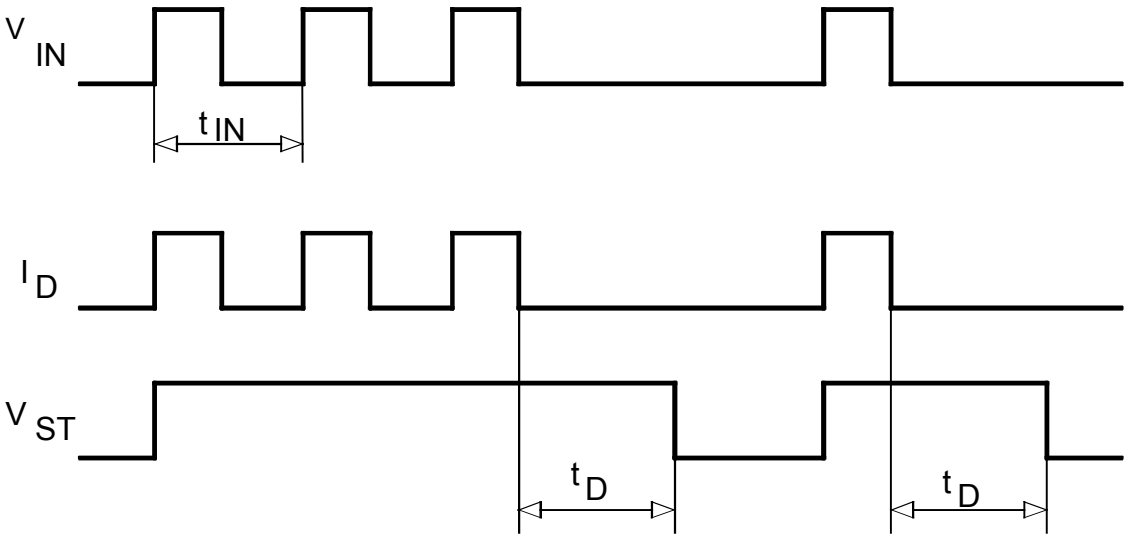
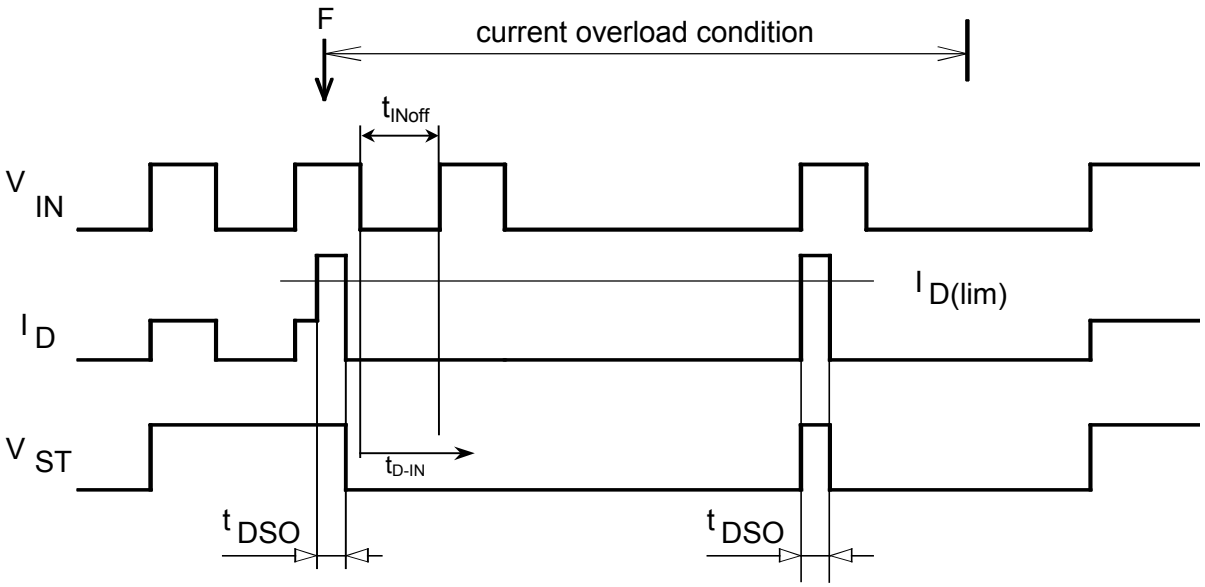


Fig. 3

Current Overload



t_{INoff} < t_{D-IN} : Input suppression time avoids a restart after overtemperature

Fig. 4

Diagnostic status output at different open load current conditions

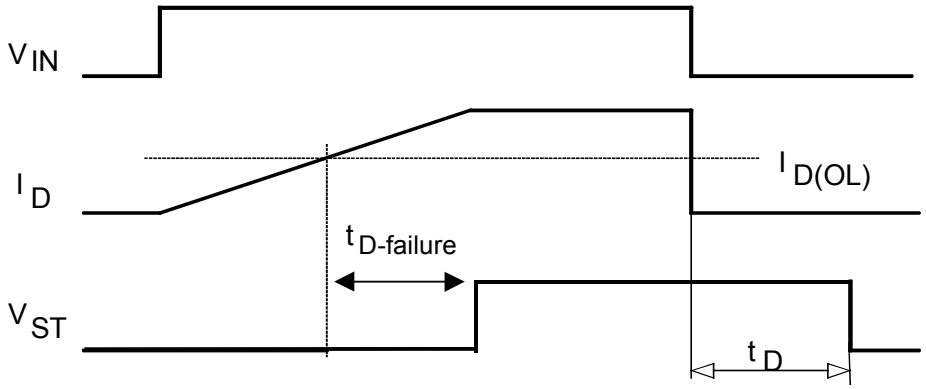
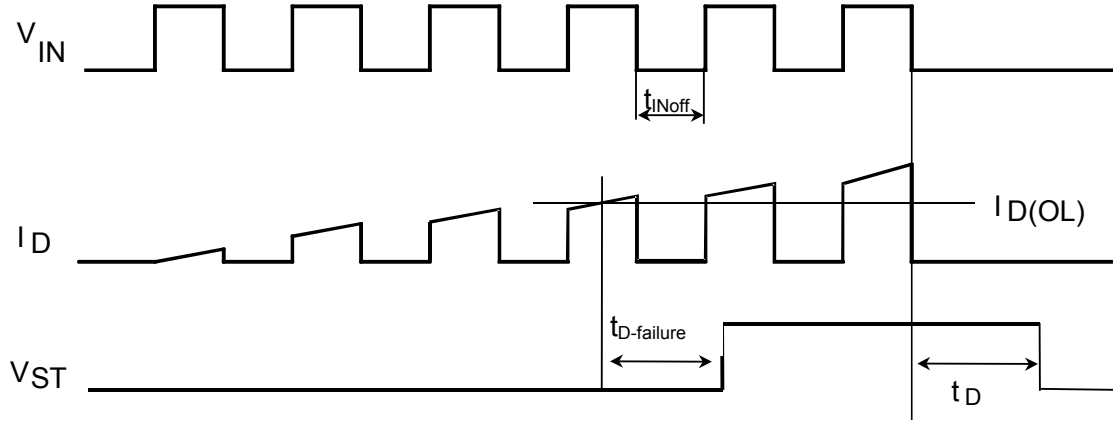
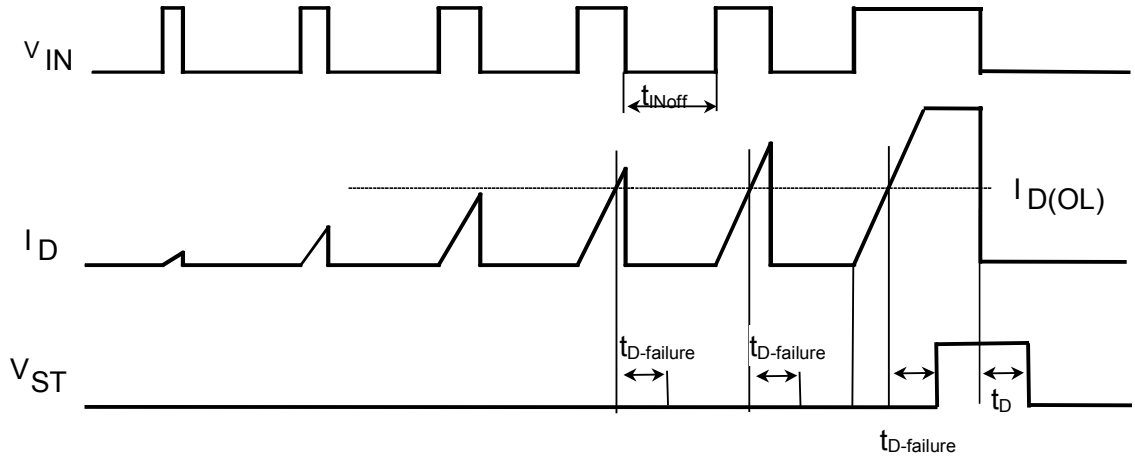


Fig. 5



$t_{INOFF} < t_D$ leads to a static status signal

Fig. 6



$t_{INoff} > t_D$: Intermittend status signal

Fig. 7

Normal operation, followed by open load condition

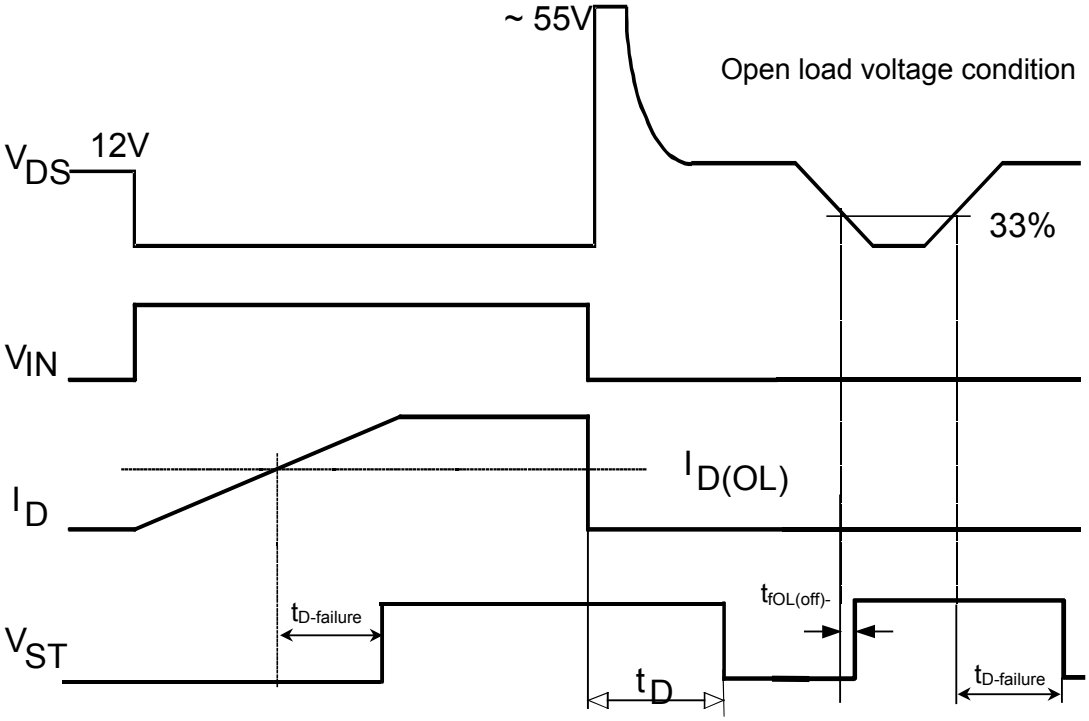


Fig. 8

Overtemperature

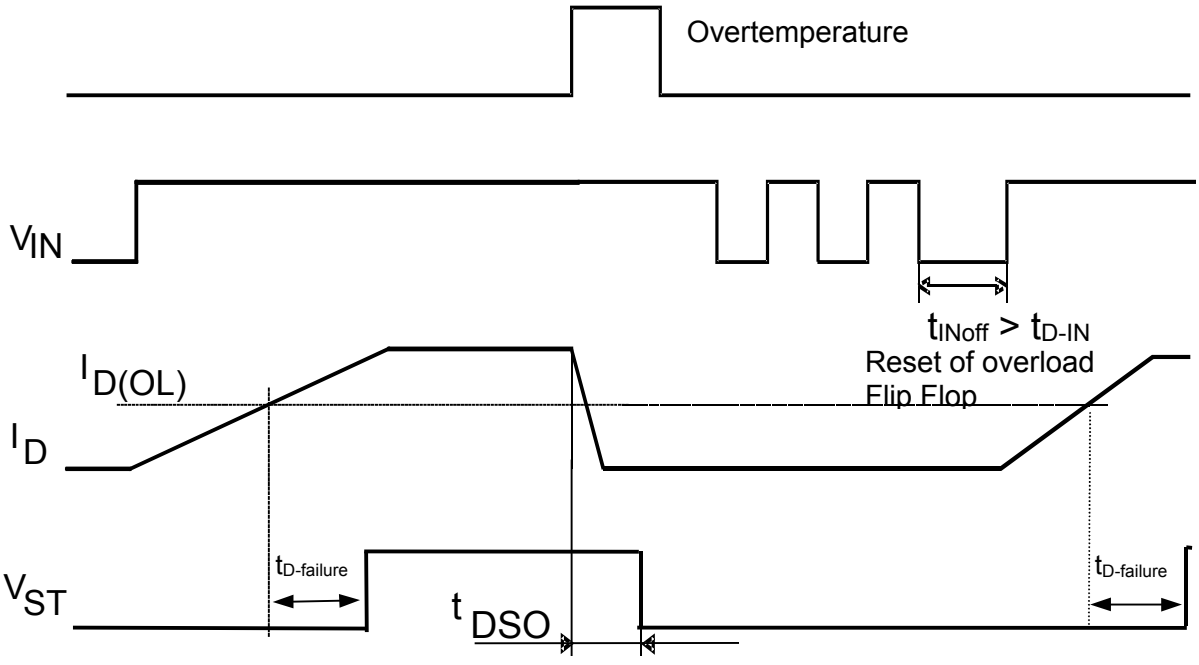
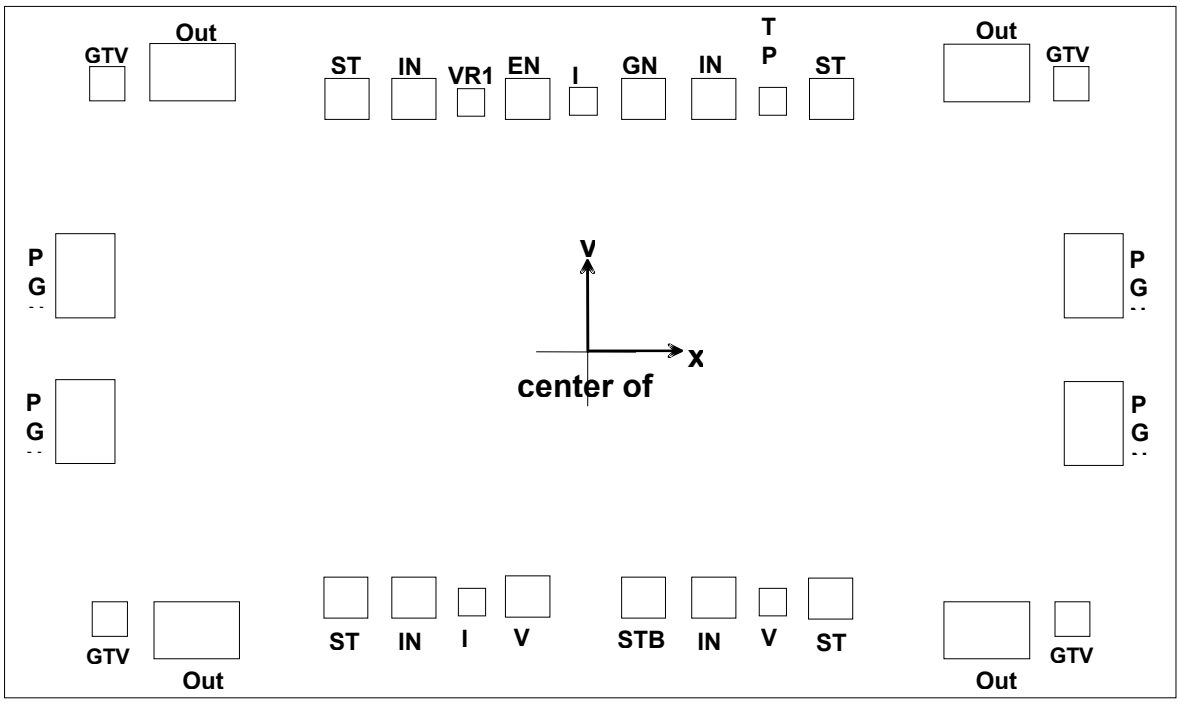


Fig. 9

Ordering code

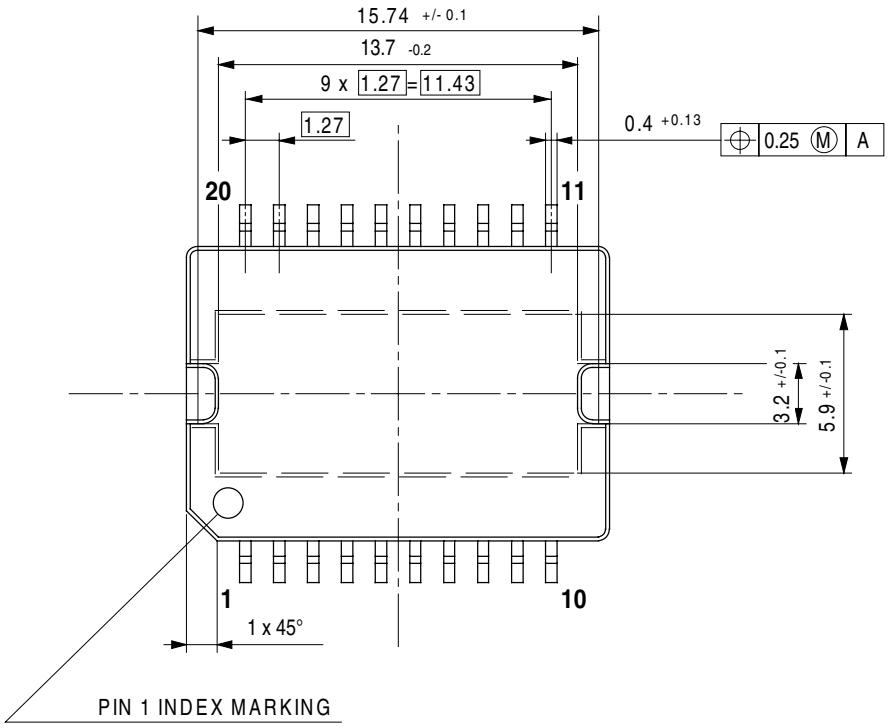
Type	Ordering Code	Package
TLE6217 G	on request	P - DSO - 20 – 12
TLE6217 C	on request	Bare dice on wafer

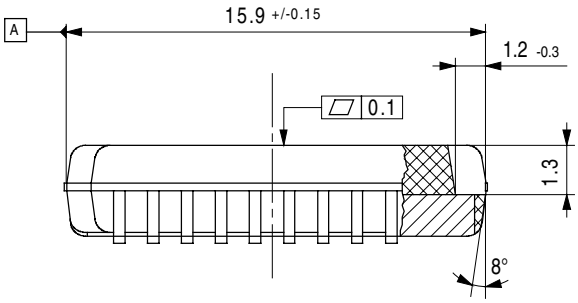
Pad Assignment

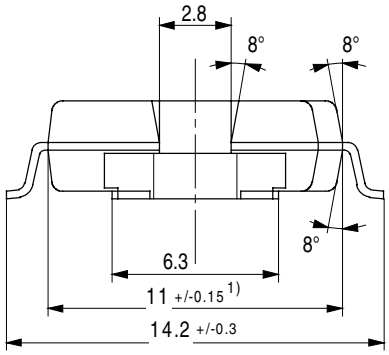


Package dimensions

All dimensions in mm







Revision List:

01.09.2001	Target Datasheet	V1
01.10.2001	First revision	V2
01.12.2001	Second revision	V3
30.04.2002	Third revision	V4
30.07.2002	Preliminary Datasheet	V5
09.09.2002	Final Datasheet	V6

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