STP7N65M2, STU7N65M2

N-channel 650 V, 0.98 Ω typ., 5 A MDmesh™ M2 Power MOSFETs in TO-220 and IPAK packages

Datasheet - preliminary data

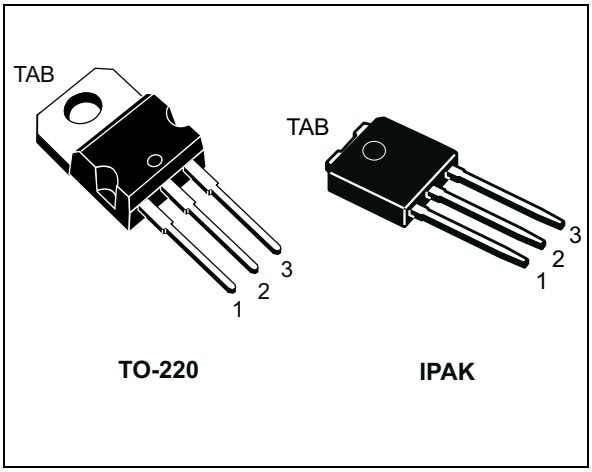
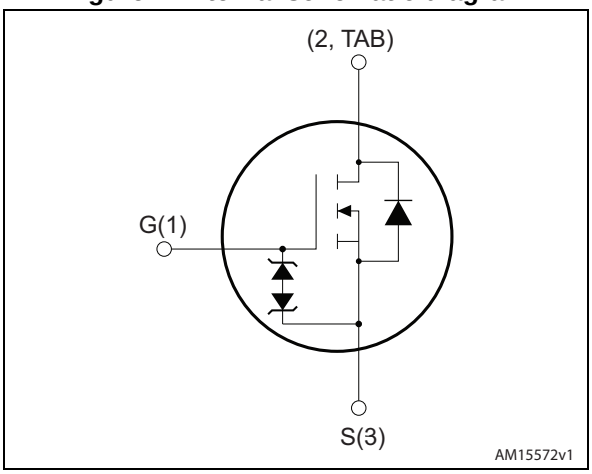


Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STP7N65M2	650 V	1.15 Ω	5 A
STU7N65M2	650 V	1.15 Ω	5 A

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFET developed using the MDmesh™ M2 technology. Thanks to the strip layout associated to an improved vertical structure, the device exhibits both low on-resistance and optimized switching characteristics. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Package	Packaging
STP7N65M2	7N65M2	TO-220	Tube
STU7N65M2	7N65M2	IPAK	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	5	A
I_D	Drain current (continuous) at T_C = 100 °C	3.2	A
I_{DM}(1)	Drain current (pulsed)	20	A
P_{TOT}	Total dissipation at T_C = 25 °C	60	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 5$ A, di/dt ≤ 400 A/µs; $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD}=400 V
3. $V_{DS} \leq 520$ V

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	IPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2.08		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	100	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1	A
E_{AS}	Single pulse avalanche energy (starting T_j=25°C, I_D= I_{AR}; V_{DD}=50V)	103	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 650 V			1	µA
		V_{GS} = 0, V_{DS} = 650 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.5 A		0.98	1.15	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	270	-	pF
C_{oss}	Output capacitance		-	14.5	-	pF
C_{rss}	Reverse transfer capacitance		-	0.8	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0	-	108	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 5 A, V_{GS} = 10 V (see *Figure 17*)	-	9	-	nC
Q_{gs}	Gate-source charge		-	2.3	-	nC
Q_{gd}	Gate-drain charge		-	4.3	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 2.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 16* and *21*)	-	8	-	ns
t_r	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	30	-	ns
t_f	Fall time		-	20	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		20	A
V_{SD} (2)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 21*)	-	275		ns
Q_{rr}	Reverse recovery charge		-	1.62		µC
I_{RRM}	Reverse recovery current		-	11.8		A
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 21*)	-	430		ns
Q_{rr}	Reverse recovery charge		-	2.54		µC
I_{RRM}	Reverse recovery current		-	11.9		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

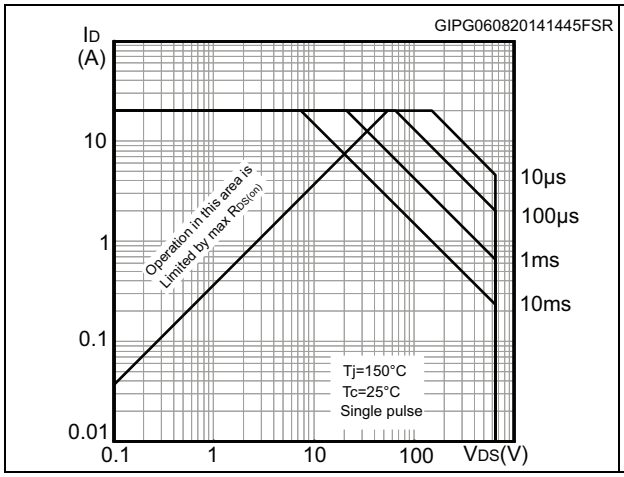


Figure 3. Thermal impedance for TO-220

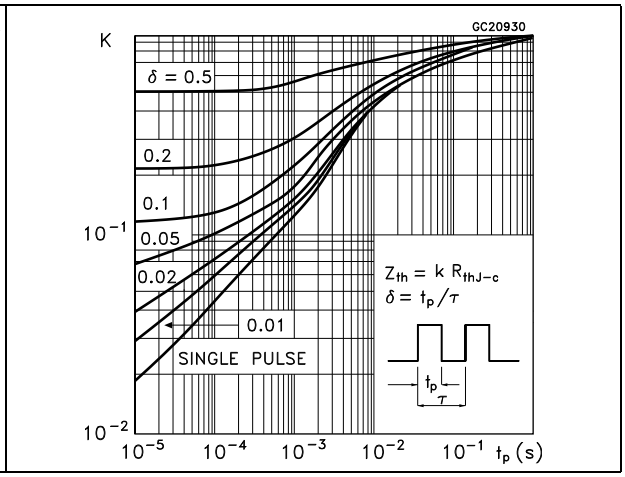


Figure 4. Safe operating area for IPAK

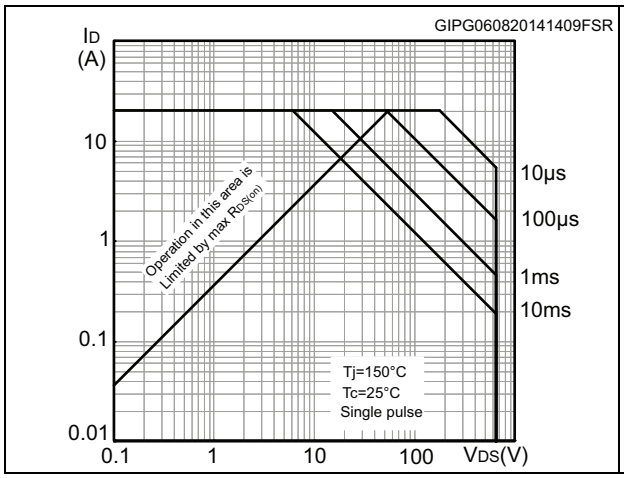


Figure 5. Thermal impedance for IPAK

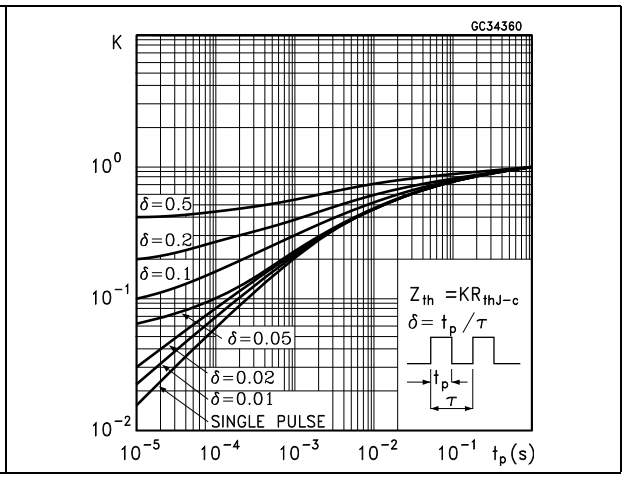


Figure 6. Output characteristics

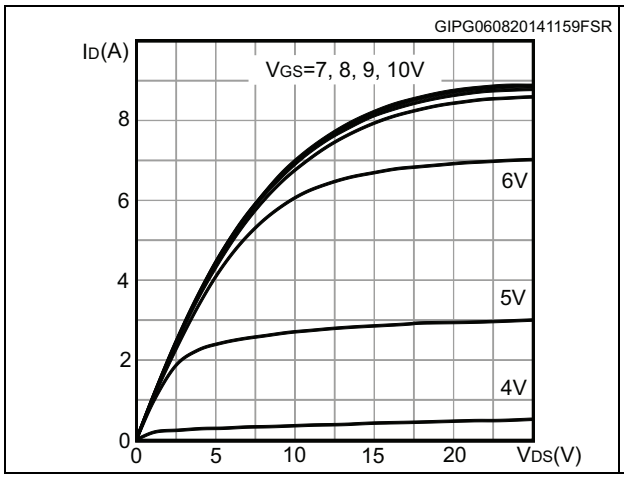


Figure 7. Transfer characteristics

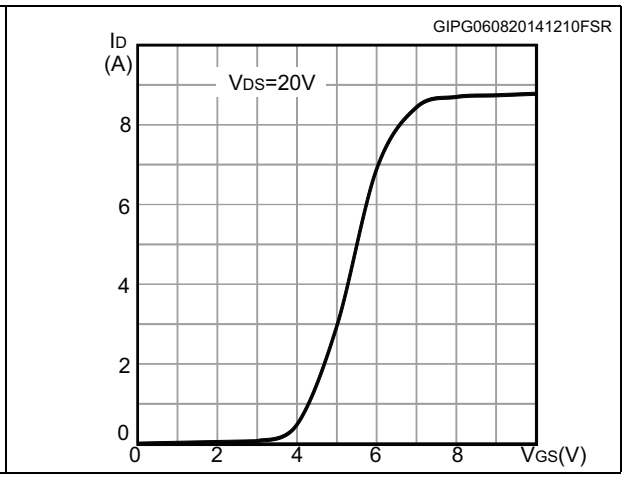


Figure 8. Gate charge vs gate-source voltage

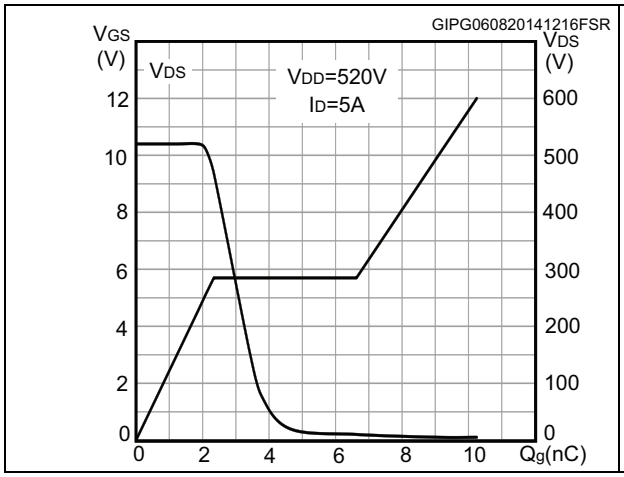


Figure 9. Static drain-source on-resistance

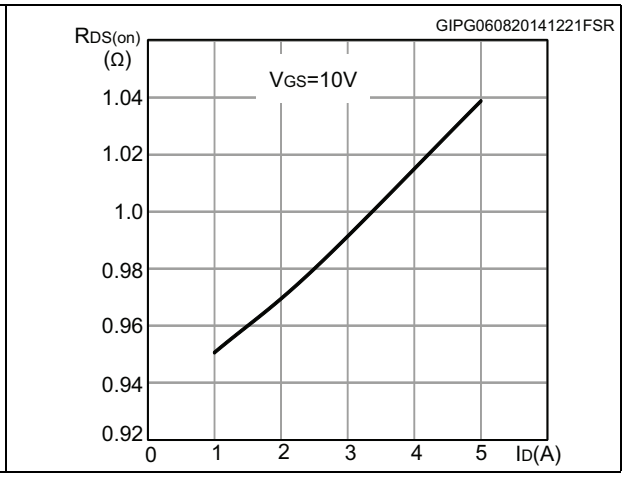


Figure 10. Capacitance variations

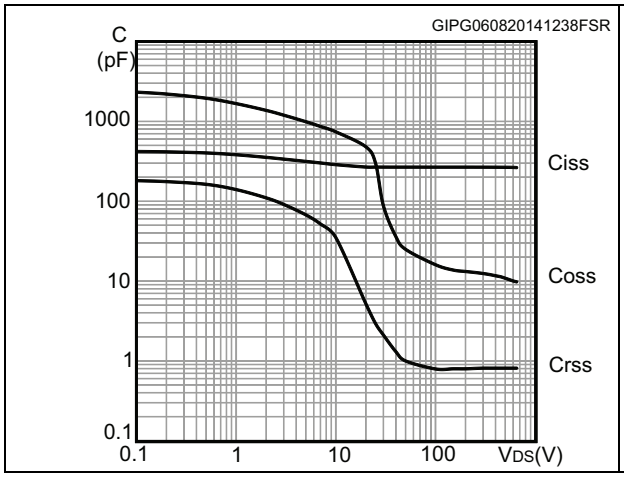


Figure 11. Output capacitance stored energy

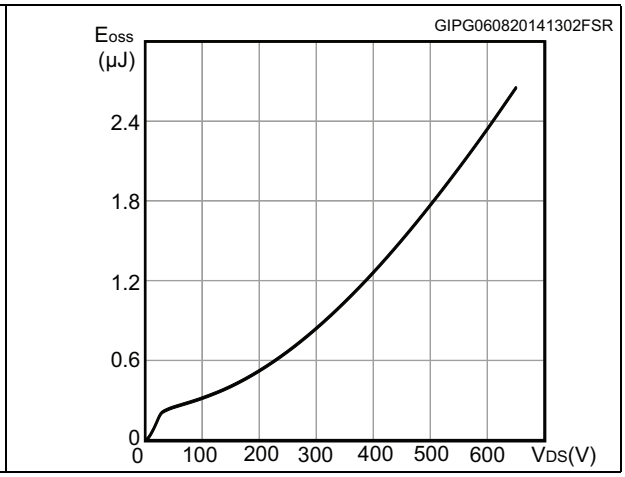


Figure 12. Normalized gate threshold voltage vs temperature

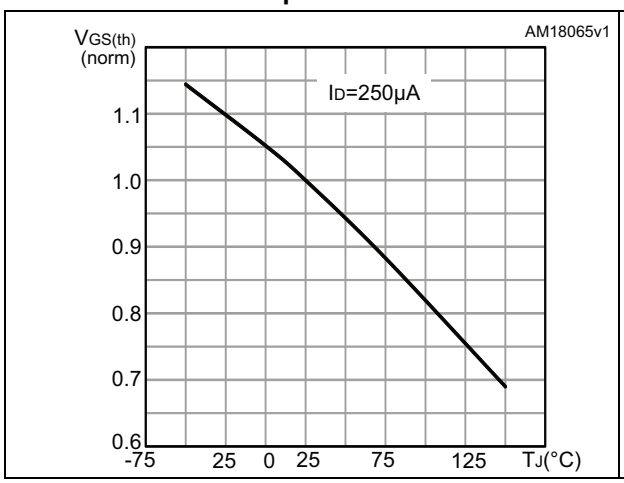


Figure 13. Normalized on-resistance vs temperature

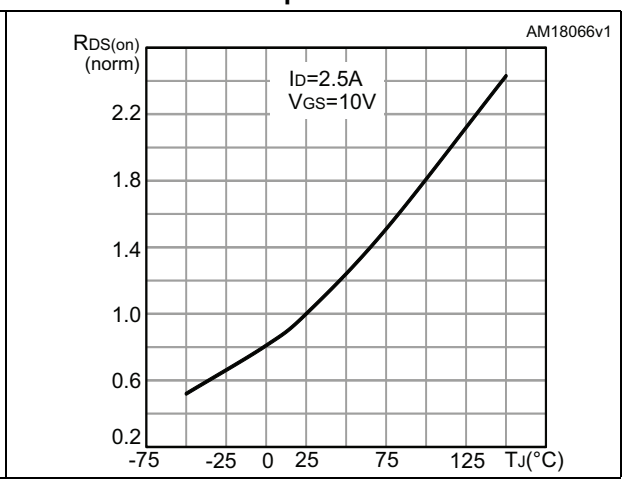


Figure 14. Source-drain diode forward characteristics

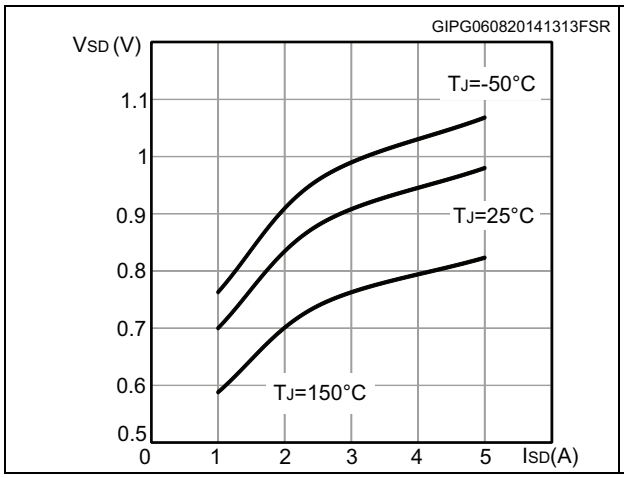
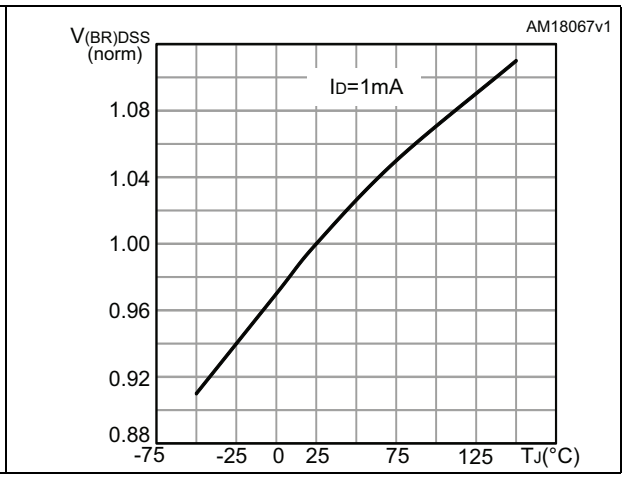


Figure 15. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 16. Switching times test circuit for resistive load

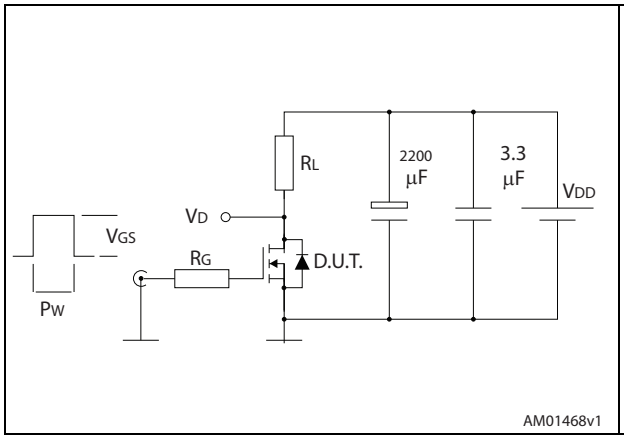


Figure 17. Gate charge test circuit

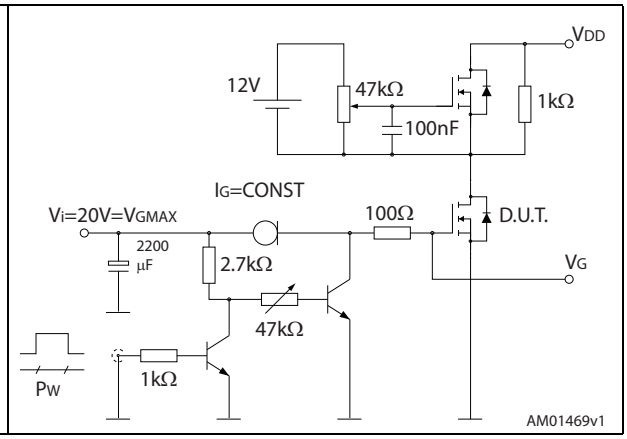


Figure 18. Test circuit for inductive load switching and diode recovery times

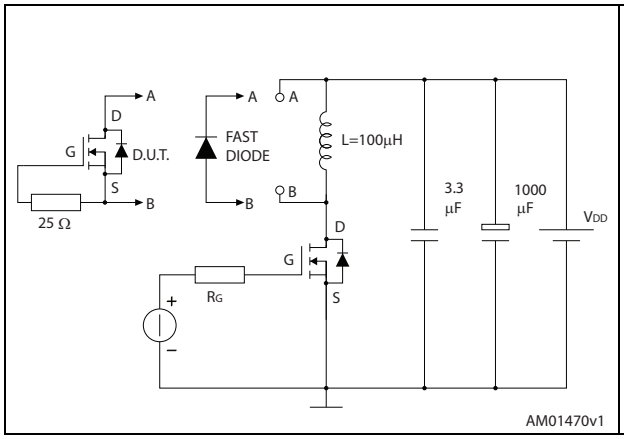


Figure 19. Unclamped inductive load test circuit

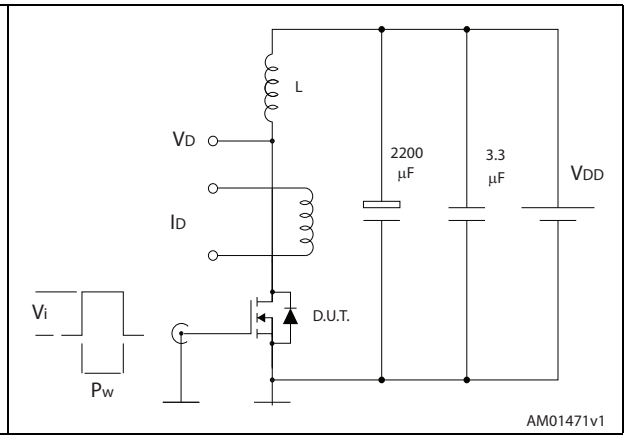


Figure 20. Unclamped inductive waveform

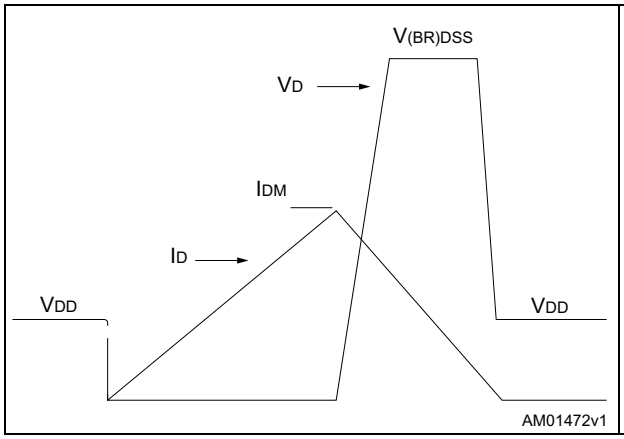
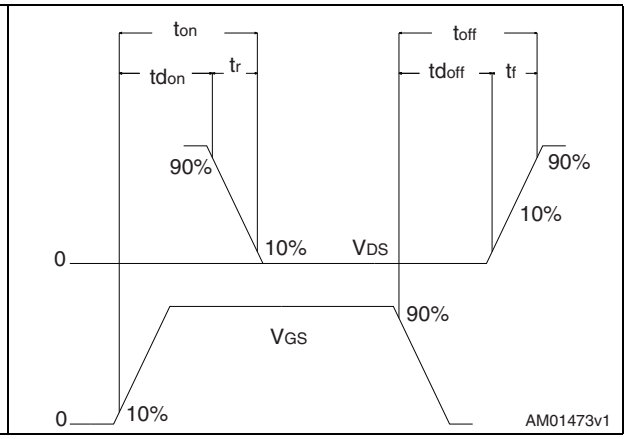


Figure 21. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 TO-220, STP7N65M2

Figure 22. TO-220 type A drawing

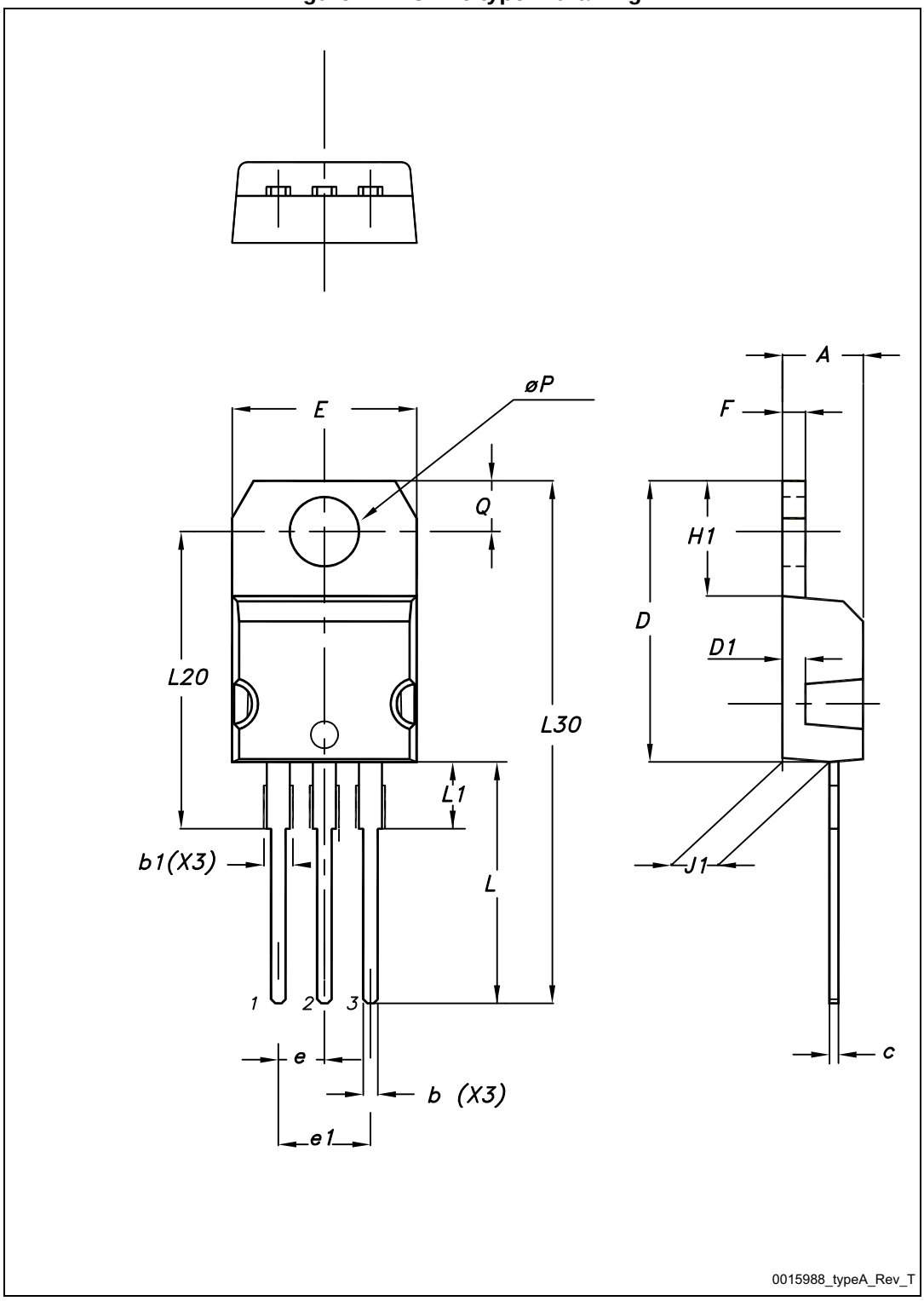


Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.2 IPAK, STU7N65M2

Figure 23. IPAK (TO-251)type A drawing

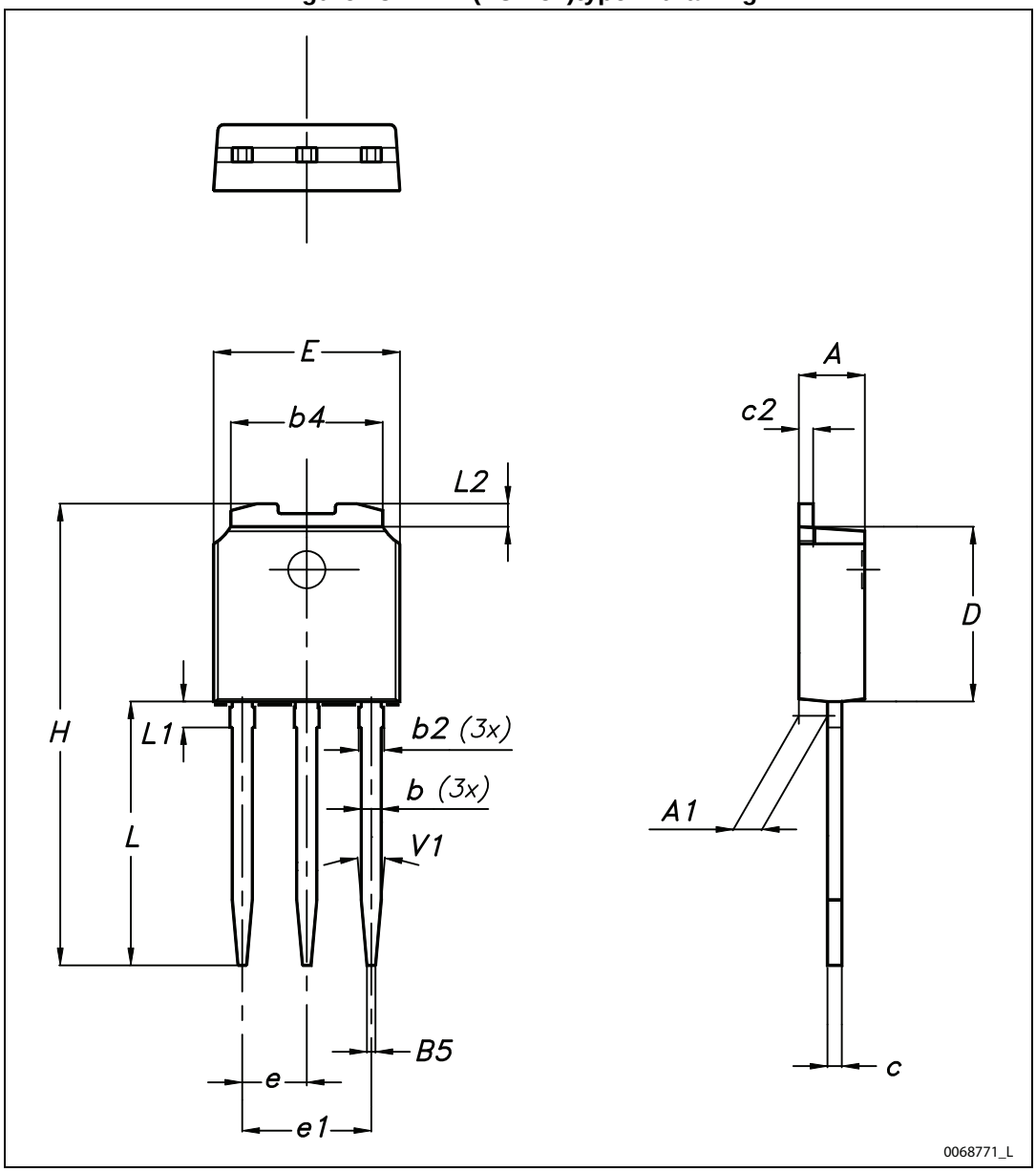


Table 10. IPAK (TO-251) type A mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.43
B5		0.30	
c	0.45		0.60
c2	0.46		0.60
D	6.00		6.20
E	6.40		6.70
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.60
L1	0.80		1.20
L2		0.80	1.25
V1		10°	

Figure 24. IPAK (TO-251) type C drawing

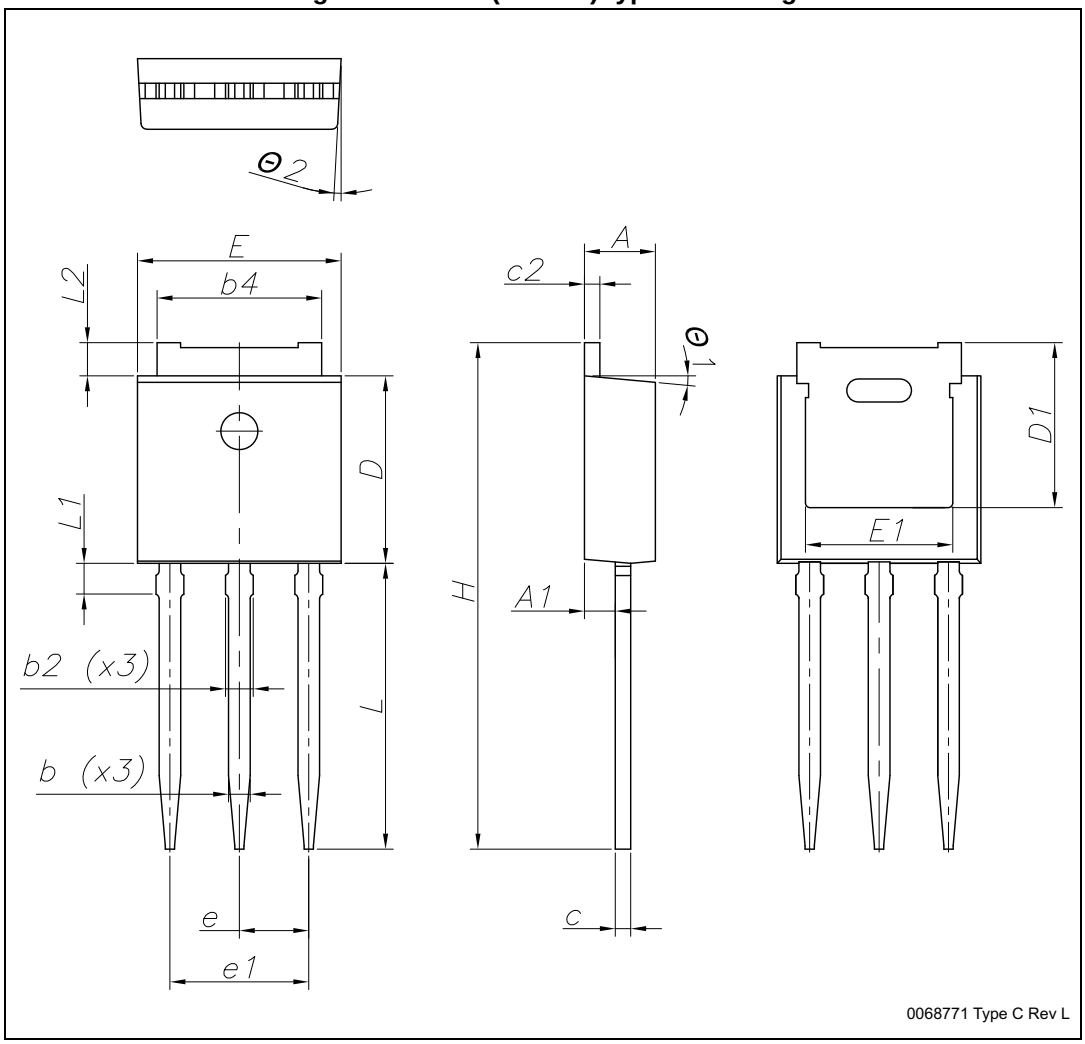


Table 11. IPAK (TO-251) type C mechanical data

Dim.	mm		
	min.	typ.	max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

5 Revision history

Table 12. Document revision history

Date	Revision	Changes
07-Aug-2014	1	First release.
09-Oct-2014	2	Added *Figure 4: Safe operating area for IPAK* and *Figure 5: Thermal impedance for IPAK*. Updated *Section 4: Package mechanical data*. Minor text changes.