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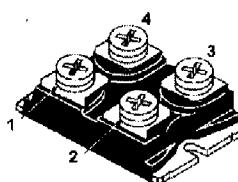
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STE53NA50

N - CHANNEL ENHANCEMENT MODE FAST POWER MOS TRANSISTOR

TYPE	V _{DSS}	R _{Ds(on)}	I _D
STE53NA50	500 V	< 0.085 Ω	53 A

- TYPICAL R_{Ds(on)} = 0.075 Ω
- HIGH CURRENT POWER MODULE
- AVALANCHE RUGGED TECHNOLOGY
- VERY LARGE SOA - LARGE PEAK POWER CAPABILITY
- EASY TO MOUNT
- SAME CURRENT CAPABILITY FOR THE TWO SOURCE TERMINALS
- EXTREMELY LOW R_{th} (Junction to case)
- VERY LOW INTERNAL PARASITIC INDUCTANCE
- ISOLATED PACKAGE UL RECOGNIZED

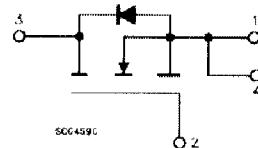


ISOTOP

APPLICATIONS

- SMPS & UPS
- MOTOR CONTROL
- WELDING EQUIPMENT
- OUTPUT STAGE FOR PWM, ULTRASONIC CIRCUITS

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{Ds}	Drain-source Voltage (V _{GS} = 0)	500	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	500	V
V _{GS}	Gate-source Voltage	± 30	V
I _D	Drain Current (continuous) at T _c = 25 °C	53	A
I _D	Drain Current (continuous) at T _c = 100 °C	33	A
I _{DM(•)}	Drain Current (pulsed)	212	A
P _{tot}	Total Dissipation at T _c = 25 °C	460	W
	Derating Factor	3.68	W/°C
T _{stg}	Storage Temperature	-55 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C
V _{iso}	Insulation Withstand Voltage (AC-RMS)	2500	V

(•) Pulse width limited by safe operating area

NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.



STE53NA50

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	0.27	$^{\circ}\text{C}/\text{W}$
R_{thc-h}	Thermal Resistance Case-heatsink With Conductive Grease Applied	Max	0.05	$^{\circ}\text{C}/\text{W}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	26	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	1014	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1\text{ mA}$ $V_{GS} = 0$	500			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}\text{C}$			100 1000	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 30\text{ V}$			± 400	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 1\text{ mA}$	2.25	3	3.75	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 27\text{ A}$		0.075	0.085	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	53			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} \text{ (*)}$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)MAX}$ $I_D = 27\text{ A}$	25			S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		13 1500 450	16 2000 650	nF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	$V_{DD} = 250 \text{ V}$ $I_D = 27 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see test circuit, figure 1)		57 92	80 130	ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 400 \text{ V}$ $I_D = 53 \text{ A}$ $V_{GS} = 10 \text{ V}$		470 54 219	658	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(V_{off})}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 400 \text{ V}$ $I_D = 53 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see test circuit, figure 3)		105 36 145	145 50 205	ns ns ns

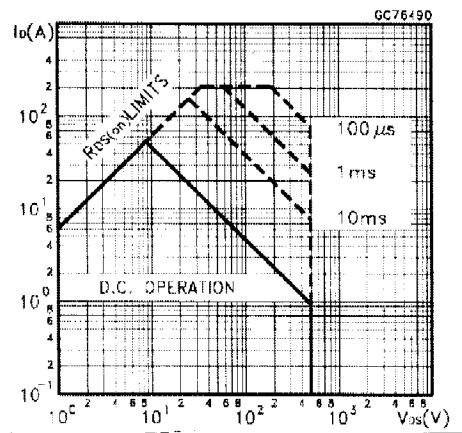
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}(\bullet)$	Source-drain Current Source-drain Current (pulsed)				53 212	A A
$V_{SD} (\ast)$	Forward On Voltage	$I_{SD} = 53 \text{ A}$ $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 53 \text{ A}$ $di/dt = 100 \text{ A}/\mu\text{s}$		1000		ns
Q_{rr}	Reverse Recovery Charge	$V_R = 100 \text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, figure 3)		31.5		μC
I_{RRM}	Reverse Recovery Current			63		A

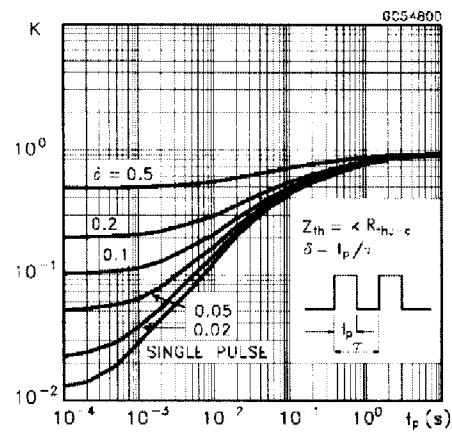
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(*) Pulse width limited by safe operating area

Safe Operating Area for



Thermal Impedance



STE53NA50**ISOTOP MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322

