R61503U

262,144-color, 176RGB x 220-dot graphics a-Si TFT liquid crystal panel controller driver

REJxxxxxxx-xxxxZ
Rev.1.1
March 29, 2007

- **Index**

Description

The R61503U is a one-chip controller driver LSI for 262,144-color TFT panel, incorporating RAM for a maximum 176RGB x 220-dot graphics display and 528-channel source driver. The R61503U provides a one-chip solution to drive TFT panel by generating gate drive signal and liquid crystal drive power supply.

To transfer data efficiently, the R61503U supports high-speed interface via 8-/9-/16-/18-bit port as system interface to microcomputer and high-speed RAM write function. As moving picture interface, the R61503U supports RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0) via 18-/16-/6-bit port and VSYNC interface (system interface + VSYNC). The moving picture interface enables moving picture display at the arbitrary position determined by window address setting. The window address setting enables displaying a moving picture and the data written in the internal RAM simultaneously and allows transferring moving picture data not constrained by the position of still picture display. By writing moving picture data via moving picture interface in the window address area, the number of data transfer can be minimized and the power consumption by the system can be reduced.

The R61503U can operate at low voltage up to 1.65V for the power supply to the I/O interface unit and it incorporates a voltage follower circuit to generate liquid crystal drive voltage. The R61503U's power management functions such as 8-color display and deep standby and so on make this LSI an ideal driver for the medium or small sized portable products such as digital cellular phones and small PDAs, where long battery life is a major concern.

Features

- One-chip controller driver for 176RGB x 220-dot graphics display in 262,144 colors on TFT panel
- One-chip solution for a-Si TFT panel
- System interface
  - High-speed interface via 8-, 9-, 16-, 18-bit parallel ports
  - Clock synchronous serial interface
- Moving picture display interface
  - RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0) via 6-, 16-, 18-bit ports
  - VSYNC interface (System interface + VSYNC)
- High-speed RAM write function
- Window address function to specify a rectangular area in the internal RAM to write data
  - Writes data within a rectangular area on the internal RAM via moving picture interface
  - Reduces data transfer by specifying the area on the RAM to rewrite data
  - Enables displaying the data in the still picture RAM area with a moving picture simultaneously
- Color display control functions
  - γ-correction function to display in 262k colors
  - 1-line unit vertical scroll function
- Low -power consumption architecture (allowing direct input of interface I/O power supply)
  - Deep standby function
  - 8-color display function
  - Partial display function (Max. 32,768 colors)
  - Input power supply voltages: Vcc = 2.5V ~ 3.6 V (logic regulator power supply)
    IOVcc = 1.65V ~ 3.6 V (interface I/O power supply)
    Vci = 2.5V ~ 3.3 V (liquid crystal analog circuit power supply)
    (Vci-VCL ≤ 6.0V)
- Incorporates a liquid crystal drive power supply circuit
  - Source driver liquid crystal drive/Vcom power supply: DDVDH-AGND = 4.5V ~ 6.0V
  - Gate drive power supply: VGH-VGL ≤ 28.0V
  - Vcom drive (Vcom power supply): VcomH = (DDVDH+0.5)V ~ 2.5V
    VcomL = (Vci+0.5)V ~ GND
- 87,120-byte internal RAM
- Internal liquid crystal drive circuit: 528-channel source output and 220-channel gate output
- N-line-/frame-inversion liquid crystal drive
- Internal oscillator, Hardware Reset
- Reversible source output shift direction
- TFT storage capacitor: Cst only
- Internal NV memory: for user identification code (4 bits) and Vcom level adjustment (12 bits)

Table 1 R61503U's power supply main specifications

No.	Item		R61503U
1	TFT data lines		528 output
2	TFT gate lines		220 output
3	TFT display storage capacitor		Cst only (Common Vcom formula)
4	Liquid crystal drive output	S1~S528	V0 ~ V31 grayscales
		G1~G220	VGH-VGL
		Vcom	VcomH/VcomL
5	Input voltage	IOVcc (interface voltage)	1.65V ~ 3.60V Power supply to IM0/ID, IM1-3, RESET, DB17-0, RD, SDI, SDO, WR/SCL, RS, CS*, VSYNC, HSYNC, DOTCLK, ENABLE Connect to Vcc and Vci on the FPC when IOVcc, Vcc and Vci are at the same electrical potential.
		Vcc (logic regulator power supply) see Note 1	2.50V ~ 3.60V Connect to IOVcc and Vci on the FPC when IOVcc, Vcc and Vci are at the same electrical potential.
		VDD(Internal logic power supply) see Note 2	1.5V
		Vci (liquid crystal drive power supply) see Note 2	2.50V ~ 3.30V Connect to IOVcc and Vcc on the when IOVcc, Vcc and Vci are at the same electrical potential.
5	Internal step-up circuits	DDVDH	Vci1 x 2
		VGH	Vci1 x 6, x 5, x 4
		VGL	Vci1 x –2, x -3, x -4, x -5

Notes: 1. When the internal logic regulator is used.

2. Generated from the internal logic regulator power supply circuit.

Block Diagram

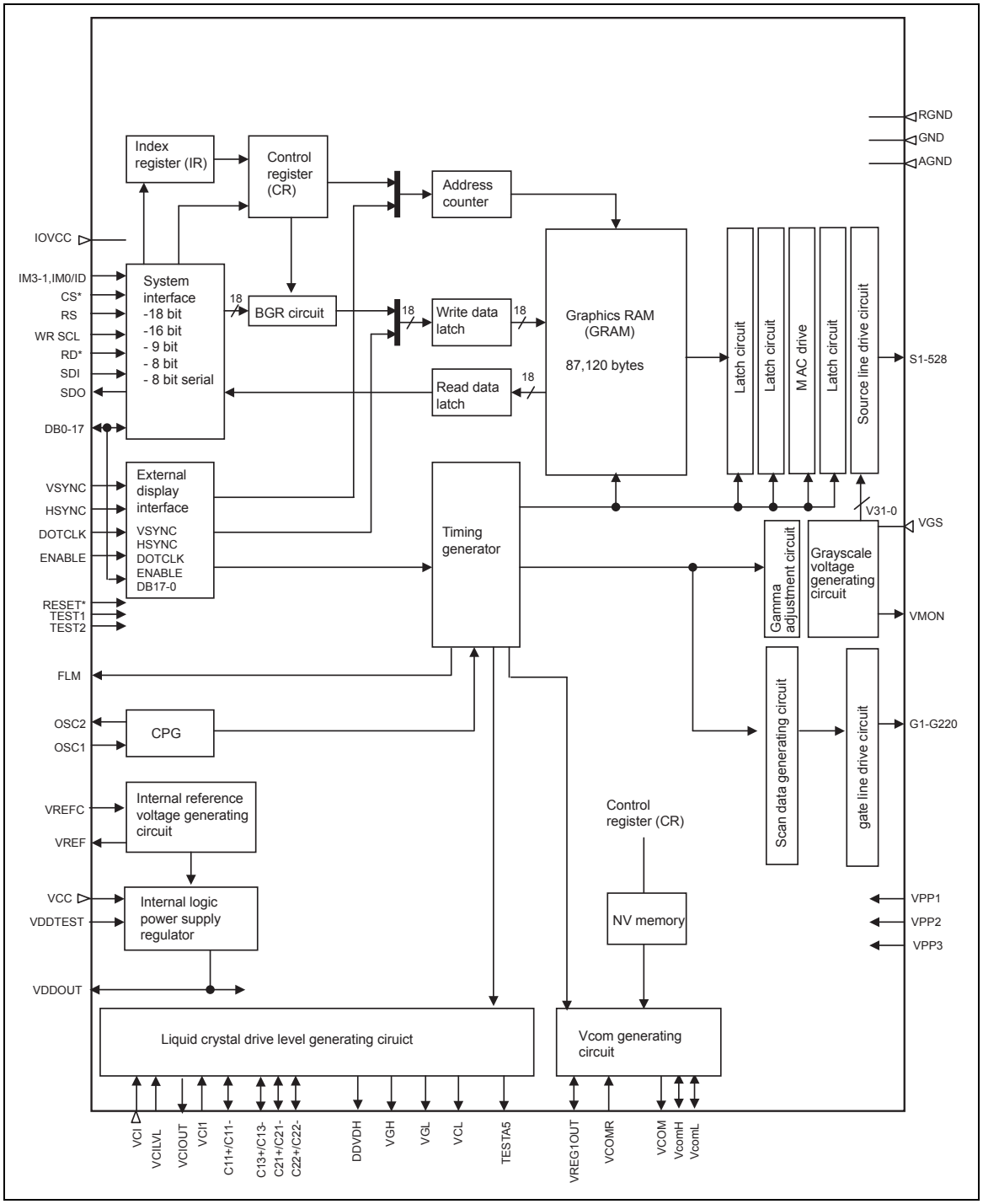


Figure 1

Pin Function

Table 2 Interface

<table>
<tr><th>Signal</th><th>Number</th><th>I/O</th><th>Connect to</th><th>Function</th><th>When not in use</th></tr>
<tr><td>IM3-1
IM0/ID</td><td>4</td><td>I</td><td>GND or IOVcc</td><td>Selects MPU interface format. Amplitude: IOVCC-IOGND.
When selecting clock synchronous serial interface, IM0 pin is used to set the device code ID.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ID</th><th>MPU interface format</th><th>DB pins</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>Clock synchronous serial interface</td><td>SDI/SDO</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>*</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td></tr>
<tr><td>1</td><td>1</td><td>*</td><td>*</td><td>Setting disabled</td><td>-</td></tr>
</table></td><td>-</td></tr>
<tr><td>CS*</td><td>1</td><td>I</td><td>MPU</td><td>Chip select signal. Amplitude: IOVcc-GND
Low: the R61503U is selected and accessible
High: the R61503U is not selected and not accessible.</td><td>-</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Register select signal. Amplitude: IOVcc-GND
Low: select Index or status register
High: select data register</td><td>IOVcc</td></tr>
<tr><td>WR*/SCL</td><td>1</td><td>I</td><td>MPU</td><td>Write strobe signal in 80-system bus interface operation and enables write operation when WR* is low. Synchronous clock signal (SCL) in serial interface operation.
Amplitude: IOVcc-GND</td><td>IOVcc</td></tr>
<tr><td>RD*</td><td>1</td><td>I</td><td>MPU</td><td>Read strobe signal in 80-system bus interface operation and enables read operation when RD* is low.
Amplitude: IOVcc-GND</td><td>IOVcc</td></tr>
<tr><td>SDI</td><td>1</td><td>I</td><td>MPU</td><td>Serial data input (SDI) pin in serial interface operation. The data is inputted on the rising edge of the SCL signal. When DAKE = 1, chip select signal is outputted for DMA transfer single address mode. In this case, the R61503U becomes accessible when the signal is Low and it becomes inaccessible when the signal is High. Amplitude: IOVcc-GND</td><td>GND or IOVcc</td></tr>
<tr><td>SDO</td><td>1</td><td>O</td><td>MPU</td><td>Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal.
Amplitude: IOVcc-GND</td><td>Open</td></tr>
</table>

Table 3 Interface (continued)

Signal	Number	I/O	Connect to	Function	When not in use
DB0-DB17	18	I/O	MPU	Parallel bi-directional data bus for 80-system interface operation (Amplitude: IOVcc-GND). Fix unused pins to either IOVcc or GND level. 8-bit I/F: DB17-DB10 are used. 9-bit I/F: DB17-DB9 are used. 16-bit I/F: DB17-DB10 and DB8-1 are used. 18-bit I/F: DB17-DB0 are used. Parallel bi-directional data bus for RGB interface operation (Amplitude: IOVcc-GND). 6-bit I/F: DB17-DB12 are used. 16-bit I/F: DB17-DB13 and DB11-1 are used. 18-bit I/F: DB17-DB0 are used.	GND or IOVCC
ENABLE	1	I	MPU	Data enable signal for RGB interface operation. (Amplitude: IOVcc-GND). Low: accessible (select) High: Note accessible (Not select) The polarity of ENABLE signal can be inverted by setting the EPL bit.	GND or IOVcc
VSYNC	1	I	MPU	Frame synchronous signal for RGB interface operation. Low active. (Amplitude: IOVcc-GND).	GND or IOVcc
HSYNC	1	I	MPU	Line synchronous signal for RGB interface operation. Low active. (Amplitude: IOVcc-GND).	GND or IOVcc
DOTCLK	1	I	MPU	Dot clock signal for RGB interface operation. The data is inputted on the rising edge of DOTCLK. (Amplitude: IOVcc-GND).	GND or IOVcc
FLM	1	O	MPU	Frame head pulse to synchronize RAM data write operation with the frame head position. (Amplitude: IOVcc-GND).	Open

Table 4 Reset an d oscillator

Signal	Number	I/O	Connect to	Function	When not in use
RESET*	1	I	Reset generating circuit	Reset signal. Initializes the R61503U when RESET input is low. Make sure to execute a power-on reset when turning on the power supply. (Amplitude: IOVcc-GND).	-
OSC1 OSC2	2	I O	Oscillator	Connect an external resistor for RC oscillation.	-

Table 5 Power supply

<table>
<tr><th>Signal</th><th>Number</th><th>I/O</th><th>Connect to</th><th>Function</th><th>When not in use</th></tr>
<tr><td>Vcc</td><td>1</td><td>-</td><td>Power supply</td><td>Power supply to internal logic regulator circuit:
Vcc = 2.5V~3.6V. Vcc ≥ IOVcc</td><td>-</td></tr>
<tr><td>GND</td><td>1</td><td>-</td><td>Power supply</td><td>Internal logic GND: GND = 0V.</td><td>-</td></tr>
<tr><td>RGND</td><td>1</td><td>-</td><td>Power supply</td><td>Internal RAM GND: RGND and GND must be at the same electrical potential. In case of COG, connect to GND on the FPC to prevent noise.</td><td>-</td></tr>
<tr><td>VDD
VDDOUT</td><td>1</td><td>O</td><td>Stabilizing capacitor</td><td>Internal logic regulator output used for internal logic power supply. Connect a stabilizing capacitor.</td><td>-</td></tr>
<tr><td>IOVcc</td><td>1</td><td>-</td><td>Power supply</td><td>Power supply to interface pins: RESET; CS; WR; RD; RS; DB17-0; VSYNC; HSYNC; DOTCLK; ENABLE.
IOVcc = 1.65V ~ 3.6V. Vcc ≥ IOVcc
In case of COG, connect to Vcc on the FPC if IOVcc=Vcc, to prevent noise.</td><td>-</td></tr>
<tr><td>AGND</td><td>1</td><td>-</td><td>Power supply</td><td>Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.</td><td>-</td></tr>
<tr><td>Vci</td><td>1</td><td>I</td><td>Power supply</td><td>Power supply to liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.</td><td>-</td></tr>
<tr><td>VciLVL</td><td>1</td><td>I</td><td>Reference power supply</td><td>VciLVL and Vci must be at the same electrical potential. Connect VciLVL to an external power supply of 2.5V ~ 3.3V. In case of COG, connect to Vci on the FPC to prevent noise.</td><td>-</td></tr>
<tr><td>VPP1</td><td>1</td><td>I</td><td>Power supply or open</td><td rowspan="3">Internal NV memory power supply. Apply the following voltages on VPP1 ~ VPP3 respectively according to the power supply ON sequence.
<table>
<tr><th>Operation mode</th><th>VPP1</th><th>VP2</th><th>VPP3</th></tr>
<tr><td>NV memory write</td><td>9.0±0.3V</td><td>7.5±0.3V</td><td>GND</td></tr>
<tr><td>NV memory read</td><td>Open</td><td>Open</td><td>Open</td></tr>
</table></td><td>Open</td></tr>
<tr><td>VPP2</td><td>1</td><td>I</td><td>Power supply or open</td><td>Open</td></tr>
<tr><td>VPP3</td><td>1</td><td>I</td><td>Power supply or open</td><td>Open</td></tr>
</table>

Table 6 Step-up circuit

Signal	Number	I/O	Connect to	Function	When not in use
Vci1	1	I/O	VciOUT	Internal reference voltage generated between Vci and GND. The output voltage level is set by instruction (VC). Reference voltage for step-up circuit 1. Vci1 must be set so that the output voltages DDVDH, VGH, VGL are generated within the respective setting ranges.	-
DDVDH	1	O	Stabilizing capacitor	DDVDH is generated from Vci1 x 2 in the step-up circuit 1. The step-up factor is set by instruction (BT). DDVDH = 4.5V ~ 6.0V Liquid crystal power supply for source driver.	-
VGH	1	O	Stabilizing capacitor, LCD panel	Liquid crystal drive power supply generated from Vci1 and DDVDH in the step-up circuit 2 (See Note below). The step-up factor is set by instruction (BT).	-
VGL	1	O	Stabilizing capacitor, LCD panel	Liquid crystal drive power supply generated from Vci1 and DDVDH in the step-up circuit 2 (See Note below). The step-up factor is set by instruction (BT).	-
C11+, C11	2	I O	Step-up capacitor	Capacitor connection pins of the step-up circuit 1.	-
C13+, C13- C21+, C21- C22+, C22-	6	I O	Step-up capacitor	Capacitor connection pins of the step-up circuit 2.	-
VCL	1	O	Stabilizing capacitor	Power supply for VcomL drive.	-

Note: Make sure VGH-VGL amplitude = Max. 28V.

Table 7 Liquid crystal drive

Signal	Number	I/O	Connect to	Function	When not in use
VREG1 OUT	1	O	Stabilizing capacitor	VREG1OUT is generated from VciLVL and the output level is set by instruction (VRH) and used for (1) source driver grayscale voltage VDH, (2) VcomH level reference voltage, and (3) Vcom amplitude reference voltage. Connect to a stabilizing capacitor when it is in use. VREG1OUT = 3.5V ~ (DDVDH – 0.5)V	Open
Vcom	1	O	TFT common electrode	Power supply to TFT common electrode. The Vcom amplitude is determined by VcomH and VcomL levels. The alternating cycle can be set to line cycle or frame cycle. Also halting/starting Vcom output can be controlled by instruction (VON).	Open
VcomH	1	O	Stabilizing capacitor	The High level of Vcom. The VcomH output level can be determined by either internal electronic volume or external variable resistor (VcomR).	Open
VcomL	1	O	Stabilizing capacitor	The Low level of Vcom.	Open
VcomR	1	I	Variable resistor or open	Connect a variable resistor between VREG1OUT and GND when adjusting the VcomH level externally.	Open
VGS	1	I	GND	Reference level of grayscale voltage generating circuit.	-
S1~S528	528	O	LCD	Liquid crystal application voltage. To change the shift direction of segment signal output, set the SS bit as follows. When SS = 0, the data in the RAM address h00000 is output from S1. When SS = 1, the data in the RAM address h00000 is output from S528.	Open
G1~G220	220	O	LCD	Gate output signal Gate select level: VGH Gate non-select level: VGL	Open

Table 8 Liquid crystal drive

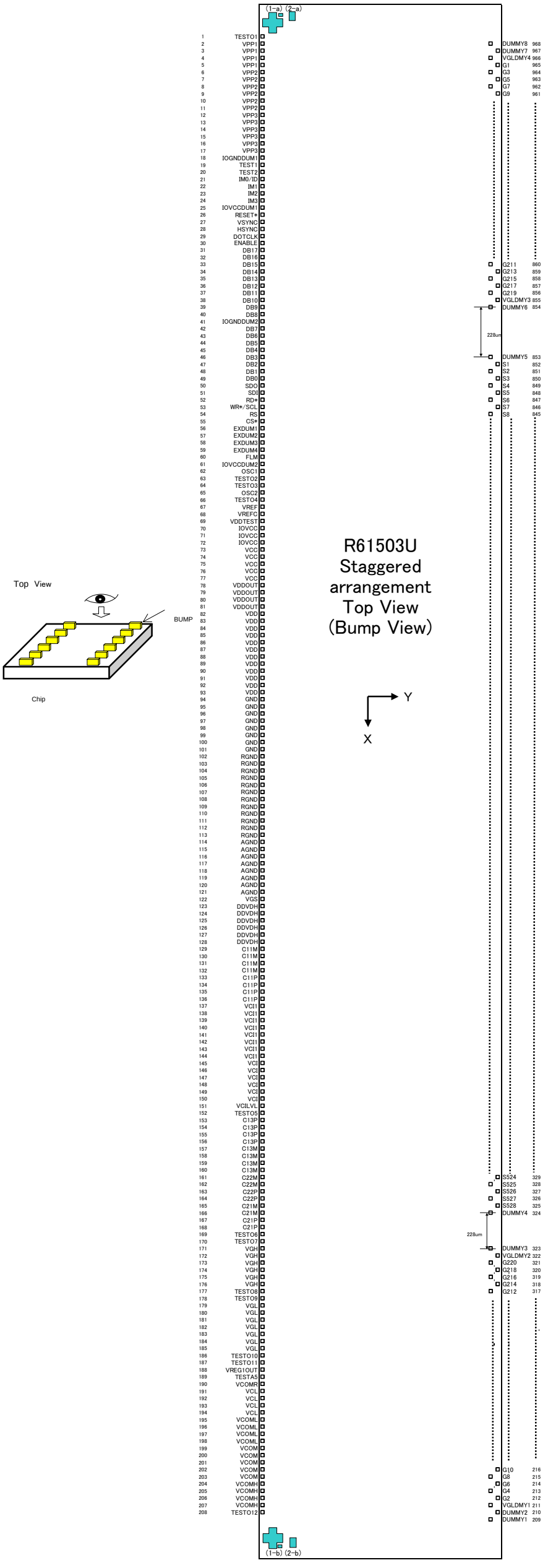
Signal	Number	I/O	Connect to	Function	When not in use
VREFC	1	I	AGND	Test pin. Fix it to GND level.	-
VREF	1	O	Open	Test pin. Leave it open.	Open
VDDTEST	1	I	AGND	Test pin. Fix it to GND level.	-
TESTA5		O	Open	Test pin. Leave it open.	Open
IOVccDUM1, IOVccDUM2	2	O	-	Use when fixing the electrical potential of unused interface pins and fixed pins (IOVcc output). When not in use, leave it open.	Open
GNDDUM1, GNDDUM2	2	O	-	Use when fixing the electrical potential of unused interface pins and fixed pins (GND output). When not in use, leave it open.	Open
DUMMY 1-8	8	-	-	Dummy pads. Leave them open.	Open
VGLDMY 1-4	4	O	-	Dummy pads. Leave them open.	Open
TESTO 1-15	32	O	-	Dummy pads. Leave them open.	Open
EXDUM1-4	1	-	-	Leave them open.	Open
TEST1-2	1	I	GND	Test pins. Connect to GND.	GND

Patents of dummy pin which is used to fix pin to Vcc or GND are pending and granted.

PATENT ISSUED: United States Patent No. 6,323,930
PATENT PENDING: Japanese Application No. 10-514484
Korean Application No. 19997002322
Taiwanese Application No.086103756
(PCT/JP96/02728(W098/12597)

R61503U Pad Arrangement

Rev0.0 2006.06.08



Top View

R61503U
Staggered
arrangement
Top View
(Bump View)

Chip Size

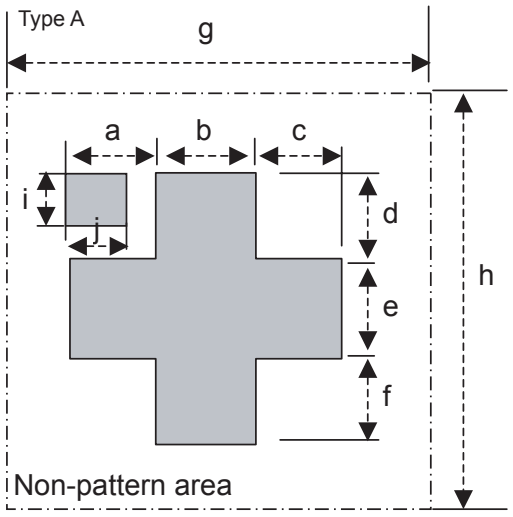
Chip size: 15.20 mm x 1.07 mm
Chip thickness: 280 μm (typ.)
Pad coordinates: Pad center
Pad origin: Chip center

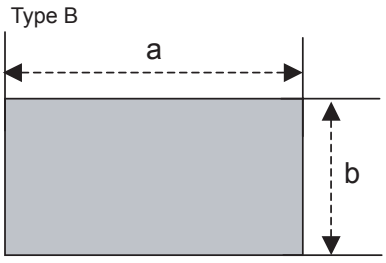
Au Bump size:
(1) 50 μm x 80 mμ No.1 ~ No.208
(2) 19 μm x 110 μm No.209 ~ No.968

Au bump pitch: See pad coordinates.
Au bump height: 15m (typ.)
No. in the figure corresponds to No. in pad coordinate table.

Alignment mark

	Alignment mark	X	Y
1-a	Type A	-7465	-400
1-b	Type A	7465	400
2-a	Type B	-7500	-293
2-b	Type B	7500	293





Unit (μm)
a: 30
b: 30
c: 30
d: 30
e: 30
f: 30
g: 150
h: 150
i: 20
j: 20

Unit (μm)
a: 70
b: 53

Figure 2

R61503U PAD Coordinates (No.1) (Unit: μm) 2006.6.8 rev0.0

pad No	pad name	X	Y	pad No	pad name	X	Y
1	TESTO1	-7245	-430	51	SDI	-3745	-430
2	VPP1	-7175	-430	52	RD*	-3675	-430
3	VPP1	-7105	-430	53	WR*/SCL	-3605	-430
4	VPP1	-7035	-430	54	RS	-3535	-430
5	VPP1	-6965	-430	55	CS*	-3465	-430
6	VPP2	-6895	-430	56	EXDUM1	-3395	-430
7	VPP2	-6825	-430	57	EXDUM2	-3325	-430
8	VPP2	-6755	-430	58	EXDUM3	-3255	-430
9	VPP2	-6685	-430	59	EXDUM4	-3185	-430
10	VPP2	-6615	-430	60	FLM	-3115	-430
11	VPP2	-6545	-430	61	IOVCCDUM2	-3045	-430
12	VPP3	-6475	-430	62	OSC1	-2975	-430
13	VPP3	-6405	-430	63	TESTO2	-2905	-430
14	VPP3	-6335	-430	64	TESTO3	-2835	-430
15	VPP3	-6265	-430	65	OSC2	-2765	-430
16	VPP3	-6195	-430	66	TESTO4	-2695	-430
17	VPP3	-6125	-430	67	VREF	-2625	-430
18	IOGNDDUM1	-6055	-430	68	VREFC	-2555	-430
19	TEST1	-5985	-430	69	VDDTEST	-2485	-430
20	TEST2	-5915	-430	70	IOVCC	-2415	-430
21	IM0/ID	-5845	-430	71	IOVCC	-2345	-430
22	IM1	-5775	-430	72	IOVCC	-2275	-430
23	IM2	-5705	-430	73	VCC	-2205	-430
24	IM3	-5635	-430	74	VCC	-2135	-430
25	IOVCCDUM1	-5565	-430	75	VCC	-2065	-430
26	RESET*	-5495	-430	76	VCC	-1995	-430
27	VSYNC	-5425	-430	77	VCC	-1925	-430
28	HSYNC	-5355	-430	78	VDDOUT	-1855	-430
29	DOTCLK	-5285	-430	79	VDDOUT	-1785	-430
30	ENABLE	-5215	-430	80	VDDOUT	-1715	-430
31	DB17	-5145	-430	81	VDDOUT	-1645	-430
32	DB16	-5075	-430	82	VDD	-1575	-430
33	DB15	-5005	-430	83	VDD	-1505	-430
34	DB14	-4935	-430	84	VDD	-1435	-430
35	DB13	-4865	-430	85	VDD	-1365	-430
36	DB12	-4795	-430	86	VDD	-1295	-430
37	DB11	-4725	-430	87	VDD	-1225	-430
38	DB10	-4655	-430	88	VDD	-1155	-430
39	DB9	-4585	-430	89	VDD	-1085	-430
40	DB8	-4515	-430	90	VDD	-1015	-430
41	IOGNDDUM2	-4445	-430	91	VDD	-945	-430
42	DB7	-4375	-430	92	VDD	-875	-430
43	DB6	-4305	-430	93	VDD	-805	-430
44	DB5	-4235	-430	94	GND	-735	-430
45	DB4	-4165	-430	95	GND	-665	-430
46	DB3	-4095	-430	96	GND	-595	-430
47	DB2	-4025	-430	97	GND	-525	-430
48	DB1	-3955	-430	98	GND	-455	-430
49	DB0	-3885	-430	99	GND	-385	-430
50	SDO	-3815	-430	100	GND	-315	-430

R61503U PAD Coordinates (No.2) (Unit: μm) 2006.6.8 rev0.0

pad No	pad name	X	Y	pad No	pad name	X	Y
101	GND	-245	-430	151	VCILVL	3255	-430
102	RGND	-175	-430	152	TESTO5	3325	-430
103	RGND	-105	-430	153	C13P	3395	-430
104	RGND	-35	-430	154	C13P	3465	-430
105	RGND	35	-430	155	C13P	3535	-430
106	RGND	105	-430	156	C13P	3605	-430
107	RGND	175	-430	157	C13M	3675	-430
108	RGND	245	-430	158	C13M	3745	-430
109	RGND	315	-430	159	C13M	3815	-430
110	RGND	385	-430	160	C13M	3885	-430
111	RGND	455	-430	161	C22M	3955	-430
112	RGND	525	-430	162	C22M	4025	-430
113	RGND	595	-430	163	C22P	4095	-430
114	AGND	665	-430	164	C22P	4165	-430
115	AGND	735	-430	165	C21M	4235	-430
116	AGND	805	-430	166	C21M	4305	-430
117	AGND	875	-430	167	C21P	4375	-430
118	AGND	945	-430	168	C21P	4445	-430
119	AGND	1015	-430	169	TESTO6	4515	-430
120	AGND	1085	-430	170	TESTO7	4585	-430
121	AGND	1155	-430	171	VGH	4655	-430
122	VGS	1225	-430	172	VGH	4725	-430
123	DDVDH	1295	-430	173	VGH	4795	-430
124	DDVDH	1365	-430	174	VGH	4865	-430
125	DDVDH	1435	-430	175	VGH	4935	-430
126	DDVDH	1505	-430	176	VGH	5005	-430
127	DDVDH	1575	-430	177	TESTO8	5075	-430
128	DDVDH	1645	-430	178	TESTO9	5145	-430
129	C11M	1715	-430	179	VGL	5215	-430
130	C11M	1785	-430	180	VGL	5285	-430
131	C11M	1855	-430	181	VGL	5355	-430
132	C11M	1925	-430	182	VGL	5425	-430
133	C11P	1995	-430	183	VGL	5495	-430
134	C11P	2065	-430	184	VGL	5565	-430
135	C11P	2135	-430	185	VGL	5635	-430
136	C11P	2205	-430	186	TESTO10	5705	-430
137	VCI1	2275	-430	187	TESTO11	5775	-430
138	VCI1	2345	-430	188	VREG1OUT	5845	-430
139	VCI1	2415	-430	189	TESTA5	5915	-430
140	VCI1	2485	-430	190	VCOMR	5985	-430
141	VCI1	2555	-430	191	VCL	6055	-430
142	VCI1	2625	-430	192	VCL	6125	-430
143	VCI1	2695	-430	193	VCL	6195	-430
144	VCI1	2765	-430	194	VCL	6265	-430
145	VCI	2835	-430	195	VCOML	6335	-430
146	VCI	2905	-430	196	VCOML	6405	-430
147	VCI	2975	-430	197	VCOML	6475	-430
148	VCI	3045	-430	198	VCOML	6545	-430
149	VCI	3115	-430	199	VCOM	6615	-430
150	VCI	3185	-430	200	VCOM	6685	-430

R61503U PAD Coordinates (No.3) (Unit: μm) 2006.6.8 rev0.0

pad No	pad name	X	Y	pad No	pad name	X	Y
201	VCOM	6755	-430	251	G80	6631	278
202	VCOM	6825	-430	252	G82	6612	413
203	VCOM	6895	-430	253	G84	6593	278
204	VCOMH	6965	-430	254	G86	6574	413
205	VCOMH	7035	-430	255	G88	6555	278
206	VCOMH	7105	-430	256	G90	6536	413
207	VCOMH	7175	-430	257	G92	6517	278
208	TESTO12	7245	-430	258	G94	6498	413
209	DUMMY1	7429	278	259	G96	6479	278
210	DUMMY2	7410	413	260	G98	6460	413
211	VGLDMY1	7391	278	261	G100	6441	278
212	G2	7372	413	262	G102	6422	413
213	G4	7353	278	263	G104	6403	278
214	G6	7334	413	264	G106	6384	413
215	G8	7315	278	265	G108	6365	278
216	G10	7296	413	266	G110	6346	413
217	G12	7277	278	267	G112	6327	278
218	G14	7258	413	268	G114	6308	413
219	G16	7239	278	269	G116	6289	278
220	G18	7220	413	270	G118	6270	413
221	G20	7201	278	271	G120	6251	278
222	G22	7182	413	272	G122	6232	413
223	G24	7163	278	273	G124	6213	278
224	G26	7144	413	274	G126	6194	413
225	G28	7125	278	275	G128	6175	278
226	G30	7106	413	276	G130	6156	413
227	G32	7087	278	277	G132	6137	278
228	G34	7068	413	278	G134	6118	413
229	G36	7049	278	279	G136	6099	278
230	G38	7030	413	280	G138	6080	413
231	G40	7011	278	281	G140	6061	278
232	G42	6992	413	282	G142	6042	413
233	G44	6973	278	283	G144	6023	278
234	G46	6954	413	284	G146	6004	413
235	G48	6935	278	285	G148	5985	278
236	G50	6916	413	286	G150	5966	413
237	G52	6897	278	287	G152	5947	278
238	G54	6878	413	288	G154	5928	413
239	G56	6859	278	289	G156	5909	278
240	G58	6840	413	290	G158	5890	413
241	G60	6821	278	291	G160	5871	278
242	G62	6802	413	292	G162	5852	413
243	G64	6783	278	293	G164	5833	278
244	G66	6764	413	294	G166	5814	413
245	G68	6745	278	295	G168	5795	278
246	G70	6726	413	296	G170	5776	413
247	G72	6707	278	297	G172	5757	278
248	G74	6688	413	298	G174	5738	413
249	G76	6669	278	299	G176	5719	278
250	G78	6650	413	300	G178	5700	413

R61503U PAD Coordinates (No.4) (Unit: μm) 2006.6.8 rev0.0

pad No	pad name	X	Y	pad No	pad name	X	Y
301	G180	5681	278	351	S502	4522	413
302	G182	5662	413	352	S501	4503	278
303	G184	5643	278	353	S500	4484	413
304	G186	5624	413	354	S499	4465	278
305	G188	5605	278	355	S498	4446	413
306	G190	5586	413	356	S497	4427	278
307	G192	5567	278	357	S496	4408	413
308	G194	5548	413	358	S495	4389	278
309	G196	5529	278	359	S494	4370	413
310	G198	5510	413	360	S493	4351	278
311	G200	5491	278	361	S492	4332	413
312	G202	5472	413	362	S491	4313	278
313	G204	5453	278	363	S490	4294	413
314	G206	5434	413	364	S489	4275	278
315	G208	5415	278	365	S488	4256	413
316	G210	5396	413	366	S487	4237	278
317	G212	5377	278	367	S486	4218	413
318	G214	5358	413	368	S485	4199	278
319	G216	5339	278	369	S484	4180	413
320	G218	5320	413	370	S483	4161	278
321	G220	5301	278	371	S482	4142	413
322	VGLDMY2	5282	413	372	S481	4123	278
323	DUMMY3	5263	278	373	S480	4104	413
324	DUMMY4	5035	278	374	S479	4085	278
325	S528	5016	413	375	S478	4066	413
326	S527	4997	278	376	S477	4047	278
327	S526	4978	413	377	S476	4028	413
328	S525	4959	278	378	S475	4009	278
329	S524	4940	413	379	S474	3990	413
330	S523	4921	278	380	S473	3971	278
331	S522	4902	413	381	S472	3952	413
332	S521	4883	278	382	S471	3933	278
333	S520	4864	413	383	S470	3914	413
334	S519	4845	278	384	S469	3895	278
335	S518	4826	413	385	S468	3876	413
336	S517	4807	278	386	S467	3857	278
337	S516	4788	413	387	S466	3838	413
338	S515	4769	278	388	S465	3819	278
339	S514	4750	413	389	S464	3800	413
340	S513	4731	278	390	S463	3781	278
341	S512	4712	413	391	S462	3762	413
342	S511	4693	278	392	S461	3743	278
343	S510	4674	413	393	S460	3724	413
344	S509	4655	278	394	S459	3705	278
345	S508	4636	413	395	S458	3686	413
346	S507	4617	278	396	S457	3667	278
347	S506	4598	413	397	S456	3648	413
348	S505	4579	278	398	S455	3629	278
349	S504	4560	413	399	S454	3610	413
350	S503	4541	278	400	S453	3591	278

R61503U PAD Coordinates (No.5) (Unit: μm) 2006.6.8 rev0.0

pad No	pad name	X	Y	pad No	pad name	X	Y
401	S452	3572	413	451	S402	2622	413
402	S451	3553	278	452	S401	2603	278
403	S450	3534	413	453	S400	2584	413
404	S449	3515	278	454	S399	2565	278
405	S448	3496	413	455	S398	2546	413
406	S447	3477	278	456	S397	2527	278
407	S446	3458	413	457	S396	2508	413
408	S445	3439	278	458	S395	2489	278
409	S444	3420	413	459	S394	2470	413
410	S443	3401	278	460	S393	2451	278
411	S442	3382	413	461	S392	2432	413
412	S441	3363	278	462	S391	2413	278
413	S440	3344	413	463	S390	2394	413
414	S439	3325	278	464	S389	2375	278
415	S438	3306	413	465	S388	2356	413
416	S437	3287	278	466	S387	2337	278
417	S436	3268	413	467	S386	2318	413
418	S435	3249	278	468	S385	2299	278
419	S434	3230	413	469	S384	2280	413
420	S433	3211	278	470	S383	2261	278
421	S432	3192	413	471	S382	2242	413
422	S431	3173	278	472	S381	2223	278
423	S430	3154	413	473	S380	2204	413
424	S429	3135	278	474	S379	2185	278
425	S428	3116	413	475	S378	2166	413
426	S427	3097	278	476	S377	2147	278
427	S426	3078	413	477	S376	2128	413
428	S425	3059	278	478	S375	2109	278
429	S424	3040	413	479	S374	2090	413
430	S423	3021	278	480	S373	2071	278
431	S422	3002	413	481	S372	2052	413
432	S421	2983	278	482	S371	2033	278
433	S420	2964	413	483	S370	2014	413
434	S419	2945	278	484	S369	1995	278
435	S418	2926	413	485	S368	1976	413
436	S417	2907	278	486	S367	1957	278
437	S416	2888	413	487	S366	1938	413
438	S415	2869	278	488	S365	1919	278
439	S414	2850	413	489	S364	1900	413
440	S413	2831	278	490	S363	1881	278
441	S412	2812	413	491	S362	1862	413
442	S411	2793	278	492	S361	1843	278
443	S410	2774	413	493	S360	1824	413
444	S409	2755	278	494	S359	1805	278
445	S408	2736	413	495	S358	1786	413
446	S407	2717	278	496	S357	1767	278
447	S406	2698	413	497	S356	1748	413
448	S405	2679	278	498	S355	1729	278
449	S404	2660	413	499	S354	1710	413
450	S403	2641	278	500	S353	1691	278

R61503U PAD Coordinates (No.6) (Unit: μm) 2006.6.8 rev0.0

pad No	pad name	X	Y	pad No	pad name	X	Y
501	S352	1672	413	551	S302	722	413
502	S351	1653	278	552	S301	703	278
503	S350	1634	413	553	S300	684	413
504	S349	1615	278	554	S299	665	278
505	S348	1596	413	555	S298	646	413
506	S347	1577	278	556	S297	627	278
507	S346	1558	413	557	S296	608	413
508	S345	1539	278	558	S295	589	278
509	S344	1520	413	559	S294	570	413
510	S343	1501	278	560	S293	551	278
511	S342	1482	413	561	S292	532	413
512	S341	1463	278	562	S291	513	278
513	S340	1444	413	563	S290	494	413
514	S339	1425	278	564	S289	475	278
515	S338	1406	413	565	S288	456	413
516	S337	1387	278	566	S287	437	278
517	S336	1368	413	567	S286	418	413
518	S335	1349	278	568	S285	399	278
519	S334	1330	413	569	S284	380	413
520	S333	1311	278	570	S283	361	278
521	S332	1292	413	571	S282	342	413
522	S331	1273	278	572	S281	323	278
523	S330	1254	413	573	S280	304	413
524	S329	1235	278	574	S279	285	278
525	S328	1216	413	575	S278	266	413
526	S327	1197	278	576	S277	247	278
527	S326	1178	413	577	S276	228	413
528	S325	1159	278	578	S275	209	278
529	S324	1140	413	579	S274	190	413
530	S323	1121	278	580	S273	171	278
531	S322	1102	413	581	S272	152	413
532	S321	1083	278	582	S271	133	278
533	S320	1064	413	583	S270	114	413
534	S319	1045	278	584	S269	95	278
535	S318	1026	413	585	S268	76	413
536	S317	1007	278	586	S267	57	278
537	S316	988	413	587	S266	38	413
538	S315	969	278	588	S265	19	278
539	S314	950	413	589	S264	-19	278
540	S313	931	278	590	S263	-38	413
541	S312	912	413	591	S262	-57	278
542	S311	893	278	592	S261	-76	413
543	S310	874	413	593	S260	-95	278
544	S309	855	278	594	S259	-114	413
545	S308	836	413	595	S258	-133	278
546	S307	817	278	596	S257	-152	413
547	S306	798	413	597	S256	-171	278
548	S305	779	278	598	S255	-190	413
549	S304	760	413	599	S254	-209	278
550	S303	741	278	600	S253	-228	413

R61503U PAD Coordinates (No.7) (Unit: μm) 2006.6.8 rev0.0

pad No	pad name	X	Y	pad No	pad name	X	Y
601	S252	-247	278	651	S202	-1197	278
602	S251	-266	413	652	S201	-1216	413
603	S250	-285	278	653	S200	-1235	278
604	S249	-304	413	654	S199	-1254	413
605	S248	-323	278	655	S198	-1273	278
606	S247	-342	413	656	S197	-1292	413
607	S246	-361	278	657	S196	-1311	278
608	S245	-380	413	658	S195	-1330	413
609	S244	-399	278	659	S194	-1349	278
610	S243	-418	413	660	S193	-1368	413
611	S242	-437	278	661	S192	-1387	278
612	S241	-456	413	662	S191	-1406	413
613	S240	-475	278	663	S190	-1425	278
614	S239	-494	413	664	S189	-1444	413
615	S238	-513	278	665	S188	-1463	278
616	S237	-532	413	666	S187	-1482	413
617	S236	-551	278	667	S186	-1501	278
618	S235	-570	413	668	S185	-1520	413
619	S234	-589	278	669	S184	-1539	278
620	S233	-608	413	670	S183	-1558	413
621	S232	-627	278	671	S182	-1577	278
622	S231	-646	413	672	S181	-1596	413
623	S230	-665	278	673	S180	-1615	278
624	S229	-684	413	674	S179	-1634	413
625	S228	-703	278	675	S178	-1653	278
626	S227	-722	413	676	S177	-1672	413
627	S226	-741	278	677	S176	-1691	278
628	S225	-760	413	678	S175	-1710	413
629	S224	-779	278	679	S174	-1729	278
630	S223	-798	413	680	S173	-1748	413
631	S222	-817	278	681	S172	-1767	278
632	S221	-836	413	682	S171	-1786	413
633	S220	-855	278	683	S170	-1805	278
634	S219	-874	413	684	S169	-1824	413
635	S218	-893	278	685	S168	-1843	278
636	S217	-912	413	686	S167	-1862	413
637	S216	-931	278	687	S166	-1881	278
638	S215	-950	413	688	S165	-1900	413
639	S214	-969	278	689	S164	-1919	278
640	S213	-988	413	690	S163	-1938	413
641	S212	-1007	278	691	S162	-1957	278
642	S211	-1026	413	692	S161	-1976	413
643	S210	-1045	278	693	S160	-1995	278
644	S209	-1064	413	694	S159	-2014	413
645	S208	-1083	278	695	S158	-2033	278
646	S207	-1102	413	696	S157	-2052	413
647	S206	-1121	278	697	S156	-2071	278
648	S205	-1140	413	698	S155	-2090	413
649	S204	-1159	278	699	S154	-2109	278
650	S203	-1178	413	700	S153	-2128	413

R61503U PAD Coordinates (No.8) (Unit: μm) 2006.6.8 rev0.0

pad No	pad name	X	Y	pad No	pad name	X	Y
701	S152	-2147	278	751	S102	-3097	278
702	S151	-2166	413	752	S101	-3116	413
703	S150	-2185	278	753	S100	-3135	278
704	S149	-2204	413	754	S99	-3154	413
705	S148	-2223	278	755	S98	-3173	278
706	S147	-2242	413	756	S97	-3192	413
707	S146	-2261	278	757	S96	-3211	278
708	S145	-2280	413	758	S95	-3230	413
709	S144	-2299	278	759	S94	-3249	278
710	S143	-2318	413	760	S93	-3268	413
711	S142	-2337	278	761	S92	-3287	278
712	S141	-2356	413	762	S91	-3306	413
713	S140	-2375	278	763	S90	-3325	278
714	S139	-2394	413	764	S89	-3344	413
715	S138	-2413	278	765	S88	-3363	278
716	S137	-2432	413	766	S87	-3382	413
717	S136	-2451	278	767	S86	-3401	278
718	S135	-2470	413	768	S85	-3420	413
719	S134	-2489	278	769	S84	-3439	278
720	S133	-2508	413	770	S83	-3458	413
721	S132	-2527	278	771	S82	-3477	278
722	S131	-2546	413	772	S81	-3496	413
723	S130	-2565	278	773	S80	-3515	278
724	S129	-2584	413	774	S79	-3534	413
725	S128	-2603	278	775	S78	-3553	278
726	S127	-2622	413	776	S77	-3572	413
727	S126	-2641	278	777	S76	-3591	278
728	S125	-2660	413	778	S75	-3610	413
729	S124	-2679	278	779	S74	-3629	278
730	S123	-2698	413	780	S73	-3648	413
731	S122	-2717	278	781	S72	-3667	278
732	S121	-2736	413	782	S71	-3686	413
733	S120	-2755	278	783	S70	-3705	278
734	S119	-2774	413	784	S69	-3724	413
735	S118	-2793	278	785	S68	-3743	278
736	S117	-2812	413	786	S67	-3762	413
737	S116	-2831	278	787	S66	-3781	278
738	S115	-2850	413	788	S65	-3800	413
739	S114	-2869	278	789	S64	-3819	278
740	S113	-2888	413	790	S63	-3838	413
741	S112	-2907	278	791	S62	-3857	278
742	S111	-2926	413	792	S61	-3876	413
743	S110	-2945	278	793	S60	-3895	278
744	S109	-2964	413	794	S59	-3914	413
745	S108	-2983	278	795	S58	-3933	278
746	S107	-3002	413	796	S57	-3952	413
747	S106	-3021	278	797	S56	-3971	278
748	S105	-3040	413	798	S55	-3990	413
749	S104	-3059	278	799	S54	-4009	278
750	S103	-3078	413	800	S53	-4028	413

R61503U PAD Coordinates (No.9) (Unit: μm) 2006.6.8 rev0.0

pad No	pad name	X	Y	pad No	pad name	X	Y
801	S52	-4047	278	851	S2	-4997	278
802	S51	-4066	413	852	S1	-5016	413
803	S50	-4085	278	853	DUMMY5	-5035	278
804	S49	-4104	413	854	DUMMY6	-5263	278
805	S48	-4123	278	855	VGLDMY3	-5282	413
806	S47	-4142	413	856	G219	-5301	278
807	S46	-4161	278	857	G217	-5320	413
808	S45	-4180	413	858	G215	-5339	278
809	S44	-4199	278	859	G213	-5358	413
810	S43	-4218	413	860	G211	-5377	278
811	S42	-4237	278	861	G209	-5396	413
812	S41	-4256	413	862	G207	-5415	278
813	S40	-4275	278	863	G205	-5434	413
814	S39	-4294	413	864	G203	-5453	278
815	S38	-4313	278	865	G201	-5472	413
816	S37	-4332	413	866	G199	-5491	278
817	S36	-4351	278	867	G197	-5510	413
818	S35	-4370	413	868	G195	-5529	278
819	S34	-4389	278	869	G193	-5548	413
820	S33	-4408	413	870	G191	-5567	278
821	S32	-4427	278	871	G189	-5586	413
822	S31	-4446	413	872	G187	-5605	278
823	S30	-4465	278	873	G185	-5624	413
824	S29	-4484	413	874	G183	-5643	278
825	S28	-4503	278	875	G181	-5662	413
826	S27	-4522	413	876	G179	-5681	278
827	S26	-4541	278	877	G177	-5700	413
828	S25	-4560	413	878	G175	-5719	278
829	S24	-4579	278	879	G173	-5738	413
830	S23	-4598	413	880	G171	-5757	278
831	S22	-4617	278	881	G169	-5776	413
832	S21	-4636	413	882	G167	-5795	278
833	S20	-4655	278	883	G165	-5814	413
834	S19	-4674	413	884	G163	-5833	278
835	S18	-4693	278	885	G161	-5852	413
836	S17	-4712	413	886	G159	-5871	278
837	S16	-4731	278	887	G157	-5890	413
838	S15	-4750	413	888	G155	-5909	278
839	S14	-4769	278	889	G153	-5928	413
840	S13	-4788	413	890	G151	-5947	278
841	S12	-4807	278	891	G149	-5966	413
842	S11	-4826	413	892	G147	-5985	278
843	S10	-4845	278	893	G145	-6004	413
844	S9	-4864	413	894	G143	-6023	278
845	S8	-4883	278	895	G141	-6042	413
846	S7	-4902	413	896	G139	-6061	278
847	S6	-4921	278	897	G137	-6080	413
848	S5	-4940	413	898	G135	-6099	278
849	S4	-4959	278	899	G133	-6118	413
850	S3	-4978	413	900	G131	-6137	278

R61503U PAD Coordinates (No.10) (Unit: μm) 2006.6.8 rev0.0

pad No	pad name	X	Y
901	G129	-6156	413
902	G127	-6175	278
903	G125	-6194	413
904	G123	-6213	278
905	G121	-6232	413
906	G119	-6251	278
907	G117	-6270	413
908	G115	-6289	278
909	G113	-6308	413
910	G111	-6327	278
911	G109	-6346	413
912	G107	-6365	278
913	G105	-6384	413
914	G103	-6403	278
915	G101	-6422	413
916	G99	-6441	278
917	G97	-6460	413
918	G95	-6479	278
919	G93	-6498	413
920	G91	-6517	278
921	G89	-6536	413
922	G87	-6555	278
923	G85	-6574	413
924	G83	-6593	278
925	G81	-6612	413
926	G79	-6631	278
927	G77	-6650	413
928	G75	-6669	278
929	G73	-6688	413
930	G71	-6707	278
931	G69	-6726	413
932	G67	-6745	278
933	G65	-6764	413
934	G63	-6783	278
935	G61	-6802	413
936	G59	-6821	278
937	G57	-6840	413
938	G55	-6859	278
939	G53	-6878	413
940	G51	-6897	278
941	G49	-6916	413
942	G47	-6935	278
943	G45	-6954	413
944	G43	-6973	278
945	G41	-6992	413
946	G39	-7011	278
947	G37	-7030	413
948	G35	-7049	278
949	G33	-7068	413
950	G31	-7087	278

pad No	pad name	X	Y
951	G29	-7106	413
952	G27	-7125	278
953	G25	-7144	413
954	G23	-7163	278
955	G21	-7182	413
956	G19	-7201	278
957	G17	-7220	413
958	G15	-7239	278
959	G13	-7258	413
960	G11	-7277	278
961	G9	-7296	413
962	G7	-7315	278
963	G5	-7334	413
964	G3	-7353	278
965	G1	-7372	413
966	VGLDMY4	-7391	278
967	DUMMY7	-7410	413
968	DUMMY8	-7429	278

Alignment mark		X	Y
Cross	(1-a)	-7465	-400
	(1-b)	7465	-400
BUMP	(2-a)	-7500	-293
	(2-b)	7500	-293

Bump Size

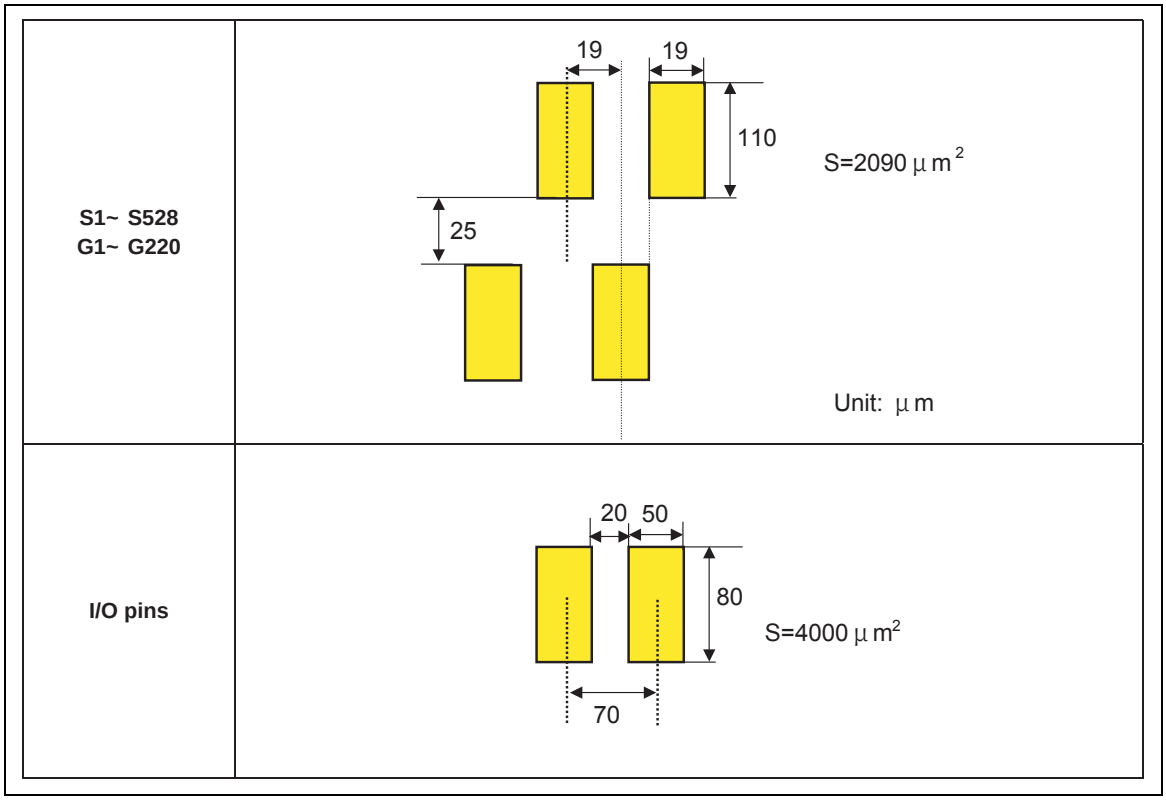


Figure 3

Block Function

1. System Interface

The R61503U supports the following system interfaces: 80-system high-speed interface via 8-, 9-, 16-, 18-bit parallel ports and clock synchronous serial interface. The interface is selected by setting the IM3-0 pins.

The R61503U has 16-bit index register (IR), 18-bit write-data register (WDR), and 18-bit read-data register (RDR). The IR is the register to store index information from control register and the internal GRAM. The WDR is the register to temporarily store the data to be written to the internal GRAM. The RDR is the register to temporarily store the data read from the GRAM. The data from the MPU to be written to the internal GRAM is first written to the WDR and then automatically written to the internal GRAM in internal operation. The data is read via the RDR from the internal GRAM. Therefore, invalid data is sent to the data bus when the first read operation from the internal GRAM is performed. Valid data is read out when the second and subsequent read operations are performed.

The instruction execution time except starting oscillation takes 0 clock cycle and instructions can be written consecutively.

Table 9 Register Selection (80-system 8/9/16/18-bit Parallel Interface)

WR*	RD*	RS	Function
0	1	0	Write index to IR
1	0	0	Read internal status
0	1	1	Write to control register/internal GRAM via WDR
1	0	1	Read from the internal GRAM via RDR

Table 10 Register Selection (clock synchronous serial interface)

Start byte		
R/W	RS	Function
0	0	Write index to IR
1	0	Read internal status
0	1	Write to control register/internal GRAM via WDR
1	1	Read from the internal GRAM via RDR

2. External Display Interface (RGB, VSYNC interfaces)

The R61503U supports RGB interface and VSYNC interface as the moving picture display interface (external display interface). When RGB interface is selected, the display operation is synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface operation, data (DB17-0) is written in synchronization with these signals according to the polarity of the enable signal (ENABLE) to prevent flicker on display while rewriting display data.

In VSYNC interface operation, the display operation is synchronized with the internal clock and VSYNC signal, which is used for frame synchronization. The display data is written to the internal GRAM via system interface but there are restrictions in setting the speed and the method to write data to the internal RAM. For details, see the "External Display Interface" section.

The R61503U allows switching between the external display interface and the system interface by instruction so that the optimal interface is selected for the kind of picture on the panel (still and/or moving picture). The R61503U writes the display data to the internal GRAM to enable transferring data only when the frame data is updated, which contributes to the reduction of data to be transferred from the system and saving power required for the moving picture display.

3. Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the address setting instruction is written in the IR, the address information is sent from the IR to the AC. When the data is written to the internal GRAM, the AC is automatically incremented (plus one) or decremented (minus one). The window address function enables writing data only within the rectangular area specified in GRAM by setting.

4. Graphics RAM (GRAM)

GRAM is graphics RAM, which can store a maximum 87,120-byte (176RGB x 220 (dots) x 18(bits)/8) bit pattern data using 18 bits per pixel.

5. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal drive voltage according to the grayscale data in the γ-correction registers to enable a maximum 262k-color display.

6. Timing Generator

The timing generator generates timing signals to operate internal circuits such as GRAM. The R61503U generates timing signals for display operation such as the RAM read operation and for internal operation such as RAM access from MPU and outputs them separately to avoid mutual interference. Also FLM is generated internally and output from the timing generator.

7. Oscillator (OSC)

The R61503U generates the RC oscillation clock signal by connecting an external oscillation resistor between the OSC1 and OSC2 pins. The oscillation frequency can be changed by changing the resistance of the external resistor. Adjust the oscillation frequency according to operating voltage and frame frequency. In deep standby mode, RC oscillation is halted to reduce power consumption. For details, see “Oscillator”.

8. Liquid crystal driver Circuit

The liquid crystal driver circuit of the R61503U consists of 528-channel source driver (S1 ~ S528) and 220-channel gate driver (G1 ~ G220). The display pattern data is latched when 528 bits of data are input. The latched data control the source driver and generates liquid crystal drive waveform. The shift direction of 528-bit source output from the source driver is determined by instruction (SS bit). The shift direction of gate output from the gate driver can be changed by setting the GS bit. The gate pin assignment can be changed by setting the SM bit. Sets SM and GS bits to select the optimal scan mode for the module.

9. Internal logic power supply regulator

The internal logic power supply regulator generates internal logic power supply VDD.

10. Liquid crystal drive power supply circuit

The liquid crystal drive power supply circuit generates the voltage levels to drive liquid crystal, VREG1OUT, DDVDH, VGH, VGL, VCL, and Vcom.

11. NV memory

8-bit user identification code and 6-bit VcomH setting instruction are written in NV memory. Changing VcomH setting instruction is allowed only once.

GRAM Address MAP

Relation between GRAM addresses and positions on the screen (SS= "0", BGR= "0")

Table 11

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			.....	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G220	"0000"H			"0001"H			"0002"H			"0003"H			.....	"00AC"H			"00AD"H			"00AE"H			"00AF"H		
G2	G219	"0100"H			"0101"H			"0102"H			"0103"H			.....	"01AC"H			"01AD"H			"01AE"H			"01AF"H		
G3	G218	"0200"H			"0201"H			"0202"H			"0203"H			.....	"02AC"H			"02AD"H			"02AE"H			"02AF"H		
G4	G217	"0300"H			"0301"H			"0302"H			"0303"H			.....	"03AC"H			"03AD"H			"03AE"H			"03AF"H		
G5	G216	"0400"H			"0401"H			"0402"H			"0403"H			.....	"04AC"H			"04AD"H			"04AE"H			"04AF"H		
G6	G215	"0500"H			"0501"H			"0502"H			"0503"H			.....	"05AC"H			"05AD"H			"05AE"H			"05AF"H		
G7	G214	"0600"H			"0601"H			"0602"H			"0603"H			.....	"06AC"H			"06AD"H			"06AE"H			"06AF"H		
G8	G213	"0700"H			"0701"H			"0702"H			"0703"H			.....	"07AC"H			"07AD"H			"07AE"H			"07AF"H		
G9	G212	"0800"H			"0801"H			"0802"H			"0803"H			.....	"08AC"H			"08AD"H			"08AE"H			"08AF"H		
G10	G211	"0900"H			"0901"H			"0902"H			"0903"H			.....	"09AC"H			"09AD"H			"09AE"H			"09AF"H		
G11	G210	"0A00"H			"0A01"H			"0A02"H			"0A03"H			.....	"0AAC"H			"0AAD"H			"0AAE"H			"0AAF"H		
G12	G209	"0B00"H			"0B01"H			"0B02"H			"0B03"H			.....	"0BAC"H			"0BAD"H			"0BAE"H			"0BAF"H		
G13	G208	"0C00"H			"0C01"H			"0C02"H			"0C03"H			.....	"0CAC"H			"0CAD"H			"0CAE"H			"0CAF"H		
G14	G207	"0D00"H			"0D01"H			"0D02"H			"0D03"H			.....	"0DAC"H			"0DAD"H			"0DAE"H			"0DAF"H		
G15	G206	"0E00"H			"0E01"H			"0E02"H			"0E03"H			.....	"0EAC"H			"0EAD"H			"0EAE"H			"0EAF"H		
G16	G205	"0F00"H			"0F01"H			"0F02"H			"0F03"H			.....	"0FAC"H			"0FAD"H			"0FAE"H			"0FAF"H		
G17	G204	"1000"H			"1001"H			"1002"H			"1003"H			.....	"10AC"H			"10AD"H			"10AE"H			"10AF"H		
G18	G203	"1100"H			"1101"H			"1102"H			"1103"H			.....	"11AC"H			"11AD"H			"11AE"H			"11AF"H		
G19	G202	"1200"H			"1201"H			"1202"H			"1203"H			.....	"12AC"H			"12AD"H			"12AE"H			"12AF"H		
G20	G201	"1300"H			"1301"H			"1302"H			"1303"H			.....	"13AC"H			"13AD"H			"13AE"H			"13AF"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G213	G8	"D400"H			"D401"H			"D402"H			"D403"H			.....	"D4AC"H			"D4AD"H			"D4AE"H			"D4AF"H		
G214	G7	"D500"H			"D501"H			"D502"H			"D503"H			.....	"D5AC"H			"D5AD"H			"D5AE"H			"D5AF"H		
G215	G6	"D600"H			"D601"H			"D602"H			"D603"H			.....	"D6AC"H			"D6AD"H			"D6AE"H			"D6AF"H		
G216	G5	"D700"H			"D701"H			"D702"H			"D703"H			.....	"D7AC"H			"D7AD"H			"D7AE"H			"D7AF"H		
G217	G4	"D800"H			"D801"H			"D802"H			"D803"H			.....	"D8AC"H			"D8AD"H			"D8AE"H			"D8AF"H		
G218	G3	"D900"H			"D901"H			"D902"H			"D903"H			.....	"D9AC"H			"D9AD"H			"D9AE"H			"D9AF"H		
G219	G2	"DA00"H			"DA01"H			"DA02"H			"DA03"H			.....	"DAAC"H			"DAAD"H			"DAAE"H			"DAAF"H		
G220	G1	"DB00"H			"DB01"H			"DB02"H			"DB03"H			.....	"DBAC"H			"DBAD"H			"DBAE"H			"DBAF"H		

Relation between GRAM data and Display data (SS= "0", BGR= "0")

The following are the interface formats of the R61503U, showing the relationship between the data written in the GRAM and the display data (one pixel) in respective interface operations.

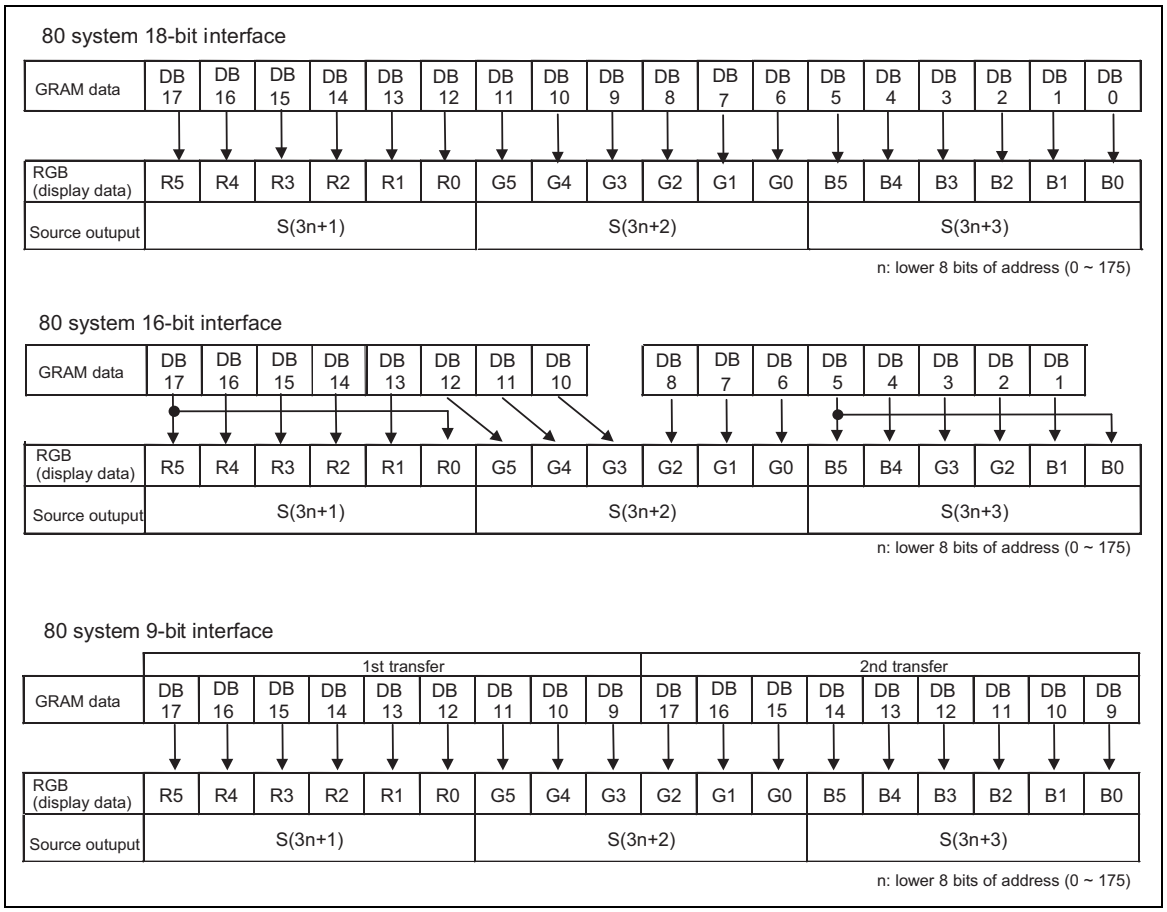


Figure 4 80-system interface (SS = "0", BGR = "0")

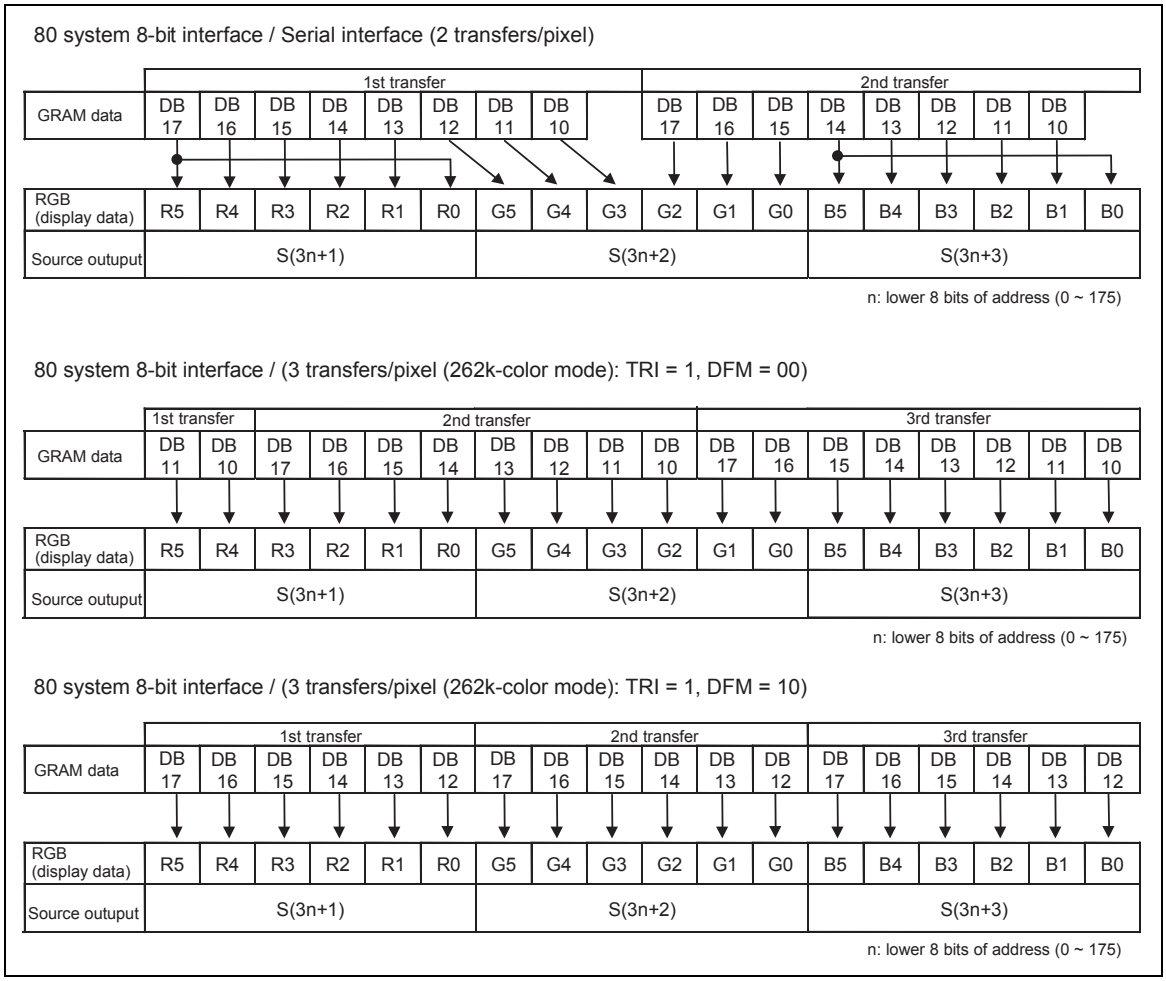


Figure 5 80-system interface (SS = "0", BGR = "0")

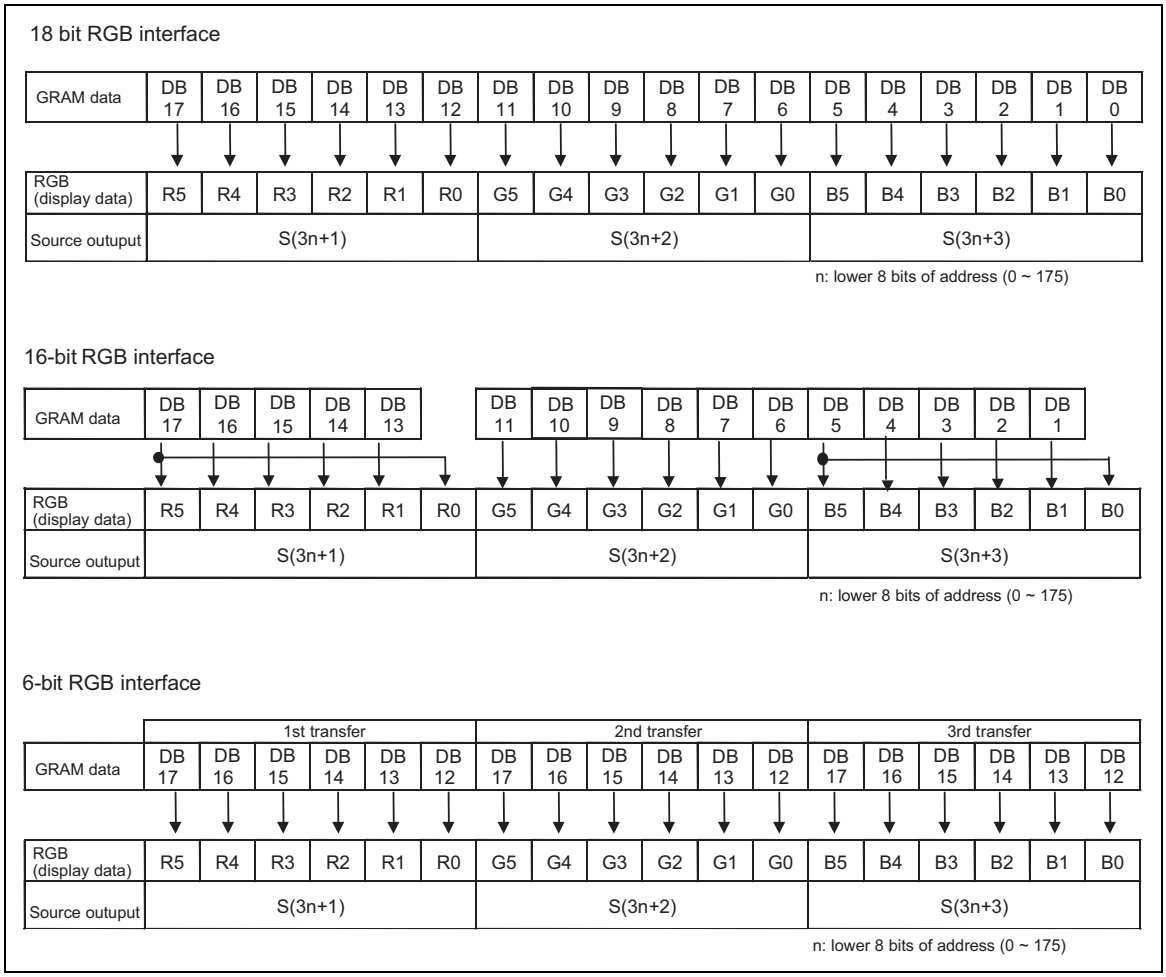


Figure 6 RGB interface (SS = "0", BGR = "0")

Relation between GRAM address and position on the screen (SS= "1", BGR= "1")

Table 12

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			.....	DB17-0			DB17-0			DB17-0			DB17-0		
G1	G220	"00AF"H			"00AE"H			"00AD"H			"00AC"H			.....	"0003"H			"0002"H			"0001"H			"0000"H		
G2	G219	"01AF"H			"01AE"H			"01AD"H			"01AC"H			.....	"0103"H			"0102"H			"0101"H			"0100"H		
G3	G218	"02AF"H			"02AE"H			"02AD"H			"02AC"H			.....	"0203"H			"0202"H			"0201"H			"0200"H		
G4	G217	"03AF"H			"03AE"H			"03AD"H			"03AC"H			.....	"0303"H			"0302"H			"0301"H			"0300"H		
G5	G216	"04AF"H			"04AE"H			"04AD"H			"04AC"H			.....	"0403"H			"0402"H			"0401"H			"0400"H		
G6	G215	"05AF"H			"05AE"H			"05AD"H			"05AC"H			.....	"0503"H			"0502"H			"0501"H			"0500"H		
G7	G214	"06AF"H			"06AE"H			"06AD"H			"06AC"H			.....	"0603"H			"0602"H			"0601"H			"0600"H		
G8	G213	"07AF"H			"07AE"H			"07AD"H			"07AC"H			.....	"0703"H			"0702"H			"0701"H			"0700"H		
G9	G212	"08AF"H			"08AE"H			"08AD"H			"08AC"H			.....	"0803"H			"0802"H			"0801"H			"0800"H		
G10	G211	"09AF"H			"09AE"H			"09AD"H			"09AC"H			.....	"0903"H			"0902"H			"0901"H			"0900"H		
G11	G210	"0AAF"H			"0AAE"H			"0AAD"H			"0AAC"H			.....	"0A03"H			"0A02"H			"0A01"H			"0A00"H		
G12	G209	"0BAF"H			"0BAE"H			"0BAD"H			"0BAC"H			.....	"0B03"H			"0B02"H			"0B01"H			"0B00"H		
G13	G208	"0CAF"H			"0CAE"H			"0CAD"H			"0CAC"H			.....	"0C03"H			"0C02"H			"0C01"H			"0C00"H		
G14	G207	"0DAF"H			"0DAE"H			"0DAD"H			"0DAC"H			.....	"0D03"H			"0D02"H			"0D01"H			"0D00"H		
G15	G206	"0EAF"H			"0EAE"H			"0EAD"H			"0EAC"H			.....	"0E03"H			"0E02"H			"0E01"H			"0E00"H		
G16	G205	"0FAF"H			"0FAE"H			"0FAD"H			"0FAC"H			.....	"0F03"H			"0F02"H			"0F01"H			"0F00"H		
G17	G204	"10AF"H			"10AE"H			"10AD"H			"10AC"H			.....	"1003"H			"1002"H			"1001"H			"1000"H		
G18	G203	"11AF"H			"11AE"H			"11AD"H			"11AC"H			.....	"1103"H			"1102"H			"1101"H			"1100"H		
G19	G202	"12AF"H			"12AE"H			"12AD"H			"12AC"H			.....	"1203"H			"1202"H			"1201"H			"1200"H		
G20	G201	"13AF"H			"13AE"H			"13AD"H			"13AC"H			.....	"1303"H			"1302"H			"1301"H			"1300"H		
:	:	:			:			:			:				:			:			:			:		
:	:	:			:			:			:				:			:			:			:		
G213	G8	"D4AF"H			"D4AE"H			"D4AD"H			"D4AC"H			.....	"D403"H			"D402"H			"D401"H			"D400"H		
G214	G7	"D5AF"H			"D5AE"H			"D5AD"H			"D5AC"H			.....	"D503"H			"D502"H			"D501"H			"D500"H		
G215	G6	"D6AF"H			"D6AE"H			"D6AD"H			"D6AC"H			.....	"D603"H			"D602"H			"D601"H			"D600"H		
G216	G5	"D7AF"H			"D7AE"H			"D7AD"H			"D7AC"H			.....	"D703"H			"D702"H			"D701"H			"D700"H		
G217	G4	"D8AF"H			"D8AE"H			"D8AD"H			"D8AC"H			.....	"D803"H			"D802"H			"D801"H			"D800"H		
G218	G3	"D9AF"H			"D9AE"H			"D9AD"H			"D9AC"H			.....	"D903"H			"D902"H			"D901"H			"D900"H		
G219	G2	"DAAF"H			"DAAE"H			"DAAD"H			"DAAC"H			.....	"DA03"H			"DA02"H			"DA01"H			"DA00"H		
G220	G1	"DBAF"H			"DBAE"H			"DBAD"H			"DBAC"H			.....	"DB03"H			"DB02"H			"DB01"H			"DB00"H		

Relation between GRAM data and Display data (SS= "1", BGR= "1")

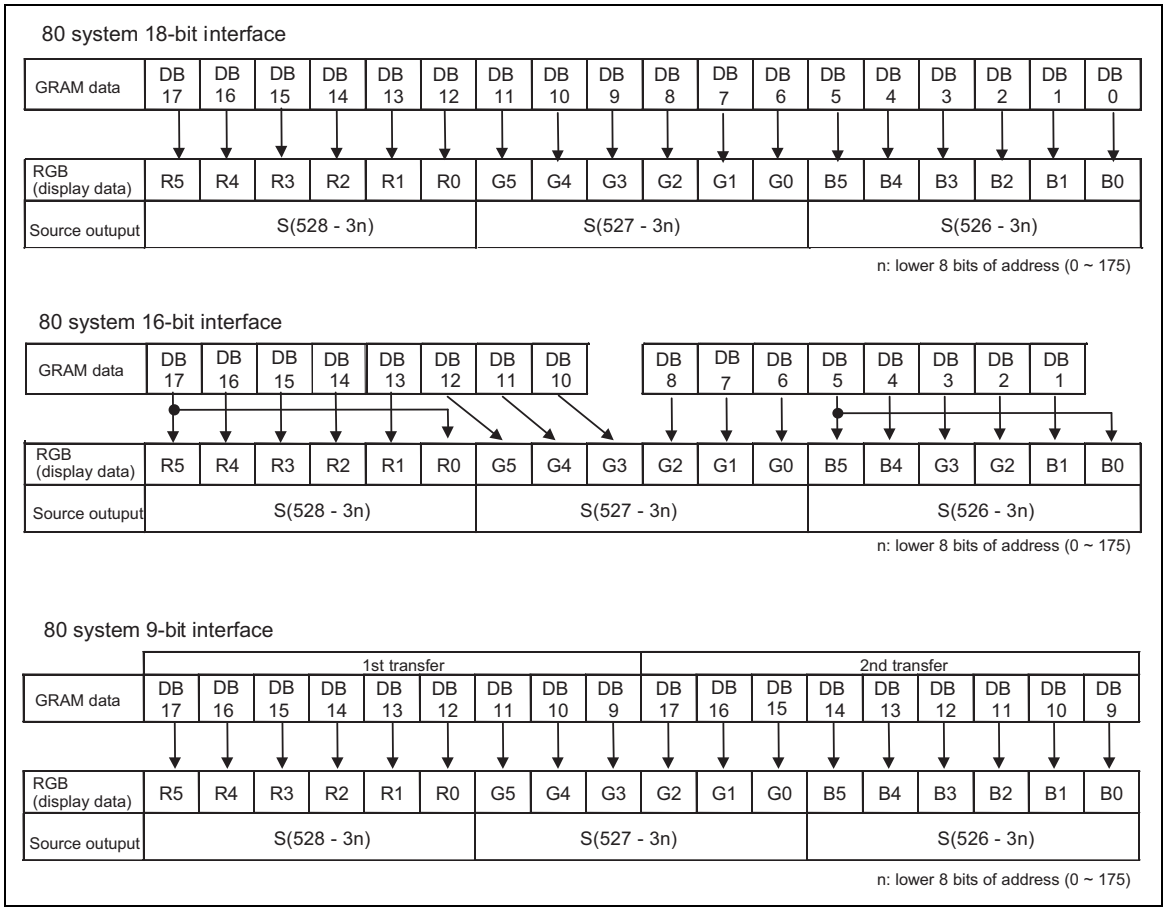


Figure 7 80-system interface (SS = "1", BGR = "1")

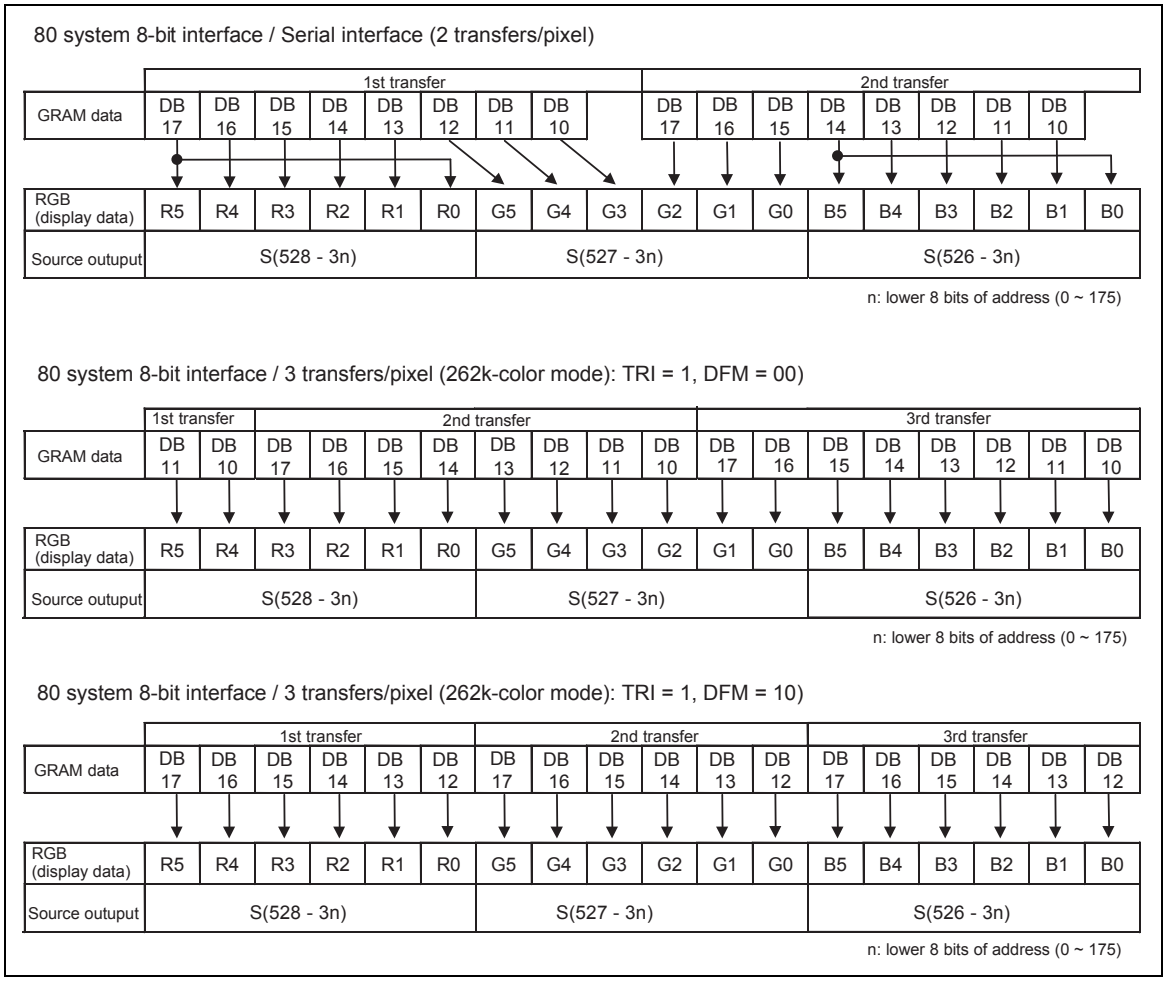


Figure 8 80-system interface (SS = "1", BGR = "1")

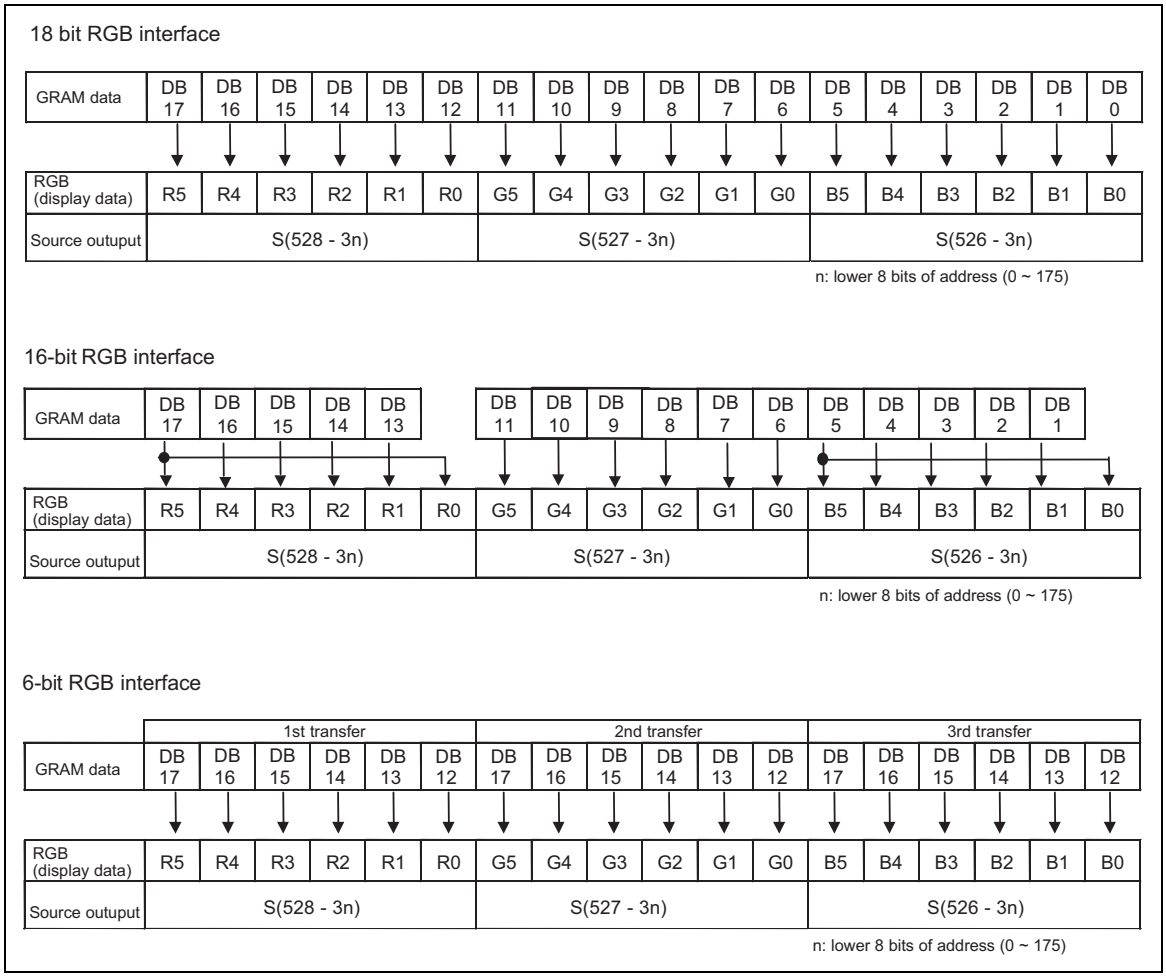


Figure 9 RGB interface (SS = “1”, BGR = “1”)

Instruction

The R61503U adopts 18-bit bus architecture to interface to high-performance microcomputer. The R61503U starts internal processing when the control information sent via 18-, 16-, 9-, 8-bit ports is stored in the instruction register (IR) and the data register (DR). Since the internal operation of the R61503U is controlled by the signals sent from the microcomputer, register selection signal (RS), read/write signal (R/W), and internal 16-bit data bus signals (IB15 to IB0) are called instruction. The R61503U accesses the internal GRAM in units of 18 bits. The instructions of the R61503U are categorized into the following 8 groups.

1. Index specification
2. Status Read
3. Display control
4. Power management control
5. GRAM address setting
6. Transfer data to/from the internal GRAM
7. γ-correction
8. NV memory control

Normally, the instruction to write data in the GRAM is used the most often. In order to minimize the data transfer and lessen the programming load on the microcomputer, the R61503U rewrites data only within the window address area and updates internal GRAM address in the address counter automatically as it writes data in the internal GRAM. The R61503U writes instruction consecutively by executing the instruction within the cycle when it is written (instruction execution time: 0 cycle).

As the following figure shows, the data bus used to transfer 16 instruction bits (IB[15:0]) is different according to the interface format. Make sure to transfer the instruction bits according to the format of the selected interface.

Instruction data format

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface as shown below.

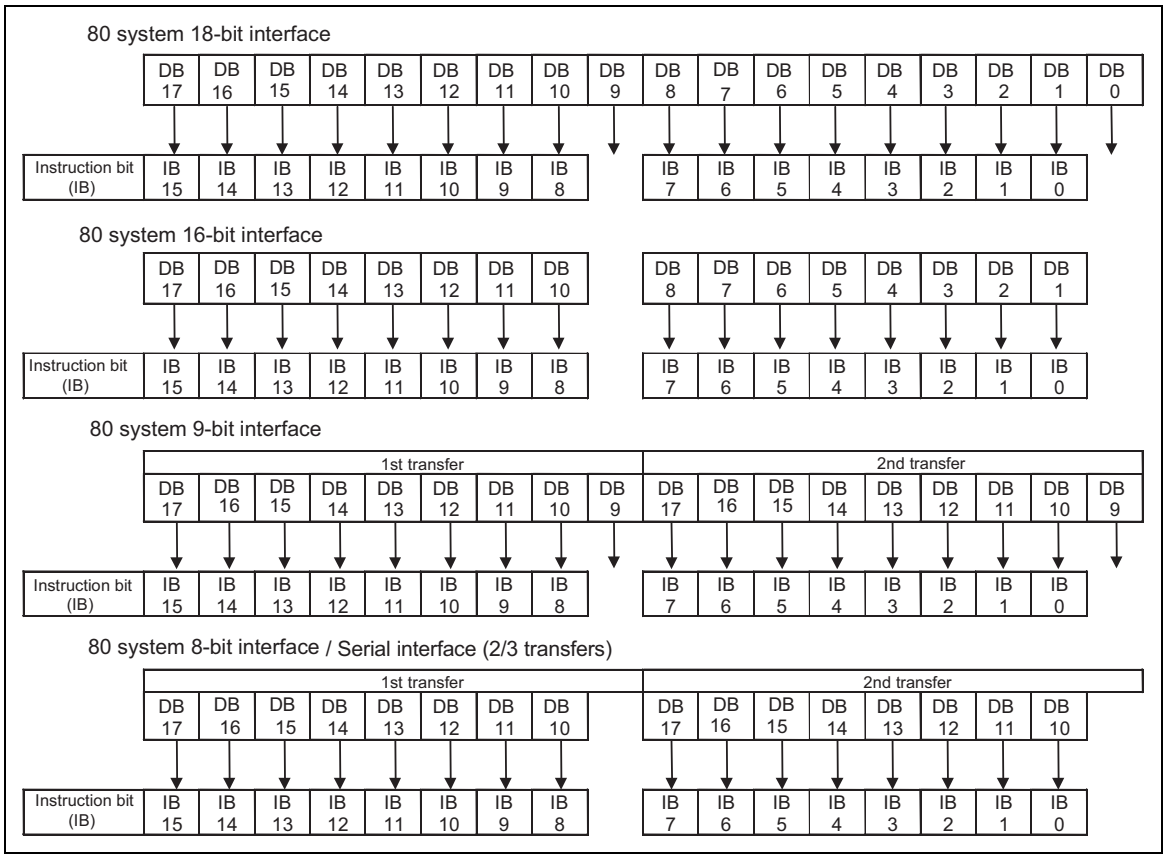


Figure 10 Instruction format

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface (see Figure 10 Instruction format).

Index specification/Status read/Display control instructions

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register represents the index of the control register to be accessed (R00h ~ RFFh) and for RAM control using binary numbers from "0000_0000" to "1111_1111". The access to a register and instruction bits in it is prohibited unless the index is specified in the index register.

Status read (SR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	0	0	0	0	0	0	0	0	L7	L6	L5	L4	L3	L2	L1	L0

The internal status of the R61503U can be read out from the SR register.

L[7:0]: represents the line where the R61503U drives liquid crystal.

Start Oscillation (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	1	0	1	0	1	0	0	0	0	0	0	1	1

The start oscillation instruction starts the oscillator from a halt in standby mode. After executing this instruction, wait at least 10 ms to stabilize the oscillator before issuing next instruction.

The device code "1503"H is read out when reading out this register forcibly.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Sets the shift direction of output from the source driver.

When SS = "0", the source driver output shift from S1 to S528.
When SS = "1", the source driver output shift from S528 to S1.

The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S528.

When SS = "0" and BGR = "0", RGB dots are assigned one to one from S1 to S528.
When SS = "1" and BGR = "1", RGB dots are assigned one to one from S528 to S1.

When changing the SS and BGR bits, RAM data must be rewritten.

SM: Sets the gate driver pin arrangement in combination with the GS bit (R70h) to select the optimal scan mode for the module. See " Scan mode setting".

LCD Driving Wave Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	1	B/C	EOR	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

EOR: By setting EOR = "1", the polarity of C pattern waveform (one-line inversion waveform) is inverted according to the result of EOR (exclusive OR) between the odd/even-number frame select signal and the one-line inversion signal. Set EOR = 1 when the number of lines to drive liquid crystal is not compatible with one-line inversion waveform. For details, see "one-line inversion AC drive".

B/C: When B/C = "0", the liquid crystal drive signal becomes frame-inversion waveform and inverts the polarity of liquid crystal in every frame cycle. When B/C = "1", liquid crystal drive signal becomes one-line inversion waveform and inverts the polarity of liquid crystal in every line cycle. For details, see "line inversion AC drive".

Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM [1]	DFM [0]	BGR	0	0	HWM	0	0	0	I/D [1]	I/D [0]	AM	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the R61503U writes data in the internal GRAM.

AM = "0", sets the horizontal direction.
AM = "1", sets the vertical direction.

When a window address area is specified in GRAM, the R61503U writes data within the window address area in the direction determined by the I/D1-0, AM settings.

I/D[1:0]: The RAM address is automatically incremented (+1) when I/D = "1" and decremented (-1) when I/D = "0" as the R61503U writes data in the GRAM. The I/D[0] bit sets either increment or decrement of RAM address (AD[7:0]) in horizontal direction. The I/D[1] bit sets either increment or decrement decrement of RAM address (AD[15:8]) in vertical direction. The AM bit sets either horizontal or vertical direction in updating RAM address automatically when writing data in the internal RAM.

HWM: When HWM = "1", the R61503U writes data in the internal GRAM in high speed with low power consumption. In this write operation, the R61503U latches the data in units of horizontal lines of window address area in the line buffer and writes the data line by line at a time in the window address area to minimize the number of RAM access and thereby reduce power consumption.

When HWM = "1", make sure the data is written to the end of the horizontal line within the window address area in each RAM write operation. If not, the RAM write operation in that line becomes a failure.

Note 1: Dummy write operation is not required in the R61503U's high speed write operation.
Note 2: The data in the line buffer is cleared when terminating the RAM write operation in the middle of horizontal line and writing other instruction.
Note 3: When switching from high-speed RAM write operation to index write operation, wait at least 2 normal-mode write cycle periods (t_{cycw}) after writing data in the internal RAM.

BGR: Reverses the order of assigning 18-bit RGB data to the data bus (DB17-0) from RGB to BGR.

When BGR = 0, the order of RGB dots is not reversed when writing data to the GRAM.
When BGR = 1, the order of RGB dots is reversed when writing data to the GRAM.

DFM[1:0]: Sets the interface format when transferring 18-bit data via 80-system 16-/8-bit interface in combination with TRI bit. Make sure to set DFM[1:0] = "00", when not using 16-/8-bit interface. See the figures in the "System interface" section for details on the interface format in RAM write operation.

TRI: Sets the interface format when transferring 18-bit data via 80-system 16-/8-bit interface in combination with DFM[1:0] bits.

In 8-bit interface operation,

TRI =0: 16-bit RAM data is transferred in two transfers via 8-bit interface.
TRI =1: 18-bit RAM data is transferred in three transfers via 8-bit interface.

In 16-bit interface operation,

TRI =0: 16-bit RAM data is transferred in one-transfer via 16-bit interface.
TRI =1: 18-bit RAM data is transferred in two transfers via 16-bit interface.

Make sure to set TRI = “0”, when not using 16-/8-bit interface. Also, set TRI = “0” in read operation.

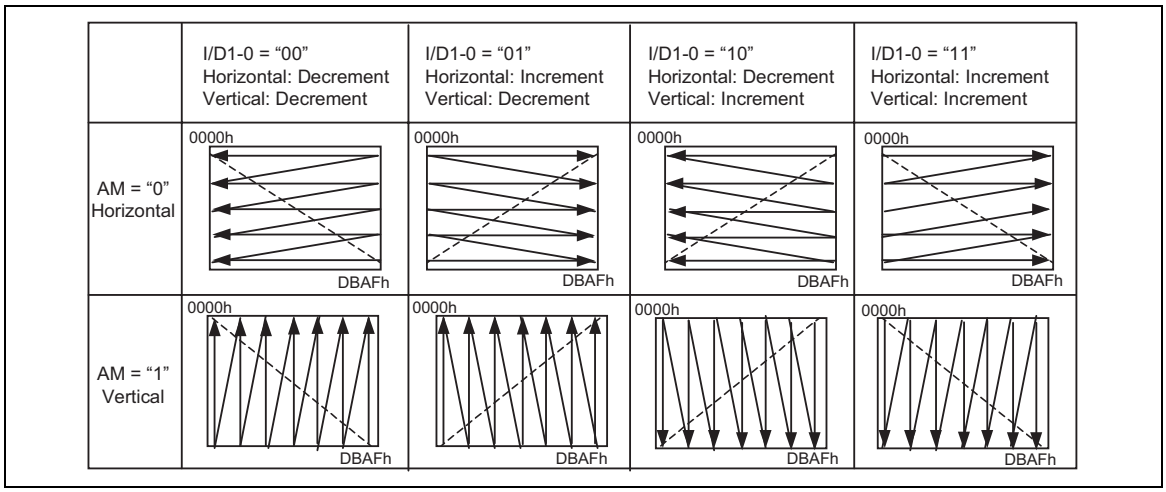
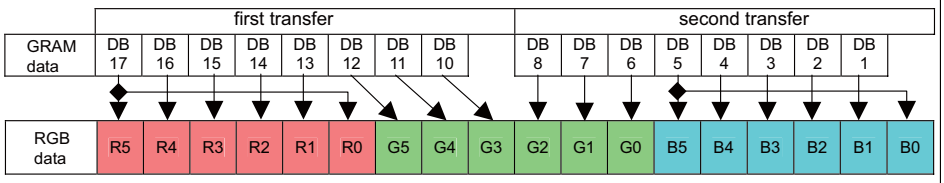
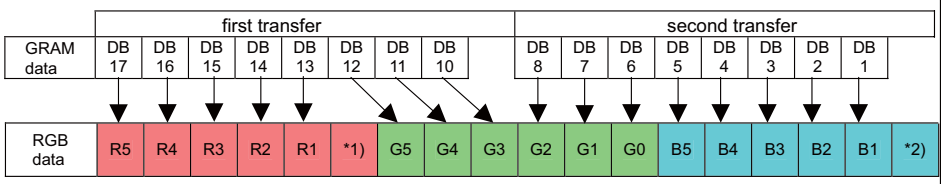


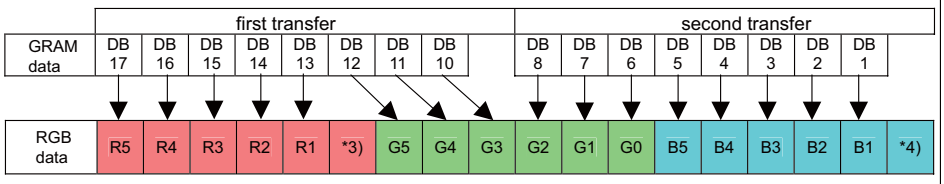
Figure 11 Automatic address transition direction setting (AM, I/D[1:0])

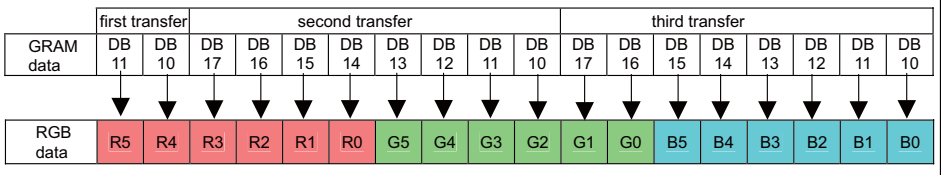
Note: When a window address area is specified in the GRAM, the data is written within the window address area.

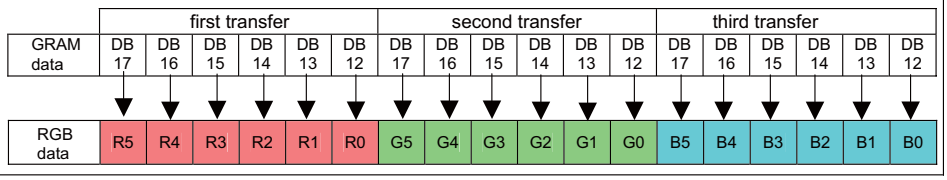
TRI	DFM 1	DFM 0	8- bit interface RAM interface format
0	0	0	80-system 8-bit interface (2 transfers/pixel) 65,536 colors
0	0	1	Setting disabled
0.	1	0	80-system 8-bit interface (2 transfers/pixel) 65,536 colors
0	1	1	80-system 8-bit interface (2 transfers/pixel) 65,536 colors
1	0	*	80-system 8-bit interface (3 transfers/pixel) 262,144 colors
1	1	*	80-system 8-bit interface (3 transfers/pixel) 262,144 colors







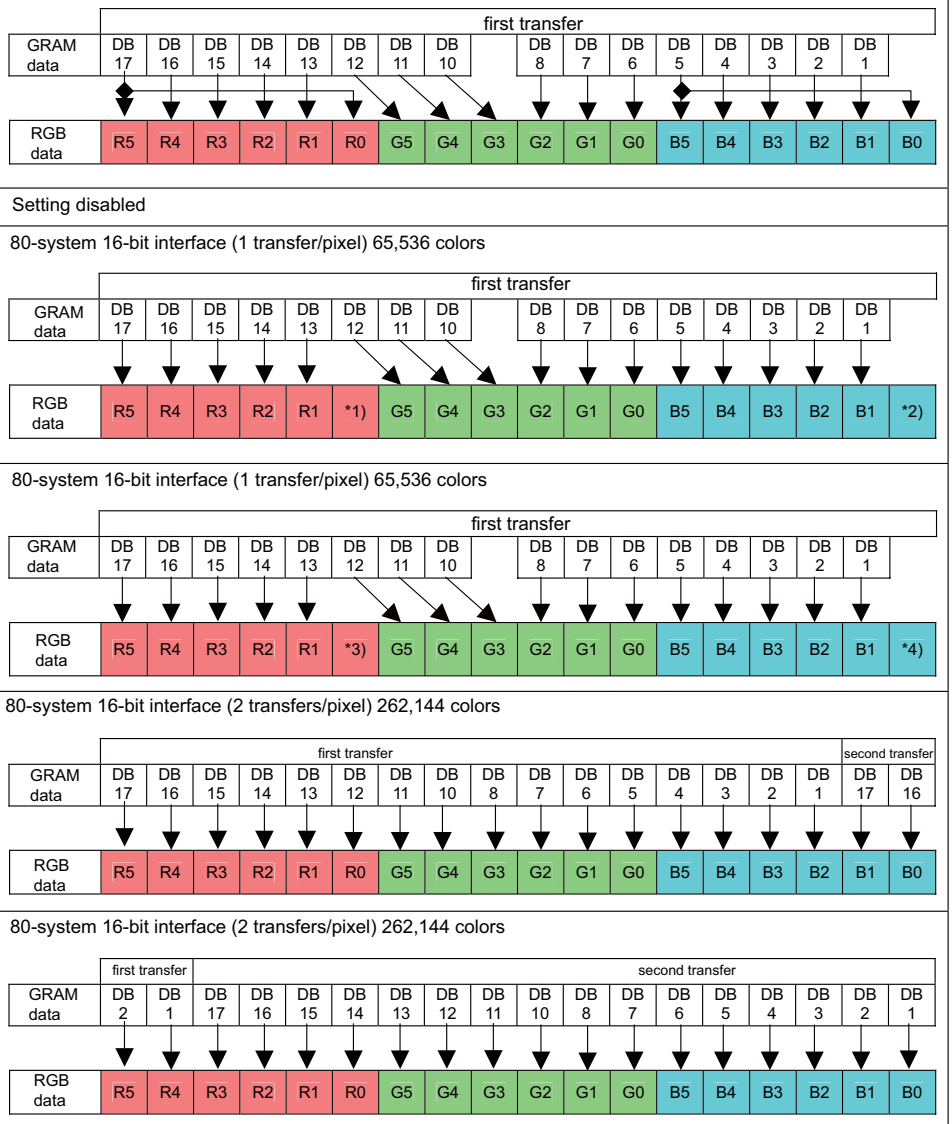




Notes: *1) The logical product of the upper 5 bits (R5 to R1) is inputted to the LSB data.
*2) The logical product of the upper 5 bits (B5 to B1) is inputted to the LSB data.
*3) The logical sum of the upper 5 bits (R5 to R1) is inputted to the LSB data.
*4) The logical sum of the upper 5 bits (B5 to B1) is inputted to the LSB data.

Figure 12 8-bit interface RAM write interface format

TRI	DFM 1	DFM 0	16- bit interface RAM interface format
0	0	0	80-system 16-bit interface (1 transfer/pixel) 65,536 colors
0	0	1	Setting disabled
0.	1	0	80-system 16-bit interface (1 transfer/pixel) 65,536 colors
0	1	1	80-system 16-bit interface (1 transfer/pixel) 65,536 colors
1	0	*	80-system 16-bit interface (2 transfers/pixel) 262,144 colors
1	1	*	80-system 16-bit interface (2 transfers/pixel) 262,144 colors



Notes: *1) The logical product of the upper 5 bits (R5 to R1) is inputted to the LSB data.
*2) The logical product of the upper 5 bits (B5 to B1) is inputted to the LSB data.
*3) The logical sum of the upper 5 bits (R5 to R1) is inputted to the LSB data.
*4) The logical sum of the upper 5 bits (B5 to B1) is inputted to the LSB data.

Figure 13 16-bit interface RAM write interface format

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	PTDE [1]	PTDE [0]	0	0	BASEE	0	0	0	GON	DTE	CL	0	D[1]	D[0]
Default value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D[1:0]: A graphics display is turned on the panel when writing D1 = "1", and is turned off when writing D1 = "0". When writing D1 = "0", the graphics display data is retained in the internal GRAM and the R61503U displays the data when writing D1 = "1". When D1 = "0", i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D1-0 = 2'b01, the R61503U continues internal display operation. When the display is turned off by setting D1-0 = 2'b00, the R61503U's internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF. For details, see "Instruction Setting".

Table 13

D[1:0]	BASEE	PTDE	Source output (S1 ~S528)	R61503U's internal operation
2'h0	*	*	GND	Halt
2'h1	*	*	GND	Operate
2'h2	*	*	Non-lit display level	Operate
2'h3	0	0	Non-lit display level	Operate
	1	0	Base image display	Operate
	0	1	Partial image display	Operate
	1	1	Setting disabled	

Notes: 1. The data write operation from the microcomputer to the internal RAM is performed irrespective of the setting of the D[1:0] bits.
2. The internal state of the R61503U in standby mode become the same as when D[1:0] = 2'b00. This does not mean the D[1:0] setting is changed when setting the standby mode.
3. The non-lit display level from the source output pins is determined by instruction (PTS).

CL: When CL = "1", the R61503U enters the 8-color mode. Follow the 8-color mode setting sequence when setting the 8-color mode. In 8-color mode, the grayscale amplifiers other than those for the V0 and V31 level are halted. If used in combination with frame-inversion liquid crystal drive, the power consumption will be further reduced.

DTE, GON: Controls the output of liquid crystal panel output signal.

Table 14

GON	DTE	Panel output signal
0	0	VGH
0	1	VGH
1	0	VGL
1	1	VGH/VGL

BASEE: Base image display enable bit. When BASEE = "0", no base image is displayed. The R61503U drives liquid crystal at non-lit display level or displays only partial images. When BASEE = "1", the base image is displayed. The D[1:0] setting has precedence over the BASEE setting.

PTDE0: Partial image 1 enable bit
PTDE1: Partial image 2 enable bit

PTDE0/1 = 0: turns off partial image. Only base image is displayed.
PTDE0/1 = 1: turns on partial image. Set the base image display enable bit to 0 (BASEE = 0).

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP [3]	FP [2]	FP [1]	FP [0]	0	0	0	0	BP [3]	BP [2]	BP [1]	BP [0]
Default		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FP [3:0]: Sets the number of lines for a front porch period (a blank period following the end of display).

BP [3:0]: Sets the number of lines for a back porch period (a blank period made before the beginning of display).

Make sure that:

BP + FP ≤ 16 lines
FP ≥ 2 lines
BP ≥ 2 lines

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. A front porch (FP) starts after the number of display lines set by NL bits is displayed. A blank period will start after a front porch (FP) period and it will continue until next VSYNC input is detected.

Note on Setting BP and FP

Set the BP and FP bits as follows in respective operation modes.

Table 15 BP and FP Settings

Internal clock operation mode	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
RGB interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

Table 16 Front and Back Porch period (Line periods)

FP[3:0] BP[3:0]	Front and Back Porch period (Line periods)
4'h0	Setting inhibited
4'h1	Setting inhibited
4'h2	2 lines
4'h3	3 lines
4'h4	4 lines
4'h5	5 lines
4'h6	6 lines
4'h7	7 lines
4'h8	8 lines
4'h9	9 lines
4'hA	10 lines
4'hB	11 lines
4'hC	12 lines
4'hD	13 lines
4'hE	14 lines
4'hF	Setting inhibited

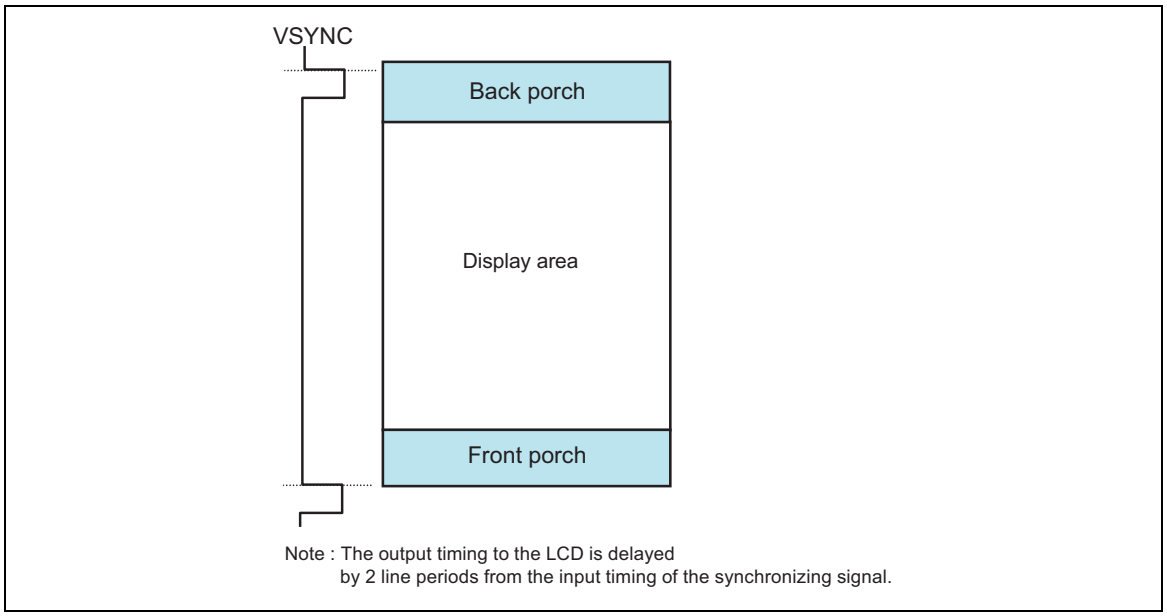


Figure 14 Front, Back Porch periods

Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PTS [2]	PTS [1]	PTS [0]	0	0	PTG [1]	PTG [0]	ISC [3]	ISC [2]	ISC [1]	ISC [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ISC[3:0]: Set the scan cycle when PTG[1:0] selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is inverted in the same timing as the interval scan cycle.

Table 17

ISC[3:0]	Scan cycle	Time for interval when (fFLM) = 60Hz	ISC[3:0]	Scan cycle	Time for interval when (fFLM) = 60Hz
4'h0	0 frame	-	4'h8	17 frames	284ms
4'h1	3 frames	50ms	4'h9	19 frames	317ms
4'h2	5 frames	84ms	4'hA	21 frames	351ms
4'h3	7 frames	117ms	4'hB	23 frames	384ms
4'h4	9 frames	150ms	4'hC	25 frames	418ms
4'h5	11 frames	184ms	4'hD	27 frames	451ms
4'h6	13 frames	217ms	4'hE	29 frames	484ms
4'h7	15 frames	251ms	4'hF	31 frames	518ms

PTG[1:0]: Sets the scan mode in non-display area.

Table 18

PTG[1]	PTG[0]	Scan mode in non-display area	Source output level in non-display area	Vcom output
0	**0**	Normal scan	PTS[2:0] setting	AC output
0	**1**	VGL (fixed)	PTS[2:0] setting	AC output
1	**0**	Interval scan	PTS[2:0] setting	AC output
1	**1**	Setting disabled	-	-

PTS[2:0]: Sets the source output level in non-display area drive period (front/back porch period and blank area between partial displays). When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V31 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

Table 19 Source output level and voltage generating operation in non-display drive period

PTS[2:0]	Source output level		Grayscale amplifier in operation	Step-up clock frequency
	Positive polarity	Negative polarity		
3'h0	V31	V0	V0 to V31	Register setting (DC0, DC1)
3'h1	Setting inhibited	Setting inhibited	-	-
3'h2	GND	GND	V0 to V31	Register setting (DC0, DC1)
3'h3	Hi-Z	Hi-Z	V0 to V31	Register setting (DC0, DC1)
3'h4	V31	V0	V0 and V31	1/2 the frequency set by DC0, DC1
3'h5	Setting inhibited	Setting inhibited	-	-
3'h6	GND	GND	V0 and V31	1/2 the frequency set by DC0, DC1
3'h7	Hi-Z	Hi-Z	V0 and V31	1/2 the frequency set by DC0, DC1

Notes: 1. The power efficiency can be improved by halting grayscale amplifiers and slowing down the step-up clock frequency only in non-display drive period.

2. The gate output level in non-lit display area drive period is determined by PTG[1:0].

External Display Interface Control 1 (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM [1]	DM [0]	0	0	RIM [1]	RIM [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0]: Sets interface format when RGB interface is selected by RM and DM bits. Set RIM[1:0] bits before starting display operation via RGB interface. Do not change the setting while the R61503U performs display operation.

Table 20 RGB interface operation

RIM[1:0]	RGB Interface operation
2'h0	18-bit RGB interface (1 transfer/pixel)
2'h1	16-bit RGB interface (1 transfer/pixel)
2'h2	6-bit RGB interface (3 transfers/pixel)
2'h3	Setting inhibited

Notes: 1: Instruction bits are set via system interface.
2: Transfer the RGB dot data one by one in synchronization with DOTCLK in 6-bit RGB interface operation.

DM[1:0]: Selects the interface for the display operation. The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

Table 21 Display Interface

DM[1:0]	Display Interface
2'h0	Internal clock operations
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	Setting inhibited

RM: Selects the interface for RAM access operation. RAM access is possible only via the interface selected by the RM bit. Set RM = 1 when writing display data via RGB interface. When RM = 0, it is possible to write data via system interface while performing display operation via RGB interface.

Table 22 RAM Access Interface

RM	RAM Access Interface
0	System interface/VSYNC interface
1	RGB interface

The R61503U selects the optimum interface according to the displayed image by setting instruction as follows.

In moving picture display operation via RGB or VSYNC interface, write data in high-speed write mode (HWM = 1) in order to access RAM in high-speed with low power consumption.

Table 23

The state of display	Operation Mode	RAM Access (RM)	Display Operation Mode (DM)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface (2)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Notes: 1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.
3. Do not make changes to the RGB interface operation setting (RIM1-0) while RGB interface is in operation.
4. See the "External Display Interface" section for the sequences when switching from one mode to another.
5. Use high-speed write function (HWM = 1) when writing data via RGB or VSYNC interface.

Internal clock operation

The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. All input via external display interface is disabled in this operation. The internal RAM can be accessed only via system interface.

RGB interface operation (1)

The display operation is synchronized with frame synchronous signal (VSYNC), line synchronous signal (HSYNC), and dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied during the display operation via RGB interface.

The R61503U transfers display data in units of pixels via DB17-0 pins. The display data is stored in the internal RAM. The combined use of high-speed RAM write mode and window address function can minimize the total number of data transfer for moving picture display by transferring only the data to be written in the moving picture RAM area when it is written and enables the R61503U to display a moving picture and the data in other than the moving picture RAM area simultaneously.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the R61503U by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB17-0 pins in accordance with the settings of these periods.

RGB interface operation (2)

This mode enables the R61503U to rewrite RAM data via system interface while using RGB interface for display operation. To rewrite RAM data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first. Then set an address in the RAM address set register and R22h in the index register.

VSYNC interface operation

The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the R61503U to display a moving picture via system interface by writing data in the internal RAM at faster than the calculated minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are restrictions in speed and method of writing RAM data. For details, see the "VSYNC Interface" section.

As external input, only VSYNC signal input is valid in this mode. Other input via external display interface becomes disabled.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) inside the R61503U according to the instruction settings for these periods.

External Display Interface Control 2 (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPL: Sets the signal polarity of the DOTCLK pin.

DPL = "0" The data is input on the rising edge of DOTCLK
DPL = "1" The data is input on the falling edge of DOTCLK

EPL: Sets the signal polarity of the ENABLE pin.

EPL = "0" The data DB17-0 is written when ENABLE = "0". Disable data write operation when ENABLE = "1".
EPL = "1" The data DB17-0 is written when ENABLE = "1". Disable data write operation when ENABLE = "0".

HSPL: Sets the signal polarity of the SYNC pin.

HSPL = "0" Low active
HSPL = "1" High active

VSPL: Sets the signal polarity of the VSYNC pin.

VSPL = "0" Low active
VSPL = "1" High active

Power Control

Power Control 1/2 (R10h/R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	SAP	BT [3]	BT [2]	BT [1]	BT [0]	APE	0	AP [1]	AP [0]	0	DSTB	SLP	STB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	DC1 [2]	DC1 [1]	DC1 [0]	0	DC0 [2]	DC0 [1]	DC0 [0]	0	VC [2]	VC [1]	VC [0]
Default		0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0

Top: R10h, bottom: R11h

STB: When STB = 1, the R61503U enters the standby mode. In standby mode, the R61503U halts RC oscillation and receiving external clock signal to halt the display operation completely. In setting the standby mode, follow the standby mode setting sequence. The R61503U accepts only the following instructions in standby mode. The instruction register setting is retained in standby mode.

1. Exit standby mode (STB = 0)
2. Start oscillation

SLP: When SLP = 1, the R61503U enters the sleep mode. In sleep mode, the internal display operation except RC oscillation is halted to reduce power consumption. No change to the GRAM data and instruction setting is accepted and the GRAM data and the instruction setting are maintained in sleep mode.

DSTB: When DSTB = 1, the R61503U enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not maintained when the R61503U enters the deep standby mode, and they must be reset after exiting deep standby mode.

AP[1:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP1-0 = 2'h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

APE: Liquid crystal power supply enable bit. Set APE = "1" when starting the generation of liquid crystal power supply according to the liquid crystal power supply startup sequence. After starting up the power supply circuit, set APE = "1".

Table 24

APE	Liquid crystal power supply circuit	Grayscale voltage generating circuit
1'h0	Halt	Halt
1'h1	Operate	Operate

BT[3:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

SAP: When SAP = "0", the internal source output circuit is halted (S1-S528 = GND). When SAP = "1", grayscale voltages are output from the source output circuit. Set SAP = "0" when turning on the power supply such as liquid crystal power supply circuit. After starting up the power supply circuit, set SAP = "1".

VC[2:0]: Sets the factor of VciLVL to generate the reference voltages VciOUT, Vci1.

DC0[2:0]: Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC1[2:0]: Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

Table 25 Step-up factor for step-up circuits 1/2

BT[3:0]	DDVDH	VCL	VGH	VGL	Capacitor connection pins
3'h0	VCI1×2 [x 2]	-VCI1	DDVDH×3 [x 6]	-(VCI1+DDVDH×2) [x -5]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'h1				-(DDVDH×2) [x -4]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'h2				-(VCI1+DDVDH) [x -3]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±,
3'h3			VCI1+DDVDH×2 [x 5]	-(VCI1+DDVDH×2) [x -5]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'h4				-(DDVDH×2) [x -4]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'h5				-(VCI1+DDVDH) [x -3]	DDVDH, VGH, VGL, VCL C11±, C13±C21±, C22±
3'h6			DDVDH×2 [x 4]	-(DDVDH×2) [x -4]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'h7				-(VCI1+DDVDH) [x -3]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'h8	Setting disabled				
3'h9	VCI1×2 [x 2]	-VCI1	DDVDH×3 [x 6]	-(VDDVDH) [x -2]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'hA	Setting disabled				
3'hB	Setting disabled				
3'hC	VCI1×2 [x 2]	-VCI1	VCI1+DDVDH×2 [x 5]	-(VDDVDH) [x -2]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'hD	Setting disabled				
3'hE	VCI1×2 [x 2]	-VCI1	DDVDH×2 [x 4]	-(VDDVDH) [x -2]	DDVDH, VGH, VGL, VCL C11±, C13±, C21±, C22±
3'hF	Setting disabled				

Notes: 1. The factors in the brackets show the step-up factors from Vci1.
2. Connect capacitors to the capacitor connection pins when generating DDVDH, VGH, VGL levels.
3. Make sure DDVDH = max. 6.0V, VGH-VGL (amplitude) = max. 28.0V.

Table 26 constant current in operational amplifiers

AP[1:0]	In LCD drive power supply amplifiers	In grayscale voltage amplifiers
2'h0	Halt operational amplifiers and step-up circuits	Halt
2'h1	0.5	0.62
2'h2	0.75	0.71
2'h3	1	1

Note: The values in the table represent the ratios of currents in respective settings to the current when AP[1:0] = 2'h3.

Table 27 operating frequencies of step-up circuits 1/2

DC0[2:0]	Step-up circuit 1 Operating frequency (f_{DCDC1})
3'h0	Fosc / 8
3'h1	fosc / 16
3'h2	fosc / 32
3'h3	fosc / 64
3'h4	fosc / 128
3'h5	Setting disabled
3'h6	Halt the step-up circuit 1
3'h7	Setting disabled

DC1[2:0]	Step-up circuit 2 Operating frequency (f_{DCDC2})
3'h0	fosc / 16
3'h1	fosc / 32
3'h2	fosc / 64
3'h3	fosc / 128
3'h4	fosc / 256
3'h5	Setting disabled
3'h6	Halt the step-up circuit 2
3'h7	Setting disabled

Note: Make sure $f_{DCDC1} \geq f_{DCDC2}$ when setting the operating frequencies of the step-up circuits 1/2.

Table 28 Reference voltage setting

VC[2:0]	VciOUT (reference voltage) Vci1 voltage
3'h0	0.94 x VciLVL
3'h1	0.89 x VciLVL
3'h2	Setting disabled
3'h3	Setting disabled
3'h4	0.76 x VciLVL
3'h5	Setting disabled
3'h6	Setting disabled
3'h7	1.00 x VciLVL

Power Control 3/4 (R12h/R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	VON	0	0	0	VCMR	VREG1R	0	PSON	PON	VRH [3]	VRH [2]	VRH [1]	VRH [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	1	VCOMG	0	0	0	VDV [3]	VDV [2]	VDV [1]	VDV [0]	VCM SEL	0	0	VCM [4]	VCM [3]	VCM [2]	VCM [1]	VCM [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Top: R12h, bottom: R13h

VRH[3:0]: Sets the factor (1.40 ~ 2.10) of VciLVL, the level of which is determined by instruction (VC), to generate the VREG1OUT voltage.

PON: Controls ON/OFF of the VGL output. When setting the PON bit, follow the power supply startup sequence.

PON = "0": Stop the step-up operation to generate VGL.
PON = "1": Start the step-up operation to generate VGL.

PSON: Starts up the internal power supply sequencer. First set PSE = "1" to enable the internal power supply sequencer and then set PSON = 1 to start up the internal power supply sequencer.

VREG1R: Sets VREG1OUT reference electrical potential.

Table 29

VREG1R	VREG1OUT reference electrical potential
0	VciLVL
1	The setting in the reference voltage output electric potential (±2.0%)

VCMR: Selects either external resistor (VcomR) or internal electric volume (VCM) to set the electrical potential of VcomH (Vcom center voltage level).

Table 30

VCMR	VCOMH electrical potential
0	VCOMR (variable resistor)
1	Internal electronic volume

Note: The internal electronic volume is set by instruction (VCM[4:0]).

VON: Controls Vcom output and its output level in combination with the following bit setting.

Table 31

VON	VCOMG	Vcom output level
0	*	GND
1	0	VcomH/GND
1	1	VcomH/VcomL

VCM[4:0]: Selects the internal electronic volume applied to VREG1OUT to set the VcomH electrical potential. Set VCMR = 1 when setting the VcomH electrical potential with internal electronic volume.

VCMSEL: Selects either the setting in the internal register (VCM[4:0]) or the setting written in the internal NV memory (R29h or R2Ah) to set the VcomH level.

VDV[3:0]: Sets the factor applied to VREG1OUT to define the amplitude of Vcom.

Table 32 VREG1OUT

VRH[3:0]	VREG1OUT	
	VREG1R = 0	VREG1R = 1
4'h0	Halt (Hi-Z)	Halt (Hi-z)
4'h1	VciLVL x 1.40	3.5V
4'h2	VciLVL x 1.45	3.625V
4'h3	VciLVL x 1.50	3.75V
4'h4	VciLVL x 1.55	3.875V
4'h5	VciLVL x 1.60	4.0V
4'h6	VciLVL x 1.65	4.125V
4'h7	VciLVL x 1.70	4.25V

VRH[3:0]	VREG1OUT	
	VREG1R = 0	VREG1R = 1
4'h8	VciLVL x 1.75	4.375V
4'h9	VciLVL x 1.80	4.5V
4'hA	VciLVL x 1.85	4.625V
4'hB	VciLVL x 1.90	4.75V
4'hC	VciLVL x 1.95	4.875V
4'hD	VciLVL x 2.00	5.0V
4'hE	VciLVL x 2.05	5.125V
4'hF	VciLVL x 2.10	5.25V

Note: Set VC and VRH so that VREG1OUT becomes equal or less than 3.5 V ~ (DDVDH -5.0)V.

Table 33

VCMSEL	VcomH level setting
0	Enable the setting in R13h (VCM[4:0])
1	Enable the setting in the internal NV memory (R29h or R2Ah)

Table 34 VCM: Internal electronic volume adjustment

VCM[4:0]	VCOMH	VCM[4:0]	VCOMH
5'h00	VREG1OUT x 0.69	5'h10	VREG1OUT x 0.85
5'h01	VREG1OUT x 0.70	5'h11	VREG1OUT x 0.86
5'h02	VREG1OUT x 0.71	5'h12	VREG1OUT x 0.87
5'h03	VREG1OUT x 0.72	5'h13	VREG1OUT x 0.88
5'h04	VREG1OUT x 0.73	5'h14	VREG1OUT x 0.89
5'h05	VREG1OUT x 0.74	5'h15	VREG1OUT x 0.90
5'h06	VREG1OUT x 0.75	5'h16	VREG1OUT x 0.91
5'h07	VREG1OUT x 0.76	5'h17	VREG1OUT x 0.92
5'h08	VREG1OUT x 0.77	5'h18	VREG1OUT x 0.93
5'h09	VREG1OUT x 0.78	5'h19	VREG1OUT x 0.94
5'h0A	VREG1OUT x 0.79	5'h1A	VREG1OUT x 0.95
5'h0B	VREG1OUT x 0.80	5'h1B	VREG1OUT x 0.96
5'h0C	VREG1OUT x 0.81	5'h1C	VREG1OUT x 0.97
5'h0D	VREG1OUT x 0.82	5'h1D	VREG1OUT x 0.98
5'h0E	VREG1OUT x 0.83	5'h1E	VREG1OUT x 0.99
5'h0F	VREG1OUT x 0.84	5'h1F	VREG1OUT x 1.00

Notes 1. Set VcomH from (DDVDH-0.5)V to 2.5V.

2. The VCM[4:0] setting is enabled when VCMR = 1.

Table 35 VDV: VCS (= Vcom) amplitude

VDV[3:0]	VCS (= Vcom) amplitude
4'h00	VREG1OUT x 0.70
4'h01	VREG1OUT x 0.72
4'h02	VREG1OUT x 0.74
4'h03	VREG1OUT x 0.76
4'h04	VREG1OUT x 0.78
4'h05	VREG1OUT x 0.80
4'h06	VREG1OUT x 0.82
4'h07	VREG1OUT x 0.84
4'h08	VREG1OUT x 0.86
4'h09	VREG1OUT x 0.88
4'h0A	VREG1OUT x 0.90
4'h0B	VREG1OUT x 0.92
4'h0C	VREG1OUT x 0.94
4'h0D	VREG1OUT x 0.96
4'h0E	VREG1OUT x 0.98
4'h0F	VREG1OUT x 1.00

Note: Set the Vcom amplitude from 2.5V to (DDVDH-0.5)V.

VCOMG: When VCOMG = 1, the VcomL voltage can be set in the negative range (1.0 ~ Vci+0.5V (max.)). When VCOMG = 0, the amplifiers for the negative voltage are halted to reduce power consumption. When VCOMG = 0, the VDV[3:0] setting is disabled. In this case the Vcom alternating amplitude is determined by the VCM[4:0] setting, which determines the VcomH level. PON must be set to 1 the setting VCOMG = 1 is enabled.

Power Sequence Control 5 (R14h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DC5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DC5: Changes the cycle of base clock for the step-up operation. When setting DC5 = 1, the step-up clock is synchronized with the 1H period, i.e. the step-up clock is reset every 1H period. By changing the setting of DC5 bit, the step-up clock cycles DC0 and DC1 are also changed.

Table 36

DC5	Base clock f_{bc}
0	f_{OSC}
1	f_{OSC}/2, synchronized with the 1H period

Table 37 Operating Frequencies of Step-up Circuits 1/2

DC0[2:0]	Step-up circuit 1 Operating frequency (f_{DCDC1})
3'h0	f_{bc} / 8
3'h1	f_{bc} / 16
3'h2	f_{bc} / 32
3'h3	f_{bc} / 64
3'h4	f_{bc} / 128
3'h5	Setting disabled
3'h6	Halt the step-up circuit 1
3'h7	Setting disabled

DC1[2:0]	Step-up circuit 2 Operating frequency (f_{DCDC2})
3'h0	f_{bc} / 16
3'h1	f_{bc} / 32
3'h2	f_{bc} / 64
3'h3	f_{bc} / 128
3'h4	f_{bc} / 256
3'h5	Setting disabled
3'h6	Halt the step-up circuit 2
3'h7	Setting disabled

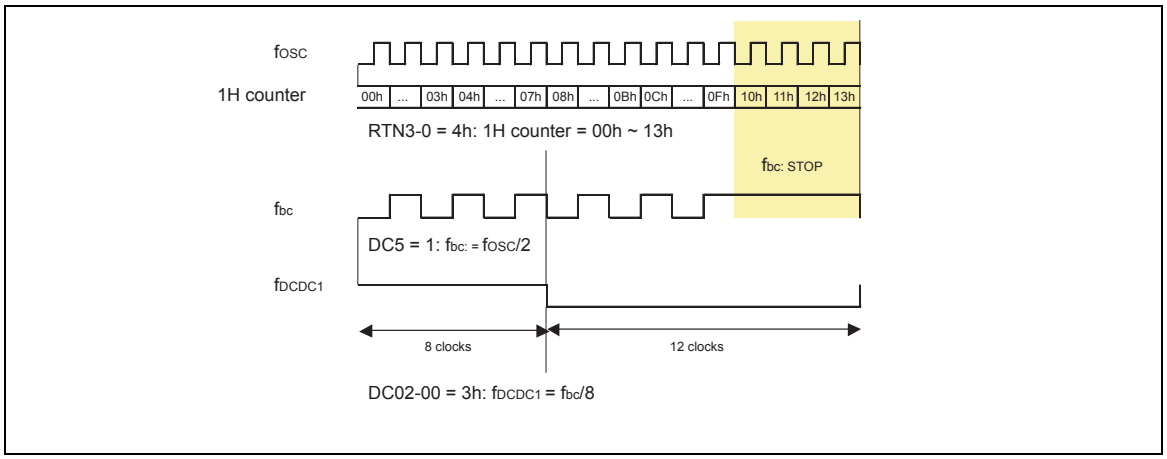


Figure 15

Power Control 6 (R18h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PSE: Power supply startup enable bit. The power supply startup operation is started by setting PSON = 1 when PSE = 1. When the power supply startup operation is completed, the PSE bit is set to "0".

RAM Access Instruction

RAM Address Set Horizontal Address (R20h),
RAM Address Set Vertical Address (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD [7]	AD [6]	AD [5]	AD [4]	AD [3]	AD [2]	AD [1]	AD [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
W	1	0	0	0	0	0	0	0	AD [16]	AD [15]	AD [14]	AD [13]	AD [12]	AD [11]	AD [10]	AD [9]	AD [8]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Top: R20h, Bottom: R21h

AD[16:0]: A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the AM, I/D[1:0] settings as the R61503U writes data to the internal GRAM so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note 1: In RGB interface operation (RM = "1"), the address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

Note 2: In internal clock operation and VSYNC interface operation (RM = "0"), the address AD16-0 is set when executing the instruction.

Table 38 GRAM address range

AD[16:0]	GRAM Setting
17'h00000 ~ 17'h 000AF	Bitmap data for G1
"00100" ~ "001AF"	Bitmap data for G2
"00200" ~ "002AF"	Bitmap data for G3
"00300" ~ "003AF"	Bitmap data for G4
:	:
"0D800" ~ "0D8AF"	Bitmap data for G217
"0D900" ~ "0D9AF"	Bitmap data for G218
"0DA00" ~ "0DAAF"	Bitmap data for G219
"0DB00" ~ "0DBAF"	Bitmap data for G220

Write/Read RAM data

Write Data to GRAM (R22h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	RAM write data WD[17:0] is transferred via different data bus in different interface operation.															

WD[17:0]: The R61503U develops data into 18 bits internally in write operation. The format to develop data into 18 bits is different in different interface operation.

The GRAM data represents the grayscale level. The R61503U automatically updates the address according to AM and I/D[1:0] settings as it writes data in the GRAM. In deep standby mode, GRAM access is disenabled. In 8-/16-bit interface operation, the MSBs of R and B dot are written as the LSBs of respective dot to expand data into 18 bits. In this case, 65,536 colors are available.

Note: When writing data in GRAM via system interface while using the RGB interface, make sure that write operations via two interfaces do not conflict with each other.

Table 39 GRAM data and LCD output level (REV = "0")

GRAM data (RGB)	Selected grayscale	
	Negative	Positive
000000	V0	V31
000001	(V0+V1)/2	(V30+V31)/2
000010	V1	V30
000011	(V1+V2)/2	(V29+V30)/2
000100	V2	V29
000101	(V2+V3)/2	(V28+V29)/2
000110	V3	V28
000111	(V3+V4)/2	(V27+V28)/2
001000	V4	V27
001001	(V4+V5)/2	(V26+V27)/2
001010	V5	V26
001011	(V5+V6)/2	(V25+V26)/2
001100	V6	V25
001101	(V6+V7)/2	(V24+V25)/2
001110	V7	V24
001111	(V7+V8)/2	(V23+V24)/2
010000	V8	V23
010001	(V8+V9)/2	(V22+V23)/2
010010	V9	V22
010011	(V9+V10)/2	(V21+V22)/2
010100	V10	V21
010101	(V10+V11)/2	(V20+V21)/2
010110	V11	V20
010111	(V11+V12)/2	(V19+V20)/2
011000	V12	V19
011001	(V12+V13)/2	(V18+V19)/2
011010	V13	V18
011011	(V13+V14)/2	(V17+V18)/2
011100	V14	V17
011101	(V14+V15)/2	(V16+V17)/2
011110	V15	V16
011111	(V15+V16)/2	(V15+V16)/2

GRAM data (RGB)	Selected grayscale	
	Negative	Positive
100000	V16	V15
100001	(V16+V17)/2	(V14+V15)/2
100010	V17	V14
100011	(V17+V18)/2	(V13+V14)/2
100100	V18	V13
100101	(V18+V19)/2	(V12+V13)/2
100110	V19	V12
100111	(V19+V20)/2	(V11+V12)/2
101000	V20	V11
101001	(V20+V21)/2	(V10+V11)/2
101010	V21	V10
101011	(V21+V22)/2	(V9+V10)/2
101100	V22	V9
101101	(V22+V23)/2	(V8+V9)/2
101110	V23	V8
101111	(V23+V24)/2	(V7+V8)/2
110000	V24	V7
110001	(V24+V25)/2	(V6+V7)/2
110010	V25	V6
110011	(V25+V26)/2	(V5+V6)/2
110100	V26	V5
110101	(V26+V27)/2	(V4+V5)/2
110110	V27	V4
110111	(V27+V28)/2	(V3+V4)/2
111000	V28	V3
111001	(V28+V29)/2	(V2+V3)/2
111010	V29	V2
111011	(V29+V30)/2	(V1+V2)/2
111100	V30	V1
111101	(V30+V31)/2	(V0+V1)/2
111110	(V30+2xV31)/3	(2xV0+V1)/3
111111	V31	V0

RAM Access via RGB interface and System interface

The R61503U writes all data in GRAM in RGB interface operation in order to rewrite the data only within the moving picture area and transfer only the data to be written over the moving picture area. The power consumption required for moving picture display can be reduced and RAM data update can be done in short period by specifying window address area and enabling high-speed write function. The R61503U also allows writing the display data in other than the moving picture area in GRAM via system interface while not updating the moving picture frame.

The R61503U allows RAM access via system interface in RGB interface operation. In RGB interface operation, the data is written to the internal RAM in synchronization with DOTCLK while ENABLE is "Low". When writing data to the RAM via system interface, set ENABLE "High" to stop writing data via RGB interface. When switching to RAM access via RGB interface from RAM access via system interface, make sure to wait for read/write bus cycle time. If there is a conflict between RAM accesses via two interfaces, there is no guarantee that the data is written in the RAM.

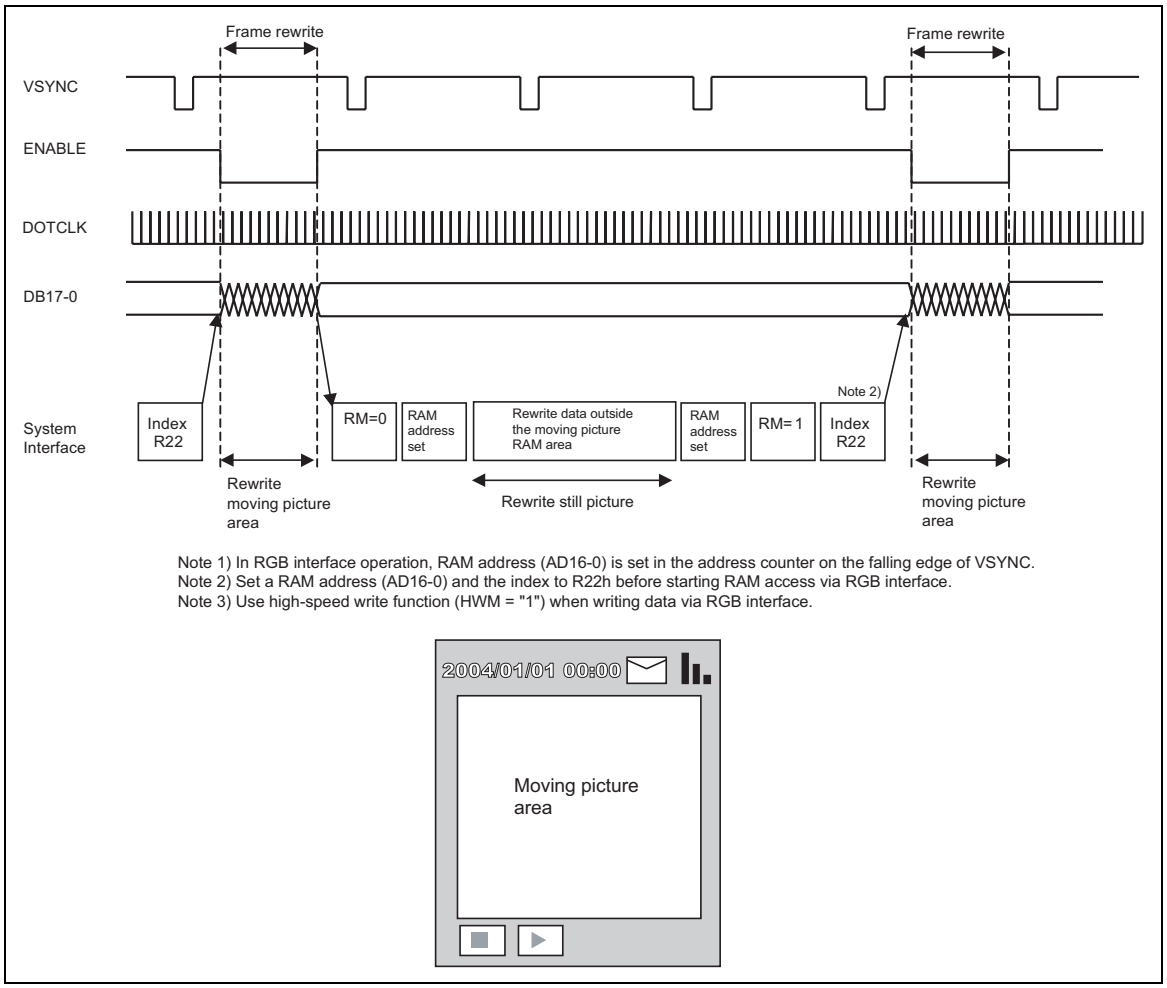


Figure 16

Read Data from GRAM (R22h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	RAM read data RD[17:0] is transferred via different data bus in different interface operation.															

RD[17:0]: 18-bit data read from the GRAM. RAM read data RD[17:0] is transferred via different data bus in different interface operation.

When the R61503U reads data from the GRAM to the microcomputer, the first word, which is read immediately after the RAM address set instruction is executed, is taken in the internal read-data latch and invalid data is sent to the data bus. Valid data is sent to the data bus when the R61503U reads out the second and subsequent words.

When either 8-bit or 16-bit interface is selected, the LSBs of R and B dot data are not read out.

Note: This register is not available in RGB interface operation.

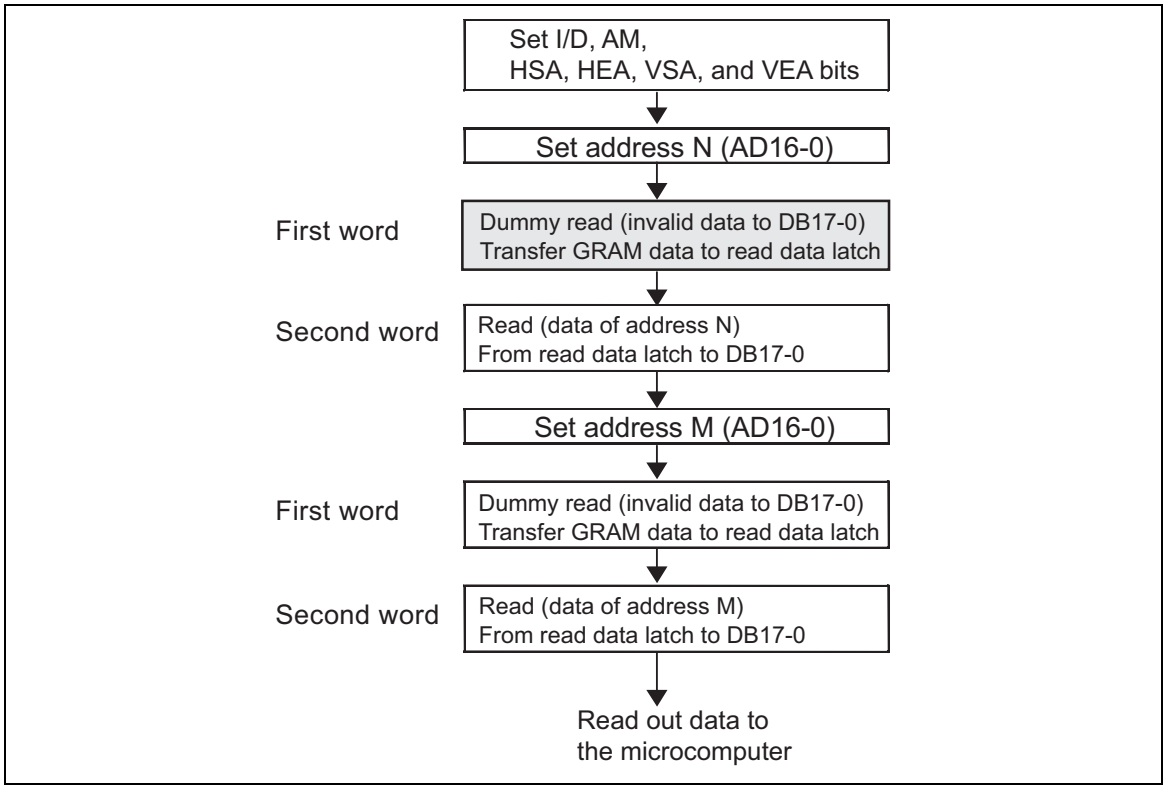


Figure 17 GRAM read sequence

NV Memory Read Data 1/2/3 (R28h/R29h/R2Ah)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R28	W	1	0	0	0	0	0	0	0	0	0	0	0	0	UID [3]	UID [2]	UID [1]	UID [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R29	W	1	0	0	0	0	0	0	0	0	EVCME0	0	0	EVCM0[4]	EVCM0[3]	EVCM0[2]	EVCM0[1]	EVCM0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R2A	W	1	0	0	0	0	0	0	0	0	EVCME1	0	0	EVCM1[4]	EVCM1[3]	EVCM1[2]	EVCM1[1]	EVCM1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

UID[3:0]: Data in Address 1, which is read from the internal NV memory and used as the user identification code. See "NV Memory Control" for details.

EVCME0, EVCM1: Select either EVCM0[4:0] or EVCM1[4:0] in the internal NV memory to set the VcomH level when setting VcomH by internal electronic volume. When VCMSEL = 1, the setting written in the internal NV memory, i.e. either EVCM0[4:0] or EVCM1[4:0], is used instead of VCM[4:0], i.e. internal register setting.

Table 40

EVCME1	EVCME0	VcomH setting
0	0	6'h0
0	1	EVCM0[4:0] (data written in Address 2)
1	0	Setting disabled
1	1	EVCM1[4:0] (data written in Address 3)

EVCM0[4:0]: Data in Address 2 in the NV memory to adjust the VcomH voltage using internal electronic volume.

EVCM1[4:0]: Data in Address 3 in the NV memory to adjust the VcomH voltage using internal electronic volume.

γ Control Instruction

γ Control (1) ~ (9) (R30h ~ R3Ah)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30	W	1	0	0	0	0	0	PKP 1[2]	PKP 1[1]	PKP 1[0]	0	0	0	0	0	PKP 0[2]	PKP 0[1]	PKP 0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31	W	1	0	0	0	0	0	PKP 3[2]	PKP 3[1]	PKP 3[0]	0	0	0	0	0	PKP 2[2]	PKP 2[1]	PKP 2[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R32	W	1	0	0	0	0	0	PKP 5[2]	PKP 5[1]	PKP 5[0]	0	0	0	0	0	PKP 4[2]	PKP 4[1]	PKP 4[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R33	W	1	0	0	0	0	0	PRP 1[2]	PRP 1[1]	PRP 1[0]	0	0	0	0	0	PRP 0[2]	PRP 0[1]	PRP 0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R34	W	1	0	0	0	0	0	PKN 1[2]	PKN 1[1]	PKN 1[0]	0	0	0	0	0	PKN 0[2]	PKN 0[1]	PKN 0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R35	W	1	0	0	0	0	0	PKN 3[2]	PKN 3[1]	PKN 3[0]	0	0	0	0	0	PKN 2[2]	PKN 2[1]	PKN 2[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R36	W	1	0	0	0	0	0	PKN 5[2]	PKN 5[1]	PKN 5[0]	0	0	0	0	0	PKN 4[2]	PKN 4[1]	PKN 4[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R37	W	1	0	0	0	0	0	PRN 1[2]	PRN 1[1]	PRN 1[0]	0	0	0	0	0	PRN 0[2]	PRN 0[1]	PRN 0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R38	W	1	0	0	0	VRP 1[4]	VRP 1[3]	VRP 1[2]	VRP 1[1]	VRP 1[0]	0	0	0	VRP 0[4]	VRP 0[3]	VRP 0[2]	VRP 0[1]	VRP 0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R39	W	1	0	0	0	VRN 1[4]	VRN 1[3]	VRN 1[2]	VRN 1[1]	VRN 1[0]	0	0	0	VRN 0[4]	VRN 0[3]	VRN 0[2]	VRN 0[1]	VRN 0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PKP5-0[2:0] γ fine adjustment register for positive polarity
PRP1-0[2:0] gradient adjustment register for positive polarity
PKN5-0[2:0] γ fine adjustment register for negative polarity
PRN1-0[2:0] gradient adjustment register for negative polarity
VRP1-0[4:0] amplitude adjustment register for positive polarity
VRN1-0[4:0] amplitude adjustment register for negative polarity

See "γ Correction function" for details.

Window Address Control Instruction

Window Horizontal RAM Start Address (R50h), Window Horizontal RAM End Address (R51h)

Window Vertical RAM Start Address (R52h), Window Vertical RAM End Address (R52h),

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R50	W	1	0	0	0	0	0	0	0	0	HSA [7]	HSA [6]	HSA [5]	HSA [4]	HSA [3]	HSA [2]	HSA [1]	HSA [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51	W	1	0	0	0	0	0	0	0	0	HEA [7]	HEA [6]	HEA [5]	HEA [4]	HEA [3]	HEA [2]	HEA [1]	HEA [0]
	Default		0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1
R52	W	1	0	0	0	0	0	0	0	VSA [8]	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R53	W	1	0	0	0	0	0	0	0	VEA [8]	VEA [7]	VEA [6]	VEA [5]	VEA [4]	VEA [3]	VEA [2]	VEA [1]	VEA [0]
	Default		0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1

HSA[7:0]/HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that "00"h ≤ HSA[7:0] < HEA[7:0] ≤ "AF"h.

VSA[8:0]/VEA[8:0]: VSA[8:0] and VEA[8:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the vertical range to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that "00"h ≤ VSA[8:0] < VEA[8:0] ≤ "DB"h.

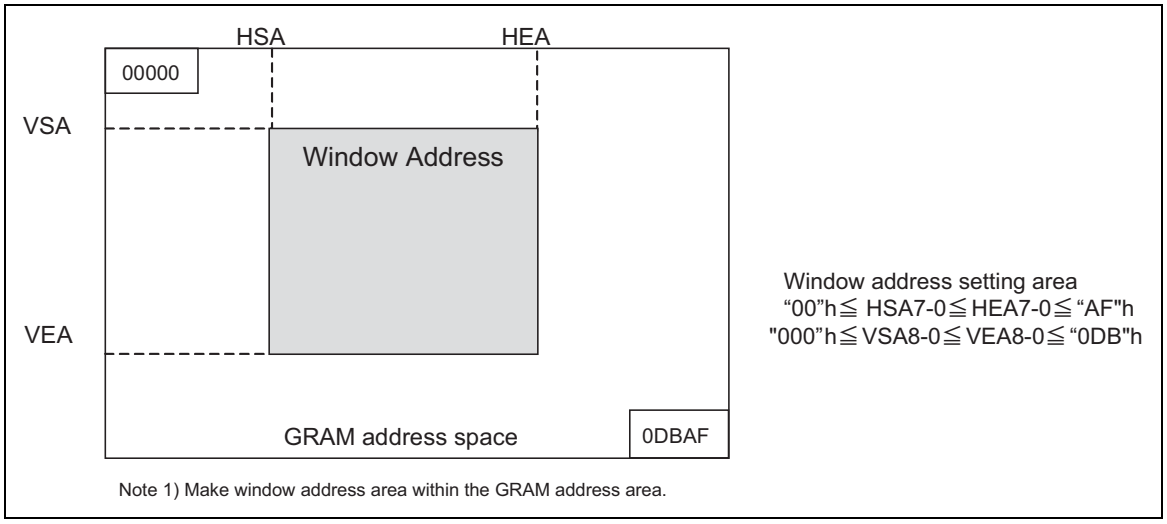


Figure 18 GRAM Address Map and Window Address Area

Base Image Display Control Instruction

Driver Output Control (R70h), Base Image Display Control (R71h), Vertical Scroll Control (R7Ah),

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R70	W	1	GS	0	0	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	0	0	0	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R71	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VLE	REV
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R7A	W	1	0	0	0	0	0	0	0	0	VL [7]	VL [6]	VL [5]	VL [4]	VL [3]	VL [2]	VL [1]	VL [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN[4:0]: Specifies the gate line where the gate driver starts scan.

Table 41

SCN [4:0]	Scan start position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
4'h00	G1	G220	G1	G220
4'h01	G9	G212	G17	G204
4'h02	G17	G204	G33	G188
4'h03	G25	G196	G49	G172
4'h04	G33	G188	G65	G156
4'h05	G41	G180	G81	G140
4'h06	G49	G172	G97	G124
4'h07	G57	G164	G113	G108
4'h08	G65	G156	G129	G92
4'h09	G73	G148	G145	G76
4'h0A	G81	G140	G161	G60
4'h0B	G89	G132	G177	G44
4'h0C	G97	G124	G193	G28
4'h0D	G105	G116	G209	G12
4'h0E	G113	G108	G9	G216
4'h0F	G121	G100	G25	G200
4'h10	G129	G92	G41	G184
4'h11	G137	G84	G57	G168
4'h12	G145	G76	G73	G152
4'h13	G153	G68	G89	G136
4'h14	G161	G60	G105	G120
4'h15	G169	G52	G121	G104
4'h16	G177	G44	G137	G88
4'h17	G185	G36	G153	G72
4'h18	G193	G28	G169	G56
4'h19	G201	G20	G185	G40
4'h1A	G209	G12	G201	G24
4'h1B	G217	G4	G217	G8
4'h1C-4'h1F	Setting disabled	Setting disabled	Setting disabled	Setting disabled

NL[4:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[4:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

Table 42

NL [4:0]	LCD drive line
6'h00	0 line
6'h01	16 lines
6'h02	24 lines
6'h03	32 lines
6'h04	40 lines
6'h05	48 lines
6'h06	56 lines
6'h07	64 lines
6'h08	72 lines
6'h09	80 lines
6'h0A	88 lines
6'h0B	96 lines
6'h0C	104 lines
6'h0D	112 lines
6'h0E	120 lines
6'h0F	128 lines

NL [4:0]	LCD drive line
6'h10	136 lines
6'h11	144 lines
6'h12	152 lines
6'h13	160 lines
6'h14	168 lines
6'h15	176 lines
6'h16	184 lines
6'h17	192 lines
6'h18	200 lines
6'h19	208 lines
6'h1A	216 lines
6'h1B	220 lines

GS: Sets the direction of scan by the gate driver in the range determined by SCN[4:0] and NL[4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

When GS = 0, the scan direction is from G1 to G220.
When GS = 1, the scan direction is from G220 to G1

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the R61503U to display the same image from the same set of data whether the liquid crystal panel is normally black or white. The source output level during the front, back porch periods and blank periods is determined by register setting (PTS).

Table 43 GRAM Data-grayscale level inversion

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V31	V0
	:	:	:
	18'hFFFFF	V0	V31
1	18'h00000	V0	V31
	:	:	:
	18'hFFFFF	V31	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the R61503U starts displaying the base image from the line (of the physical display) determined by VL[7:0] bits. VL[7:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

Table 44

VLE	Base image
0	Fixed
1	Enable scrolling

VL[7:0]: Sets the amount of scrolling of the base image. The base image is scrolled in vertical direction and displayed from the line which is determined by VL[7:0]. Make sure BSA(0) +VL[7:0] ≤ BEA(220).

Partial control instruction

Partial image 1 display position (R80h)

Partial image 1 RAM start address (R81h), Partial image 1 RAM end address (R82h)

Partial image 2 display position (R83h)

Partial image 2 RAM Address (R84h), Partial image 2 RAM end address (R85h),

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R80	W	1	0	0	0	0	0	0	0	0	PTDP0[7]	PTDP0[6]	PTDP0[5]	PTDP0[4]	PTDP0[3]	PTDP0[2]	PTDP0[1]	PTDP0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R81	W		0	0	0	0	0	0	0	0	PTSA0[7]	PTSA0[6]	PTSA0[5]	PTSA0[4]	PTSA0[3]	PTSA0[2]	PTSA0[1]	PTSA0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R82	W		0	0	0	0	0	0	0	0	PTEA0[7]	PTEA0[6]	PTEA0[5]	PTEA0[4]	PTEA0[3]	PTEA0[2]	PTEA0[1]	PTEA0[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R83	W	1	0	0	0	0	0	0	0	0	PTDP1[7]	PTDP1[6]	PTDP1[5]	PTDP1[4]	PTDP1[3]	PTDP1[2]	PTDP1[1]	PTDP1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R84	W	1	0	0	0	0	0	0	0	0	PTSA1[7]	PTSA1[6]	PTSA1[5]	PTSA1[4]	PTSA1[3]	PTSA1[2]	PTSA1[1]	PTSA1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R85	W	1	0	0	0	0	0	0	0	0	PTEA1[7]	PTEA1[6]	PTEA1[5]	PTEA1[4]	PTEA1[3]	PTEA1[2]	PTEA1[1]	PTEA1[0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP0[7:0]: Sets the display position of partial image 1.
PTDP1[7:0]: Sets the display position of partial image 2.

The display areas of the partial images 1 and 2 must not overlap each another. In setting, make sure

Partial image 1 display area < Partial image 2 display area, and

Coordinates of partial image 1 display area: (PTDP0, PTDP0+(PTEA0 – PTSA0))
Coordinates of partial image 2 display area: (PTDP1, PTDP1+(PTEA1 – PTSA1))

If PTDP0 is set to “8’h00”, the partial image 1 is displayed from the 1st line of the panel on the base image.

PTSA0[7:0] PTEA0[7:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 1. Make sure PTSA0[7:0] ≤ PTEA0[7:0].

PTSA1[7:0] PTEA1[7:0]: Sets the start line address and the end line address of the RAM area storing the data of partial image 2. Make sure PTSA1[7:0] ≤ PTEA1[7:0].

Panel interface control instruction

Panel interface control 1 (R90h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVI [1]	DIVI [0]	0	0	0	0	RTNI [3]	RTNI [2]	RTNI [1]	RTNI [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTNI[3:0]: Sets 1H (line) period. This setting is enabled while the R61503U's display operation is synchronized with internal clock signal.

DIVI[1:0]: Sets the division ratio of internal clock frequency. The R61503U's internal operation is synchronized with the frequency-divided internal clock, the frequency of which is divided by the division ratio set by DIVI[1:0]. When changing the DIVI[1:0] setting, the width of the reference clock for liquid crystal panel control signals is changed.

The frame frequency can be adjusted by register setting (RTNI and DIVI bits). When changing the number of lines to drive the liquid crystal panel, the frame frequency must be adjusted. See "Frame-Frequency Adjustment Function" for details.

DIVI[1:0] is disenabled in RGB interface operation.

Frame Frequency Calculation

$$\text{Frame frequency} = \frac{fosc}{\text{Clocks per line x division ratio x (line + BP + FP)}} \quad [Hz]$$

fosc : RC oscillation frequency

Line: Number of lines to drive the LCD (NL bits)

Division ratio: DIVI

Clocks per line: RTNI

Table 45 clocks in 1H period (internal clock operation: 1 clock = 1 OSC)

RTNI[3:0]	Clocks per Line	RTNI[3:0]	Clocks per Line
4'h0	16 clocks	4'h8	24 clocks
4'h1	17 clocks	4'h9	25 clocks
4'h2	18 clocks	4'hA	26 clocks
4'h3	19 clocks	4'hB	27 clocks
4'h4	20 clocks	4'hC	28 clocks
4'h5	21 clocks	4'hD	29 clocks
4'h6	22 clocks	4'hE	30 clocks
4'h7	23 clocks	4'hF	31 clocks

Table 46 Division ratio of the internal operation clock

DIVI[1:0]	Division Ratio	Internal Operation Clock Frequency
2'h0	1/1	fosc / 1
2'h1	1/2	fosc / 2
2'h2	1/4	fosc / 4
2'h3	1/8	fosc / 8

Note: fosc: RC oscillation frequency

Panel interface control 2 (R91h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	NOI [2]	NOI [1]	NOI [0]	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOI[2:0]: Sets the gate output non-overlap period when the R61503U's display operation is synchronized with internal clock signal.

Table 47

NOI[2:0]	Gate non-overlap period
3'h0	0 clocks
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: The gate output non-overlap period is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI), from the reference point.

Panel interface control 3 (R92h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTI [2]	SDTI [1]	SDTI [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDTI[2:0]: Sets the source output position when the R61503U's display operation is synchronized with internal clock signal.

Table 48

SDTI[2:0]	Source output position
3'h0	0 clock
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: The source output position is defined by the number of frequency-divided internal clocks, the frequency of which is determined by instruction (DIVI), from the reference point.

Panel interface control 4 (R93h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVE [1]	DIVE [0]	0	0	RTNE [5]	RTNE [4]	RTNE [3]	RTNE [2]	RTNE [1]	RTNE [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RTNE[5:0]: Sets RTNE in combination with DIVE so that the number of DOTCLK calculated from the following formula becomes the number of DOTCLK included in 1H (line) period, when the R61503U's display operation is synchronized with RGB interface signals.

DIVE (division ratio) x RTNE (DOTCLKs) ≤ DOTCLKs in 1H period.

DIVE[1:0]: Sets the division ratio of DOTCLK. The R61503U's internal operation is synchronized with the frequency-divided DOTCLK, the frequency of which is divided by the division ratio set by DIVE[1:0]. This setting is enabled while the R61503U's display operation is synchronized with RGB interface signals.

Table 49 DOTCLKs in 1H period (RGB interface operation)

RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)	RTNE[5:0]	Clocks per line period (1H)
6'h00	Setting inhibited	6'h10	16 clocks	6'h20	32 clocks	6'h30	48 clocks
6'h01	Setting inhibited	6'h11	17 clocks	6'h21	33 clocks	6'h31	49 clocks
6'h02	Setting inhibited	6'h12	18 clocks	6'h22	34 clocks	6'h32	50 clocks
6'h03	Setting inhibited	6'h13	19 clocks	6'h23	35 clocks	6'h33	51 clocks
6'h04	Setting inhibited	6'h14	20 clocks	6'h24	36 clocks	6'h34	52 clocks
6'h05	Setting inhibited	6'h15	21 clocks	6'h25	37 clocks	6'h35	53 clocks
6'h06	Setting inhibited	6'h16	22 clocks	6'h26	38 clocks	6'h36	54 clocks
6'h07	Setting inhibited	6'h17	23 clocks	6'h27	39 clocks	6'h37	55 clocks
6'h08	Setting inhibited	6'h18	24 clocks	6'h28	40 clocks	6'h38	56 clocks
6'h09	Setting inhibited	6'h19	25 clocks	6'h29	41 clocks	6'h39	57 clocks
6'h0A	Setting inhibited	6'h1A	26 clocks	6'h2A	42 clocks	6'h3A	58 clocks
6'h0B	Setting inhibited	6'h1B	27 clocks	6'h2B	43 clocks	6'h3B	59 clocks
6'h0C	Setting inhibited	6'h1C	28 clocks	6'h2C	44 clocks	6'h3C	60 clocks
6'h0D	Setting inhibited	6'h1D	29 clocks	6'h2D	45 clocks	6'h3D	61 clocks
6'h0E	Setting inhibited	6'h1E	30 clocks	6'h2E	46 clocks	6'h3E	62 clocks
6'h0F	Setting inhibited	6'h1F	31 clocks	6'h2F	47 clocks	6'h3F	63 clocks

Table 50 Division Ratio of DOTCLK (RGB interface operation)

DIVE[1:0]	Division Ratio	Internal operation clock unit in RGB interface operation			
		18-bit RGB Interface	DOTCLK = 5MHz	6-bit x3 transfers RGB Interface	DOTCLK = 15MHz
2'h0	Setting inhibited	Setting inhibited	-	Setting inhibited	-
2'h1	1/4	4 DOTCLKs	0.8 μS	12 DOTCLKs	0.8 μS
2'h2	1/8	8 DOTCLKs	1.6 μS	24 DOTCLKs	1.6 μS
2'h3	1/16	16 DOTCLKs	3.2 μS	48 DOTCLKs	3.2 μS

Panel interface control 5 (R94h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	NOE [3	NOE [2]	NOE [1]	NOE [0]	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOE[3:0]: Sets the gate output non-overlap period when the R61503U's display operation is synchronized with RGB interface signals.

Table 51

NOE[3:0]	Gate non-overlap period	NOE[3:0]	Gate non-overlap period
4'h0	0 clocks	4'h8	8 clocks
4'h1	1 clock	4'h9	9 clock
4'h2	2 clocks	4'hA	10 clocks
4'h3	3 clocks	4'hB	11 clocks
4'h4	4 clocks	4'hC	12 clocks
4'h5	5 clocks	4'hD	13 clocks
4'h6	6 clocks	4'hE	14 clocks
4'h7	7 clocks	4'hF	15 clocks

Note: 1 clock = (number of data transfer/pixel) x DIVE (division ratio) [DOTCLK]

Panel interface control 6 (R95h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTE [2]	SDTE [1]	SDTE [0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SDTE[2:0]: Sets the source output position and Vcom alternating position. This setting is enabled while the R61503U's display operation is synchronized with RGB interface signals.

Table 52

SDTE[2:0]	Source output position Vcom alternating position
3'h0	0 clock
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note: 1 clock = (number of data transfer/pixel) x DIVE (division ratio) [DOTCLK]

NV Memory Control

NV Memory Access Control 1 (RA0h), NV Memory Access Control 2 (RA1h)

Calibration Control (RA4h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
RA0	W/R	1	0	0	0	0	0	0	0	0	TE	0	EOP [1]	EOP [0]	0	0	EAD [1]	EAD [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RA1	W/R		0	0	0	0	0	0	0	0	ED [7]	ED [6]	ED [5]	ED [4]	ED [3]	ED [2]	ED [1]	ED [0]
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RA4	W/R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB
	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TE: Enable internal NV memory control bit (EOP). Follow the NV memory control sequence when setting TE. When resetting register (loading EOP = 2'h2) and executing a calibration, TE is set automatically according to the internal automatic sequence and it does not have to be set.

EOP[1:0]: Internal NV memory control bit. Follow the NV memory control sequence when setting EOP[1:0].

Table 53

EOP[1:0]	NV memory control
2'h0	Halt
2'h1	Write
2'h2	Reset register (load)

EAD[1:0]: Internal NV memory address. Set EAD[1:0] = 00 ~ 10 when writing to the internal NV memory. The EAD[1:0] setting determines to which register (R28h, R29h, R2Ah) the data ED[7:0] is written.

ED[7:0]: The data written in the internal NV memory.

Table 54

EAD[1:0]	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
2'h0	0	0	0	0	UID[3]	UID[2]	UID[1]	UID[0]
2'h1	EVCME0*	0	0	EVCM0[4]	EVCM0[3]	EVCM0[2]	EVCM0[1]	EVCM0[0]
2'h2	EVCME1*	0	0	EVCM1[4]	EVCM1[3]	EVCM1[2]	EVCM1[1]	EVCM1[0]

Note*: Make sure to write "1" to EVCME0, EVCME1.

CALB: When CALB = 1, the R61503U executes a calibration to the internal operation. Set CALB = 1 after power-on reset. The CALB setting is automatically returned to "0".

Instruction List

Main category		Sub category		Upper code								Lower code							
Upper Index		Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
–	Index			*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status read			L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
0*	Display control 1	00h	Start oscillation	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
			Device code read	0	0	0	1	0	1	0	1	0	0	0	0	0	0	1	1
		01h	Driver output control 1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
		02h	Liquid crystal drive waveform	0	0	0	0	0	1	BC0	EOR	0	0	0	0	0	0	0	0
		03h	Entry mode	TRI	DFM1	DFM0	BGR	0	DACKE	HWM		0	0	ID1	ID0	AM	0	0	0
		04h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		05h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		06h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		07h	Display control 1	0	0	PTDE1	PTDE0	0	0	BASEE	0	0	0	GON	DTE	CL	0	D1	D0
		08h	Display control 2	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
		09h	Display control 3	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
		0A-0Bh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0Ch	External display interface 1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
		0Dh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0Eh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0Fh	External display interface 2	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	DPL	EPL
1*	Power control	10h	Power control 1	0	0	0	SAP	BT3	BT2	BT1	BT0	APE	0	AP1	AP0	0	DSTB	SLP	STB
		11h	Power control 2	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC01	0	VC2	VC1	VC0
		12h	Power control 3	0	0	0	VON	0	0	0	VCMR	VREG1R	0	PSON	PON	VRH3	VRH2	VRH1	VRH0
		13h	Power control 4	VCOMG	0	0	0	VDV3	VDV2	VDV1	VDV0	VCMSEL	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
		14h	Power control 5	DC5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		15h- 17h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		18h	Power control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PSE
		19h-1Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2*	RAM Access	20h	RAM Address set (horizontal direction)	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		21h	RAM Address set (vertical direction)	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
		22h	RAM data write/ read	RAM write data (WD17-0) / read data (RD17-0) bits are transferred via different data bus lines according to the selected interface's format.															
		23h- 27h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		28h	NV memory read data 1	0	0	0	0	0	0	0	0	0	0	0	0	UID3	UID2	UID1	UID0
		29h	NV memory read data 2	0	0	0	0	0	0	0	0	EVCME0	0	0	EVCM04	EVCM03	EVCM02	EVCM01	EVCM00
		2Ah	NV memory read data 3	0	0	0	0	0	0	0	0	EVCME1	0	0	EVCM14	EVCM13	EVCM12	EVCM11	EVCM10
		2Bh- 2Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3*	Gamma control	30h	Gamma control 1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
		31h	Gamma control 2	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
		32h	Gamma control 3	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
		33h	Gamma control 4	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
		34h	Gamma control 5	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
		35h	Gamma control 6	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
		36h	Gamma control 7	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
		37h	Gamma control 8	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
		38h	Gamma control 9	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	VRP04	VRP03	VRP02	VPR01	VRP00
		39h	Gamma control 10	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	VRN04	VRN03	VRN02	VRN01	VRN00
		3Ah	Gamma control 11	0	0	0	VAJN14	VAJN13	VAJN12	VAJN11	VAJN10	0	0	0	VAJP04	VAJP03	VAJP02	VAJP01	VAJP00

Main category		Sub category		Upper code								Lower code							
Upper Index		Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
		3Bh-3Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4*		40h- 4Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5*	Window address control	50h	Horizontal RAM address start position	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
		51h	Horizontal RAM address end position	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
		52h	Vertical RAM address start position	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
		53h	Vertical RAM address end position	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
		54h- 5Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6*		60h- 6Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7*	Base image display control	70h	Driver output control 2	GS	0	0	NL4	NL3	NL2	NL1	NL0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0
		71h	Base image display control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VLE	REV
		72h- 79h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		7Ah	Vertical scroll control	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL5	VL3	VL2	VL1	VL0
		7Bh- 7Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8*	Partial image control	80h	Partial image 1 display position	0	0	0	0	0	0	0	0	PTDP 07	PTDP 06	PTDP 05	PTDP 04	PTDP 03	PTDP 02	PTDP 01	PTDP 00
		81h	Partial image 1 RAM area (start line)	0	0	0	0	0	0	0	0	PTSA 07	PTSA 06	PTSA 05	PTSA 04	PTSA 03	PTSA 02	PTSA 01	PTSA 00
		82h	Partial image 1 RAM area (end line)	0	0	0	0	0	0	0	0	PTEA 07	PTEA 06	PTEA 05	PTEA 04	PTEA 03	PTEA 02	PTEA 01	PTEA 00
		83h	Partial image 2 display position	0	0	0	0	0	0	0	0	PTDP 17	PTDP 16	PTDP 15	PTDP 14	PTDP 13	PTDP 12	PTDP 11	PTDP 10
		84h	Partial image 2 RAM area (start line)	0	0	0	0	0	0	0	0	PTSA 17	PTSA 16	PTSA 15	PTSA 14	PTSA 13	PTSA 12	PTSA 11	PTSA 10
		85h	Partial image 2 RAM area (end line)	0	0	0	0	0	0	0	0	PTEA 17	PTEA 16	PTEA 15	PTEA 14	PTEA 13	PTEA 12	PTEA 11	PTEA 10
		86h- 8Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9*	Panel interface control	90h	Panel interface control 1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	0	RTNI3	RTNI2	RTNI1	RTNI0
		91h	Panel interface control 2	0	0	0	0	0	NOI2	NOI1	NOI0	0	0	0	0	0	0	0	0
		92h	Panel interface control 3	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTI2	SDTI1	SDTI0
		93h	Panel interface control 4	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0
		94h	Panel interface control 5	0	0	0	0	NOE3	NOE2	NOE1	NOE0	0	0	0	0	0	0	0	0
		95h	Panel interface control 6	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTE2	SDTE1	SDTE0
		96h- 97h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		98h- 9Fh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
A*	NV memory control	A0h	NV memory access control 1	0	0	0	0	0	0	0	0	TE	0	EOP1	EOP0	0	0	EAD1	EAD0
		A1h	NV memory access control 2	0	0	0	0	0	0	0	0	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
		A2h-A3h	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		A4h	Calibration control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CALB
		A5h-AFh	Setting disabled	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reset Function

The R61503U is initialized by the RESET input. During reset period, the R61503U is in a busy state and instruction from the MPU and GRAM access are not accepted. The R61503U's internal power supply circuit unit is initialized also by the RESET input. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes (for 10 ms). During this period, GRAM access and initial instruction setting are prohibited.

1. Initial state of instruction bits (default)

See the instruction list of p.86. The default value is shown in the parenthesis of each instruction bit cell.

2. RAM Data initialization

The RAM data is not automatically initialized by the RESET input. It must be initialized by software in display-off period (D1-0 = "00").

3. Output pin initial state * see Note

1. LCD driver S1~S528 : GND
   G1~G220 : VGL (= GND)
2. Vcom : GND
3. VcomH : Vci
4. VcomL : GND
5. VREG1OUT : VGS
6. Vci1 : Hi-z
7. DDVDH : Vci
8. VGH : DDVDH (= Vci)
9. VGL : GND
10. Oscillator : Oscillate

4. Initial state of input/output pins* see Note

1. C11+ : Hi-z
2. C11- : Hi-z
3. C13+ : Vci1 (= Hi-z)
4. C13- : GND
5. C21+ : DDVDH (= Vci)
6. C21- : GND
7. C22+ : DDVDH (= Vci)
8. C22- : GND
9. VDD : VDD

Note: The initial states of output and input pins become the states mentioned in the above when the R61503U's power supply circuit is connected as exemplified in "Connection example".

5. Note on Reset function

a) When a RESET input is entered into the R61503U while it is in deep standby mode, the R61503U starts up the inside logic regulator and makes a transition to the initial state. During this period, the state of the interface pins may become unstable. For this reason, do not enter a RESET input in deep standby mode.

b) When transferring instruction and data in either two or three transfers via 8-/16-bit interface, make sure to execute data transfer synchronization after reset operation.

Interface and data format

The R61503U supports system interface for setting instructions etc, and external display interface for displaying a moving picture. The R61503U can select the optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As external display interface, the R61503U supports RGB interface and VSYNC interface, which enables data rewrite operation without flickering the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the R61503U writes display data while the data enable signal (ENABLE) allows write operation via RGB data signal bus (DB17-0). The display data is stored in the R61503U's GRAM so that data is transferred only when rewriting the frames of moving picture and the data transfer required for moving picture display can be minimized. The window address function specifies the RAM area to write data for moving picture display, which enables displaying a moving picture and RAM data in other than the moving picture area simultaneously. To access the R61503U's internal RAM in high speed with low power consumption, use high-speed write function (HWM = 1) in RGB or VSYNC interface operation.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display via system interface by writing the data to the GRAM at faster than the minimum calculated speed in synchronization with the falling edge of VSYNC. In this case, there are restrictions in setting the frequency and the method to write data to the internal RAM.

The R61503U operates in either one of the following four modes according to the state of the display. The operation mode is set in the external display interface control register. When switching from one mode to another, make sure to follow the relevant sequence in setting instruction bits.

Table 55

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM1-0)
Internal operating clock only (Displaying still picture)	System interface (RM = 0)	Internal operating clock (DM1-0 = 00)
RGB interface (1) (Displaying moving picture)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (Rewriting still picture while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Notes: 1. Instructions are set only via system interface.

2. The RGB and VSYNC interfaces cannot be used simultaneously.
3. Do not make changes to the RGB interface operation setting (RIM1-0) while RGB interface is in operation.
4. See the "External Display Interface" section for the sequences when switching from one mode to another.
5. Use high-speed write function (HWM = 1) when writing data via RGB or VSYNC interface.

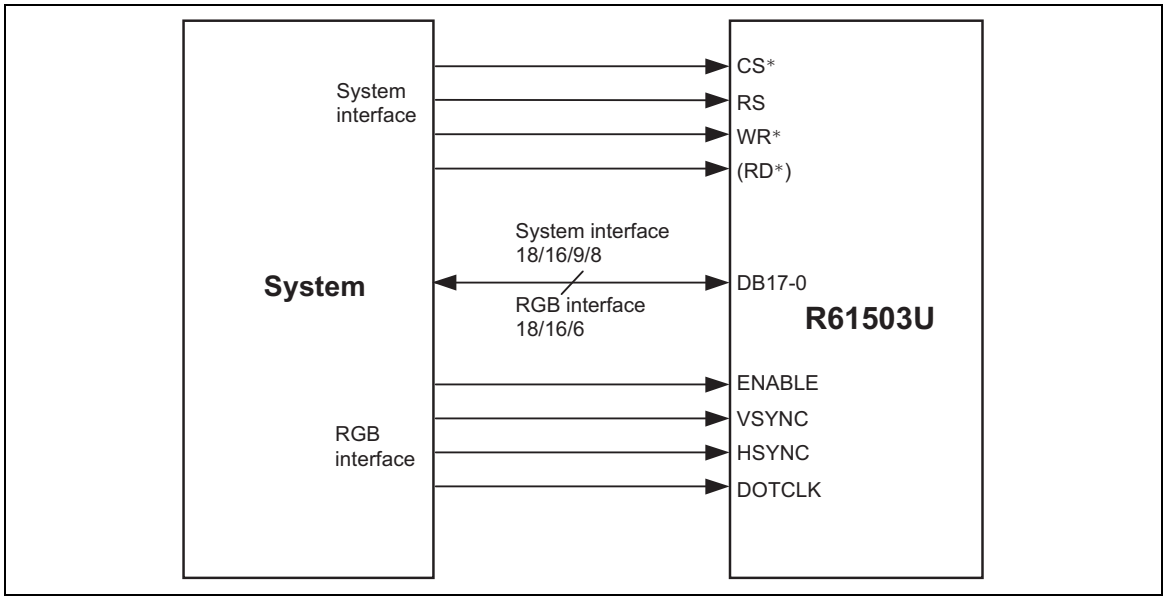


Figure 19

Internal clock operation

The display operation is synchronized with signals generated from internal oscillator's clock (OSC) in this mode. All input via external display interface is disabled in this operation. The internal RAM can be accessed only via system interface.

RGB interface operation (1)

The display operation is synchronized with frame synchronous signal (VSYNC), line synchronous signal (HSYNC), and dot clock signal (DOTCLK) in RGB interface operation. These signals must be supplied during the display operation via RGB interface.

The R61503U transfers display data in units of pixels via DB17-0 pins. The display data is stored in the internal RAM. The combined use of high-speed RAM write mode and window address function can minimize the total number of data transfer for moving picture display by transferring only the data to be written in the moving picture RAM area when it is written and enables the R61503U to display a moving picture and the data in other than the moving picture RAM area simultaneously.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated inside the R61503U by counting the number of clocks of line synchronous signal (HSYNC) from the falling edge of the frame synchronous signal (VSYNC). Make sure to transfer pixel data via DB17-0 pins in accordance with the setting of these periods.

RGB interface operation (2)

This mode enables the R61503U to rewrite RAM data via system interface while using RGB interface for display operation. To rewrite RAM data via system interface, make sure that display data is not transferred via RGB interface (ENABLE = high). To return to the RGB interface operation, change the ENABLE setting first. Then set an address in the RAM address set register and R22h in the index register.

VSYNC interface operation

The internal display operation is synchronized with the frame synchronous signal (VSYNC) in this mode. This mode enables the R61503U to display a moving picture via system interface by writing data in the internal RAM at faster than the calculated minimum speed via system interface from the falling edge of frame synchronous (VSYNC). In this case, there are restrictions in speed and method of writing RAM data. For details, see the "VSYNC Interface" section.

As external input, only VSYNC signal input is valid in this mode. Other input via external display interface becomes disabled.

The front porch (FP), back porch (BP), and the display (NL) periods are automatically calculated from the frame synchronous signal (VSYNC) inside the R61503U according to the instruction settings for these periods.

System Interface

The following kinds of system interface are available with the R61503U and the interface is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

Table 56 IM bits settings and system interface

IM3	IM2	IM1	IM0	Interface operation	DB Pins	Colors
0	0	0	0	Setting disabled	-	-
0	0	0	1	Setting disabled	-	-
0	0	1	0	80-system 16-bit interface	DB17-10 and DB8-1	65,536, 262,144 See Note 1
0	0	1	1	80-system 8-bit interface	DB17-10	65,536, 262,144 See Note 2
0	1	0	*	Clock synchronous serial interface	DB1-0	65,536
0	1	1	*	Setting disabled	-	-
1	0	0	0	Setting disabled	-	-
1	0	0	1	Setting disabled	-	-
1	0	1	0	80-system 18-bit interface	DB17-0	262,144
1	0	1	1	80-system 9-bit interface	DB17-9	262,144
1	1	*	*	Setting disabled	-	-

Notes : 1. 262,144 colors in 2 transfers, 65,536 colors in 1 transfer.
2. 262,144 colors in 3 transfers, 65,536 colors in 2 transfers.

80-system 18-bit interface

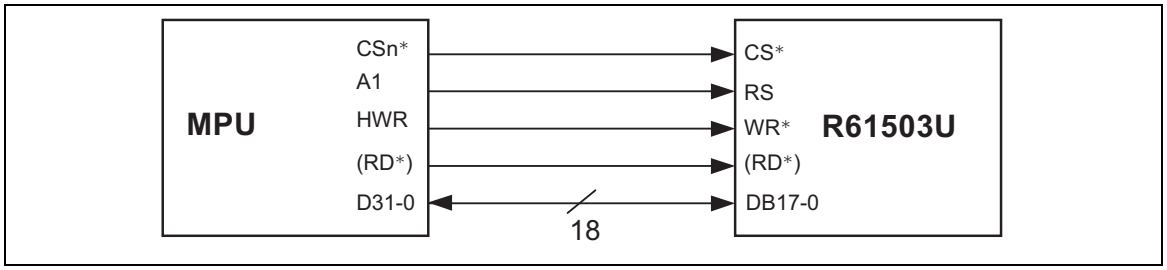


Figure 20

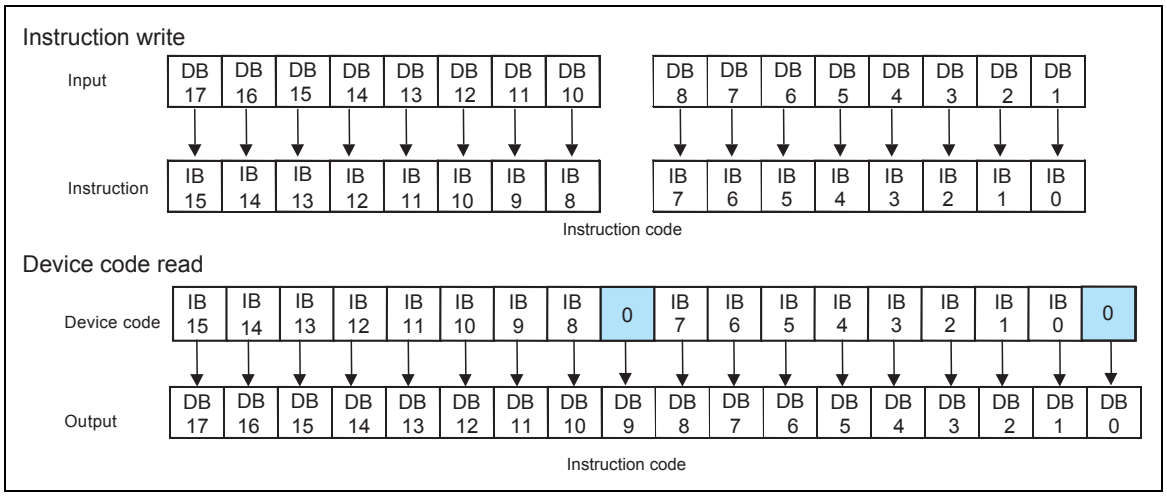


Figure 21 Instruction/Device code read (18-bit interface)

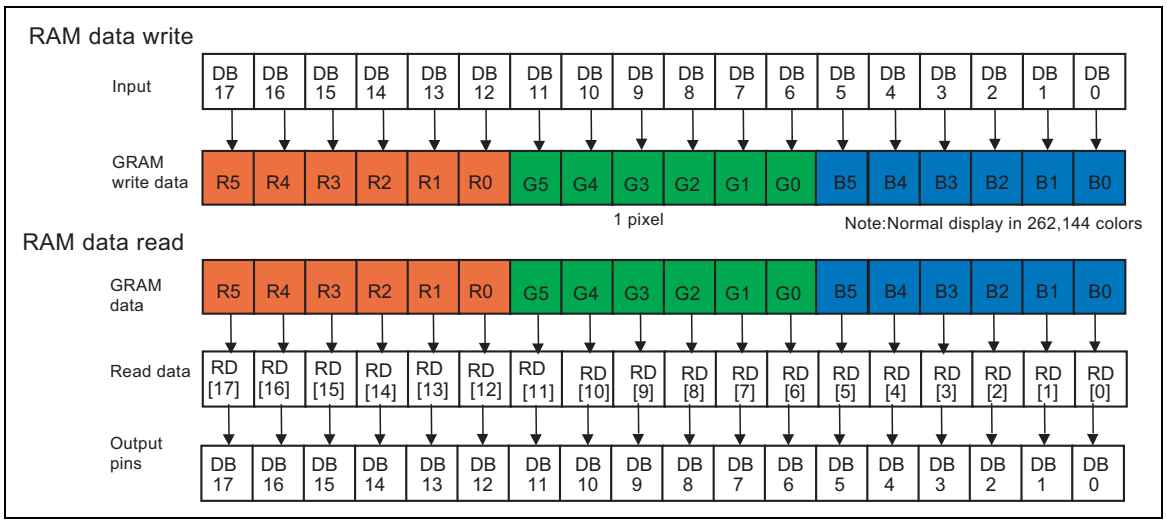


Figure 22 RAM data write/read (18-bit interface)

80-system 16-bit interface

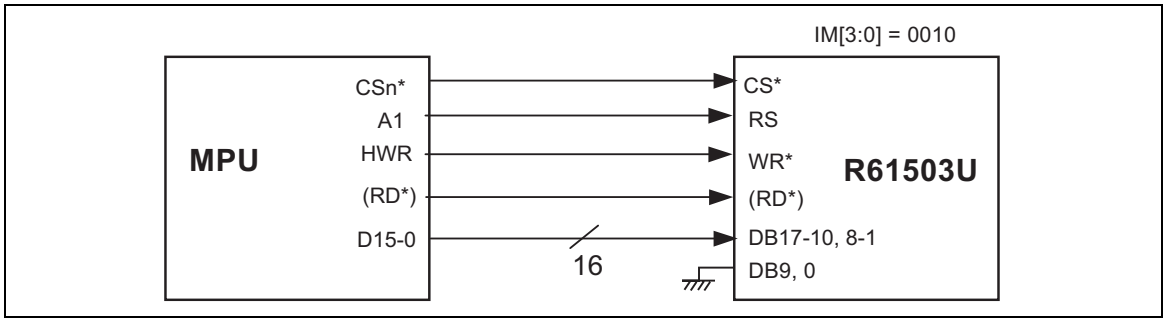


Figure 23

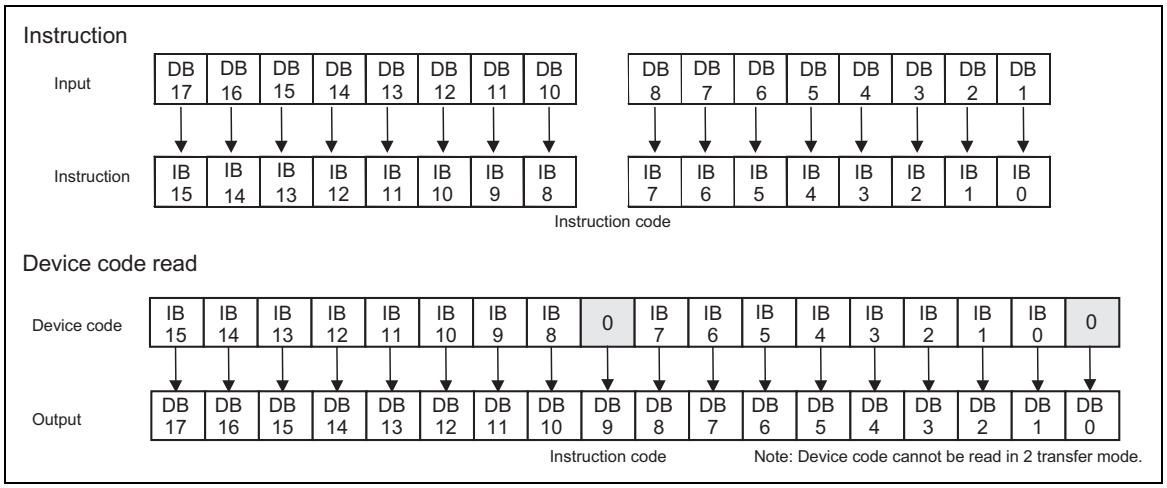


Figure 24 Instruction/Device code read (16-bit interface)

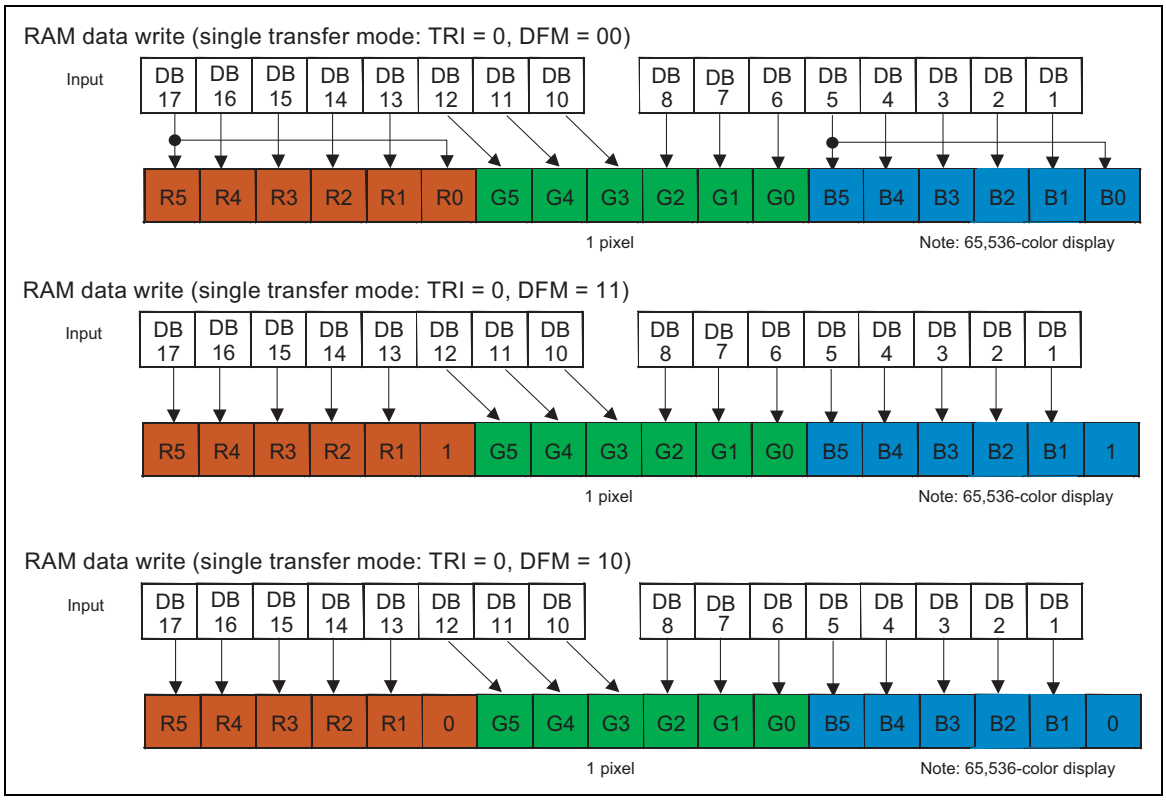


Figure 25 RAM data write (16-bit interface)

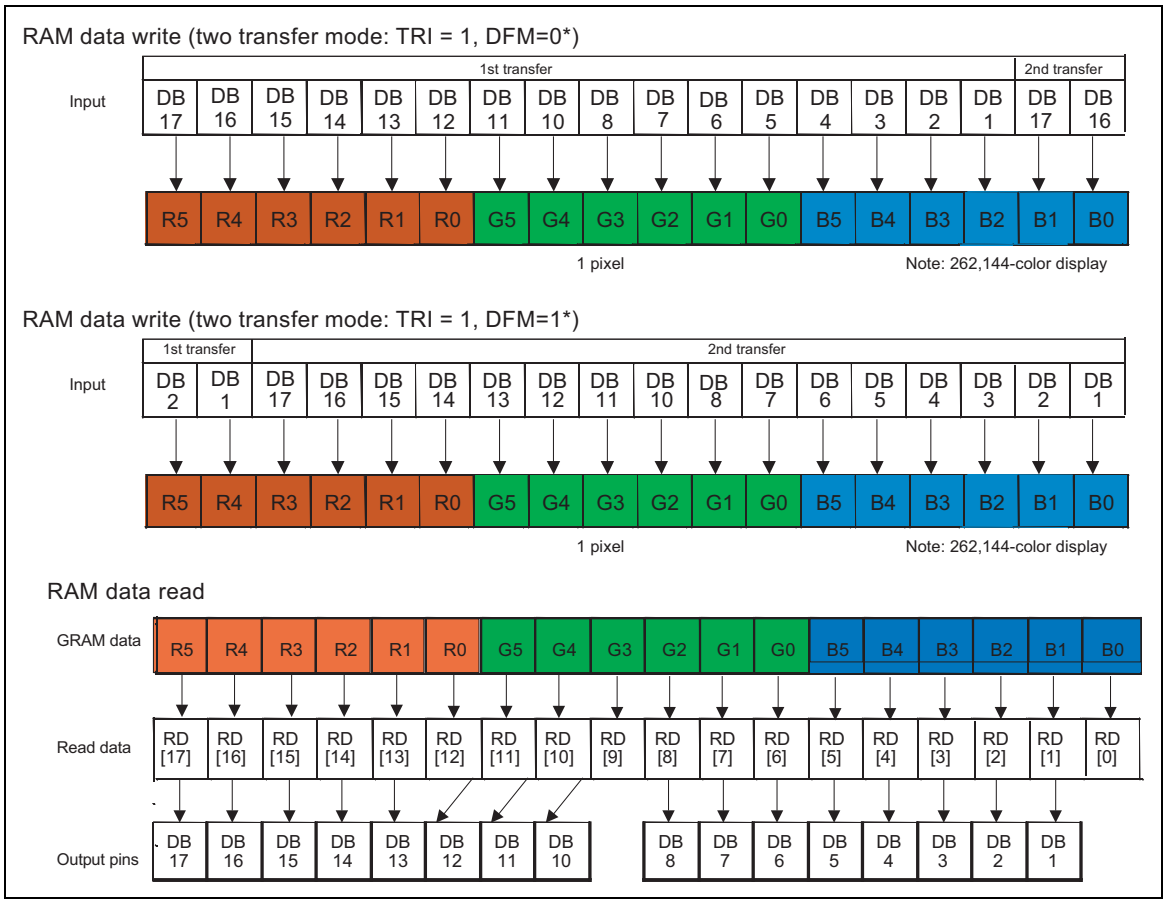


Figure 26 RAM data write/read (16-bit interface)

80-system 9-bit interface

When transferring 16-bit instruction via 9-bit interface (DB17~DB9), it is divided into upper and lower 8 bits (DB9 is not used) and the upper 8 bits are transferred first. The RAM write data is divided into upper and lower 9 bits and the upper 9 bits are transferred first. The unused DB8-0 pins must be fixed at either IOVcc or GND level. When writing in the index register, make sure to write the upper byte (8 bits).

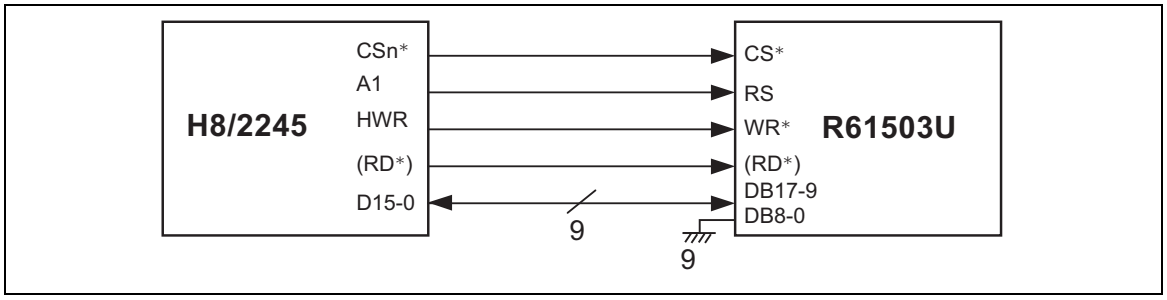


Figure 27

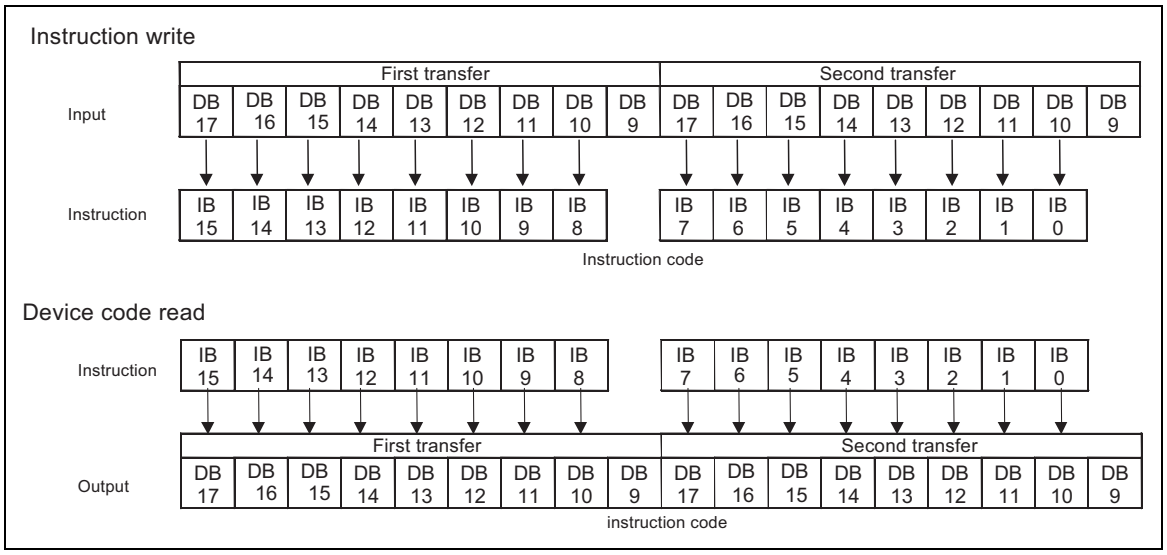


Figure 28 Instruction/Device code read (9-bit interface)

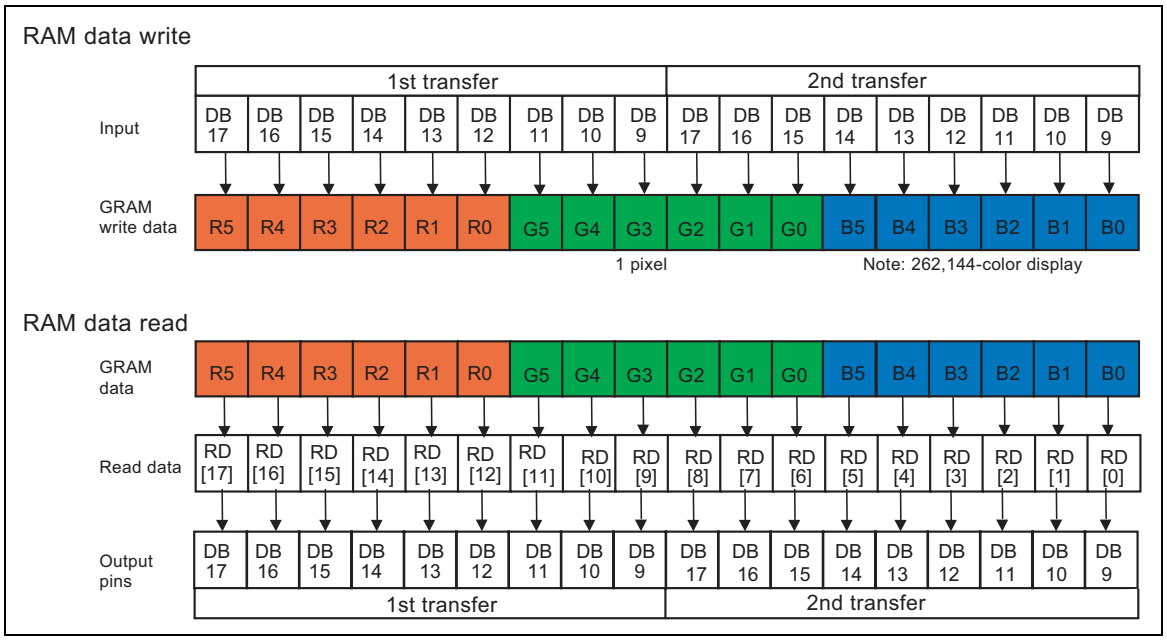


Figure 29 RAM data write/read (9-bit interface)

The R61503U supports data transfer synchronization function to reset the counters, which count the number of upper and lower 9 bits when transferring data via 9-bit bus interface. If a mismatch occurs in transferring upper and lower 9 bits due to noise and so on, "00"H instruction is written 4 times consecutively to reset the counters so that data transfer can resume from upper 9 bits from the next frame. The synchronization function, when executed periodically, can prevent the runaway operation of the display system.

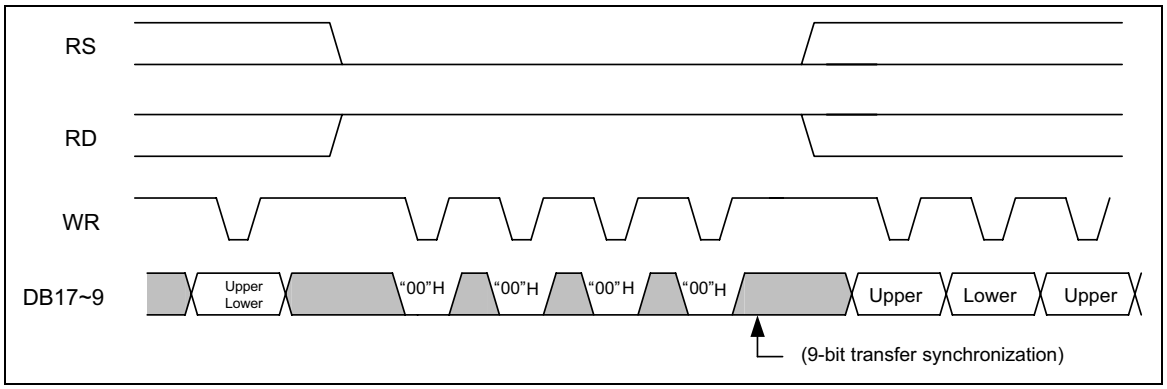


Figure 30 Data transfer synchronization (9-bit)

Make sure to execute transfer synchronization after reset operation, when starting instruction bit transfer.

80-system 8-bit interface

When transferring 16-bit instruction via 8-bit interface (DB17~DB10), it is divided into upper and lower 8 bits and the upper 8 bits are transferred first. The RAM write data is divided into upper and lower 8 bits and the upper 8 bits are transferred first. The unused DB9-0 pins must be fixed at either IOVcc or GND level. When writing in the index register, make sure to write the upper byte (8 bits).

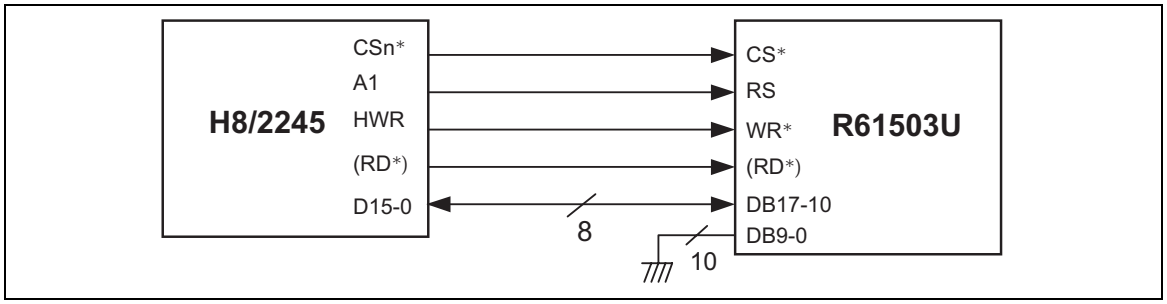


Figure 31

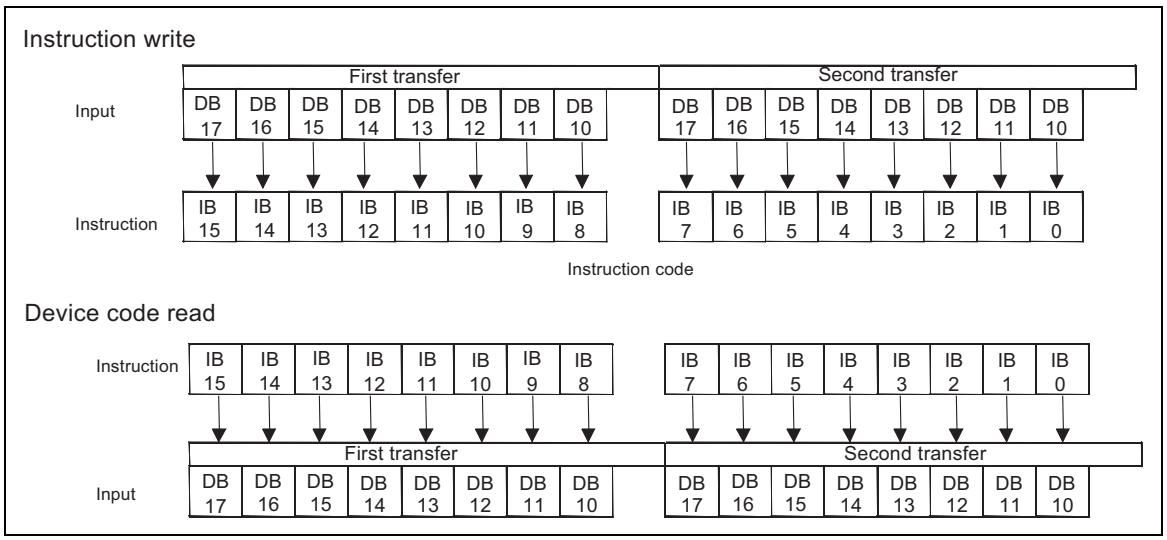


Figure 32 Instruction/Device code read (8-bit interface)

Note: Data cannot be read in 3-transfer mode.

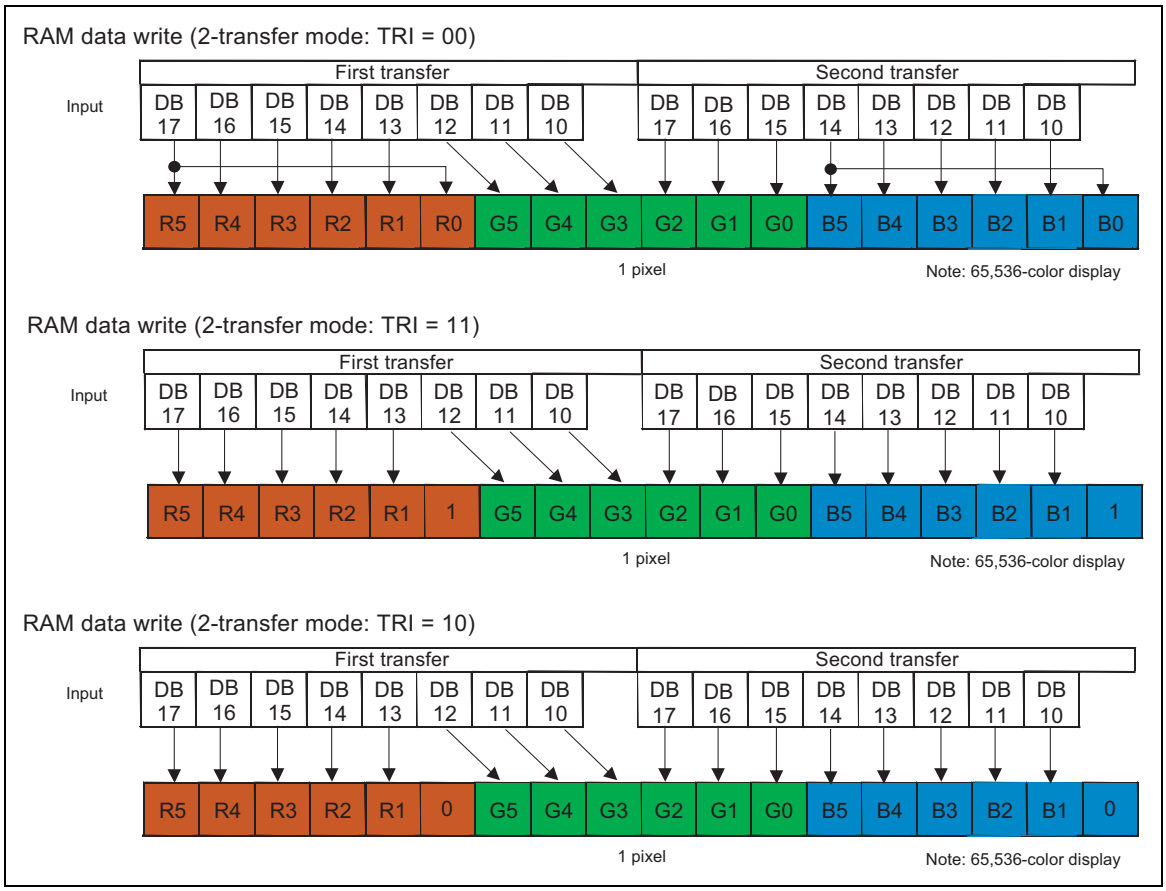


Figure 33 RAM data write (8-bit interface)

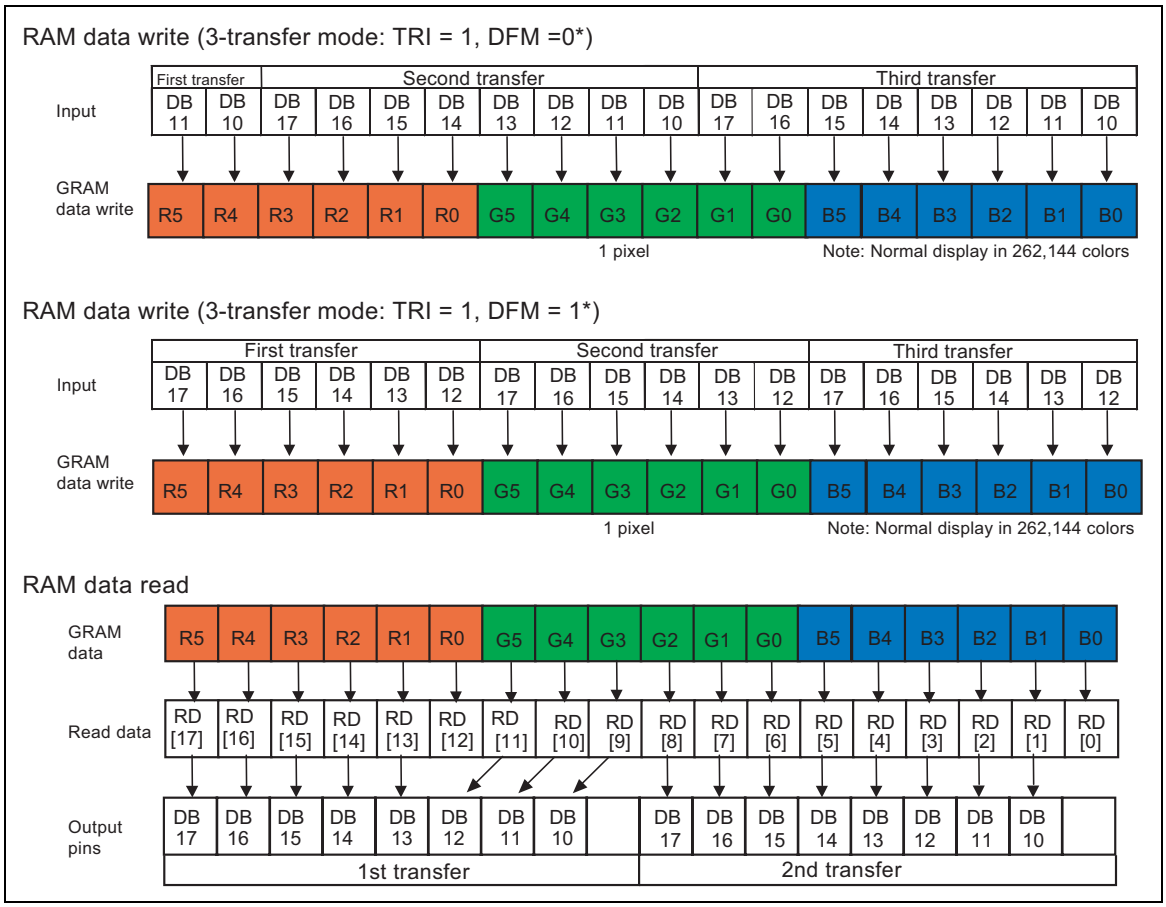


Figure 34 RAM data write/read (8-bit interface)

Note: Data cannot be read in 3-transfer mode.

The R61503U supports data transfer synchronization function to reset the counters, which count the number of upper and lower 8 bits when transferring data via 8-bit bus interface. If a mismatch occurs in transferring upper and lower 8 bits due to noise and so on, "00"H instruction is written 4 times consecutively to reset the counters so that data transfer can resume from upper 8 bits from the next frame. The synchronization function, when executed periodically, can prevent the runaway operation of the display system.

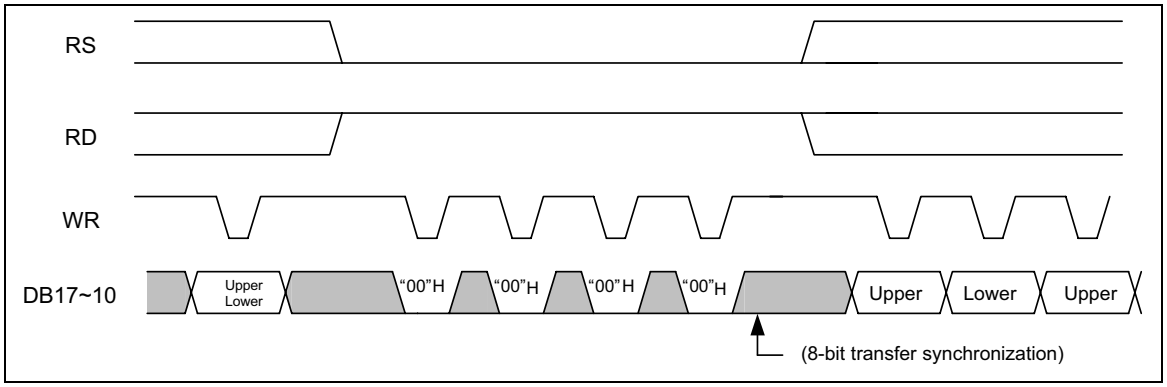


Figure 35 Data transfer synchronization (8-bit)

Make sure to execute transfer synchronization after reset operation, when starting instruction bit transfer.

Serial interface

The serial interface is selected by setting the IM3/2/1 pins to GND/IOVcc/GND levels, respectively. The data is transferred via chip select line (CS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either IOVcc or GND level.

The R61503U recognizes the start of data transfer on the falling edge of CS input and starts transferring the start byte. It recognizes the end of data transfer on the rising edge of CS input. The R61503U is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the R61503U are compared and both 6-bit data match. Then, the R61503U starts taking in subsequent data. The least significant bit of the device identification code is determined by setting the ID pin. Send "01110" to the five upper bits of the device identification code. Two different chip addresses must be assigned to the R61503U because the seventh bit of the start byte is register select bit (RS). When RS = 0, either index register write or status read operation is executed. When RS = 1, either instruction write operation or RAM read/write operation is executed. The eighth bit of the start byte is R/W bit, which selects either read or write operation. The R61503U receives data when the R/W = 0, and transfers data when the R/W = 1.

When writing data to the GRAM via serial interface, the data is written to the GRAM after it is transferred in two bytes. The R61503U writes data to the GRAM in units of 18 bits by adding the same bits as the MSBs to the LSB of R and B dot data.

After receiving the start byte, the R61503U starts transferring or receiving data in units of bytes. The R61503U transfers data from the MSB. The R61503U's instruction consists of 16 bits and it is executed inside the R61503U after it is transferred in two bytes (16 bits: DB15-0) from the MSB. The R61503U expands RAM write data into 18 bits when writing them to the internal GRAM. The first byte received by the R61503U following the start byte is recognized as the upper eight bits of instruction and the second byte is recognized as the lower 8 bits of instruction.

When reading data from the GRAM, valid data is not transferred to the data bus until first five bytes of data are read from the GRAM following the start byte. The R61503U sends valid data to the data bus when it reads the sixth and subsequent byte data.

Table 57 Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: The ID bit is selected by setting the IM0/ID pin.

Table 58

RS	R/W	Function
0	0	Set index register
0	1	Read status
1	0	Write instruction or RAM data
1	1	Read instruction or RAM data

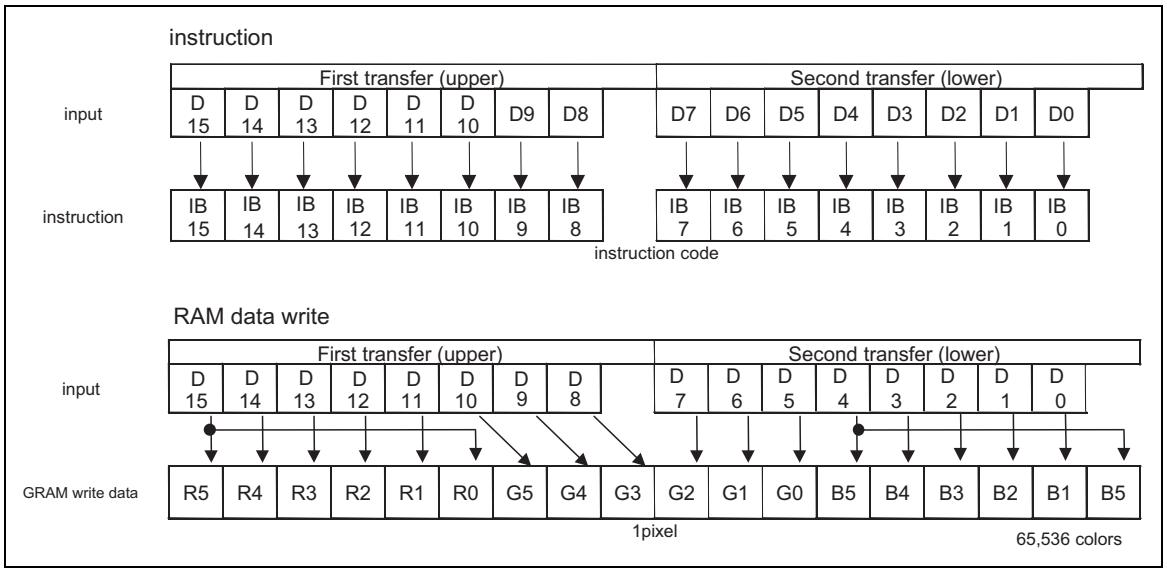
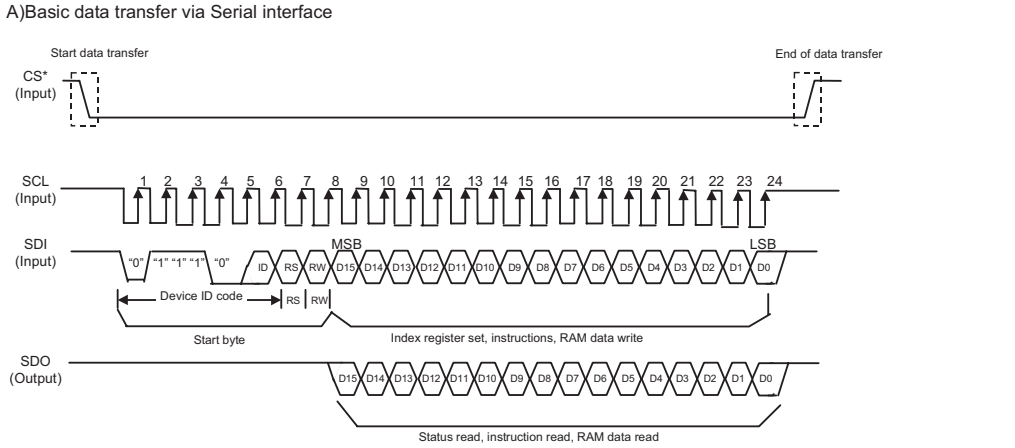
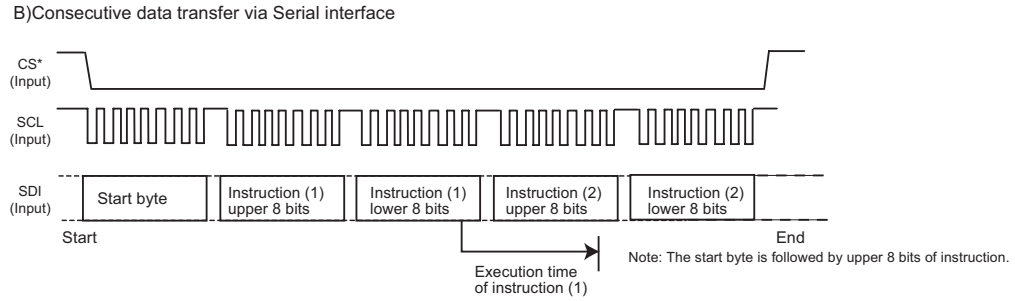
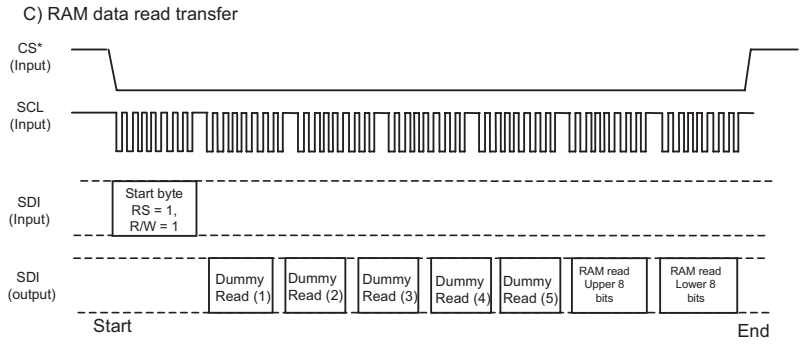


Figure 36 Instruction /RAM data write (Serial interface)







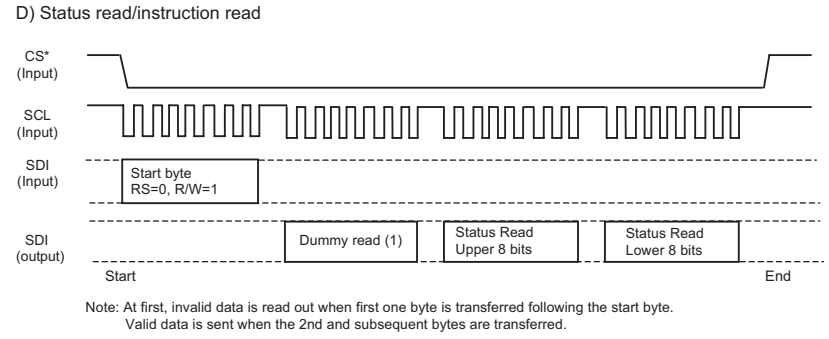


Figure 37 Serial interface data transfer timing

VSYNC Interface

The R61503U supports VSYNC interface, which enables displaying a moving picture via system interface by synchronizing the display operation with the VSYNC signal. VSYNC interface can realize moving picture display with minimum modification to the conventional system operation.

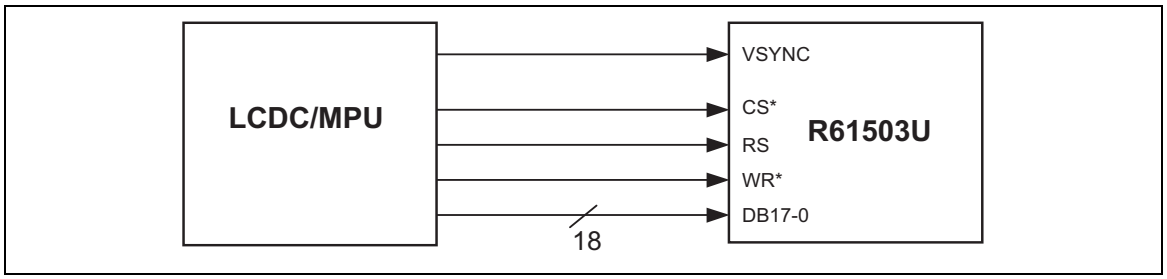


Figure 38 VSYNC interface

The VSYNC interface is selected by setting DM1-0 = 10 and RM = 0. In VSYNC interface operation, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM at faster than the calculated minimum speed (internal display operation speed + margin), it becomes possible to rewrite the moving picture data without flickering the display and display a moving picture via system interface.

The display operation is performed in synchronization with the internal clock signal generated from the internal oscillator and the VSYNC signal. The display data is written in the internal RAM so that the R61503U rewrites the data only within the moving picture area and minimize the number of data transfer required for moving picture display. By writing data using high-speed write function (HWM =1), the R61503U can write data via VSYNC interface in high speed with low power consumption.

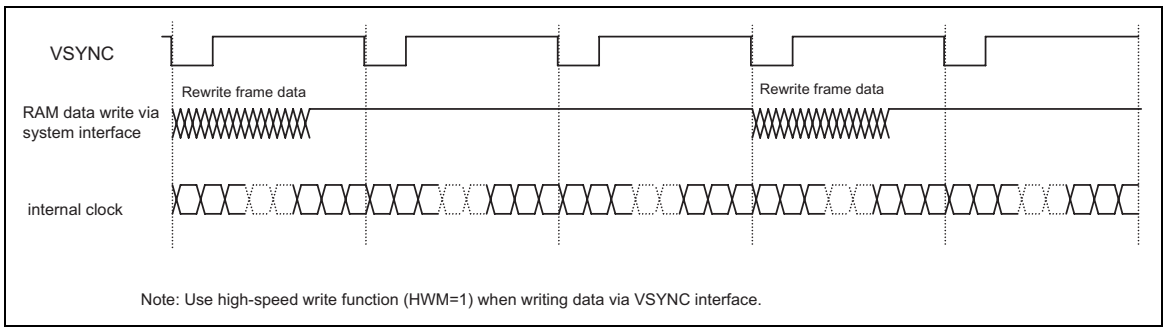


Figure 39 Moving picture data write via VSYNC

The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

Internal clock frequency (fosc) [Hz]
= Frame frequency × (Display lines (NL) + Front porch (FP) + Back porch (BP)) × Clocks per line (RTNI)

RAM write speed (min.) [Hz] > 176 × Display lines (NL) / ((Back porch (BP) + Display lines (NL) – Margins) × Clocks per line (RTNI) × 1 / fosc)

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]

Display size 176 RGB × 220 lines
Display lines 220 lines
Back/front porch 14/2 lines (BP = 1110/ FP = 0010)
Frame frequency 60 Hz
Clocks per line 16 clocks

Internal clock frequency (fosc) [Hz]
= 60 Hz × (220 + 2 + 14) lines × 16 clocks / 0.9 × 1.1 = 277 kHz

Notes: 1. When setting the internal clock frequency, possible causes of fluctuation must also be taken into consideration. In this example, the internal clock frequency allows for a margin of ±10% for variances and guarantees that display operation is completed within one VSYNC cycle.
2. This example includes variances attributed to LSI fabrication process and room temperature. Other possible causes of variances, such as differences in external resistors and voltage change are not considered in this example. It is necessary to include a margin for these factors.

Minimum speed for RAM writing [Hz]
> 176 × 220 / {((14 + 220 - 2) lines × 16 clocks) / 277 kHz} = 2.89 MHz

Notes: 1. In this example, it is assumed that the R61503U starts writing data in the internal RAM on the falling edge of VSYNC.
2. There must at least be a margin of 2 lines between the line to which the R61503U has just written data and the line where display operation on the LCD is performed.

In this example, the RAM write operation at a speed of 2.89MHz or more, which starts on the falling edge of VSYNC, guarantees the completion of data write operation in a certain line address before the R61503U starts the display operation of the data written in that line and moving picture data can be written without causing flicker on the display.

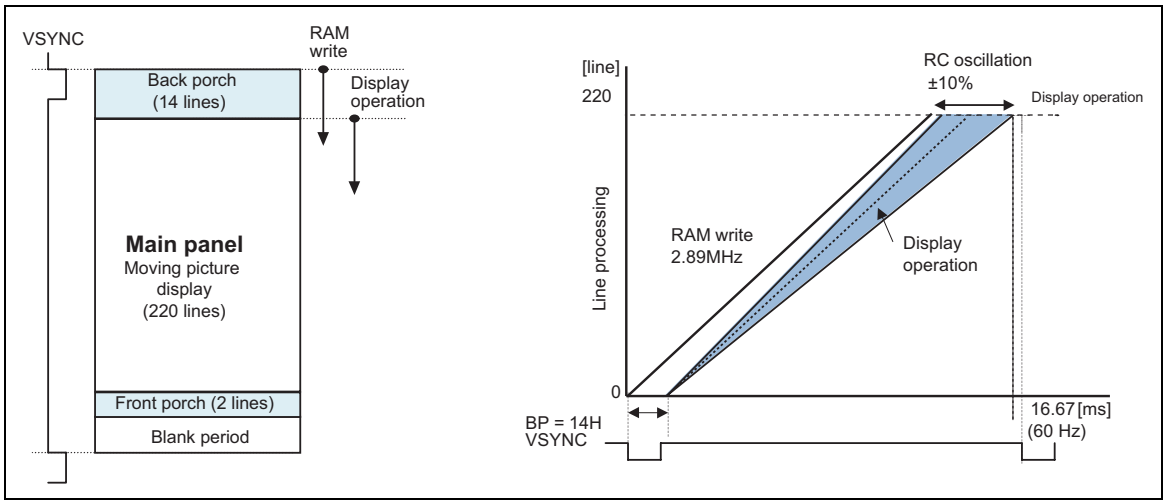


Figure 40 Write/display operation timing via VSYNC interface

Notes to VSYNC Interface Operation

1. The above example of calculation gives a theoretical value. Possible causes of variances of internal oscillator should be taken into consideration. Make enough margins in setting RAM write speed for VSYNC interface operation.

2. The above example shows the values when writing over the full screen. Extra margin will be created if the moving picture display area is smaller than that.

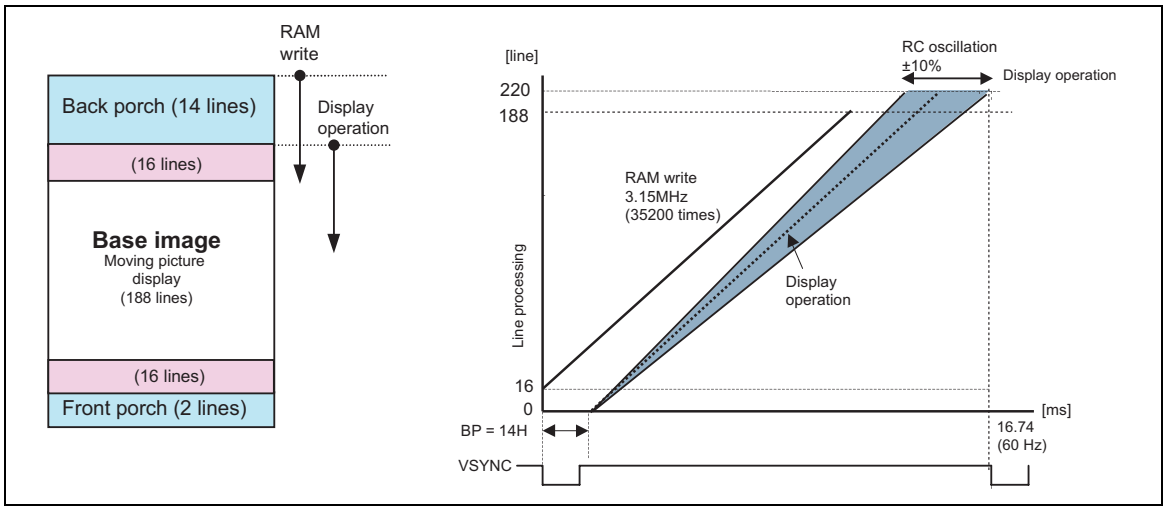


Figure 41 RAM write speed margin

3. The front porch period continues from the end of one frame period to the next VSYNC input.

4. The instructions to switch from internal clock operation (DM1-0 = 00) to VSYNC interface operation modes and vice versa are enabled from the next frame period.

5. The partial display and vertical scroll functions and interlaced scan are not available in VSYNC interface operation.

6. In VSYNC interface operation, set AM = 0 to transfer display data correctly.

7. In VSYNC interface operation, use high-speed write function (HWM = 1) when writing display data to the internal RAM.

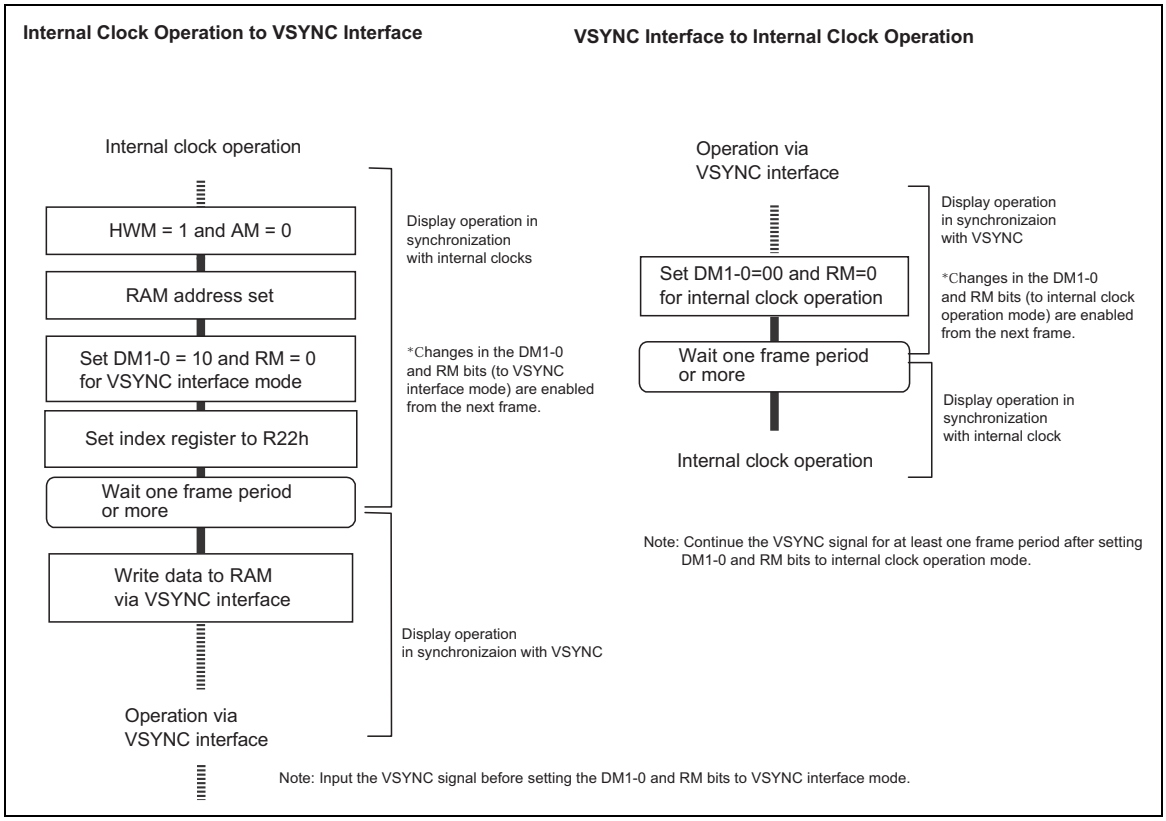


Figure 42 Sequence to switch between VSYNC and Internal clock operation modes

External Display Interface

The R61503U supports the RGB interface. The interface format is set by RM[1:0] bits. The internal RAM is accessible via RGB interface.

Table 59

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, DB11-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting disabled	-

Note: Using more than one RGB interface at a time is prohibited.

RGB Interface

The display operation via RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The data can be written only within the specified area with low power consumption by using window address function and high-speed write mode (HWM = 1). In RGB interface operation, front and back porch periods must be made before and after the display period.

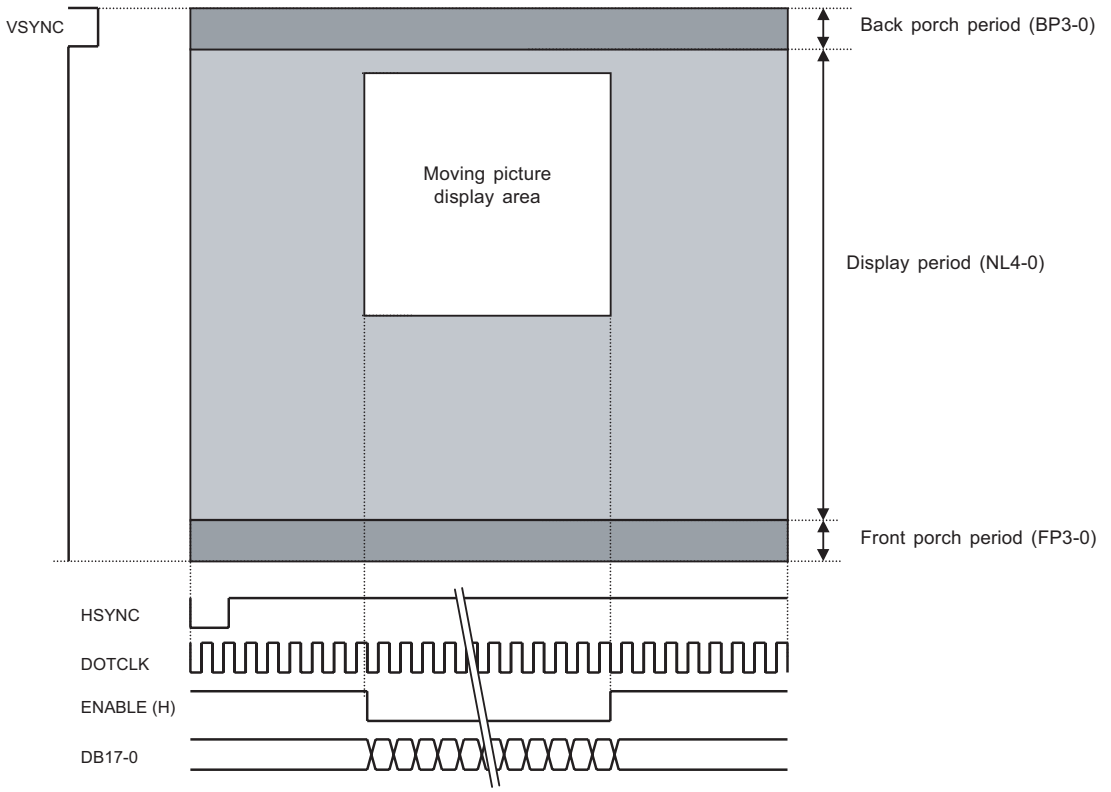


Figure 43

ENABLE signal function

The following table shows the relationship between the ENABLE, EPL setting and RAM access operation. ENABLE signal does not accompany address change in writing data although ENABLE must be “Low”. EPL controls the active polarity of ENABLE signal.

Table 60

EPL	ENABLE	RAM write	RAM address
0	0	Enable	Update
0	1	Disenable	Retain
1	0	Disenable	Retain
1	1	Enable	Update

RGB interface timing

Signal timing chart of 16/18-bit RGB interface

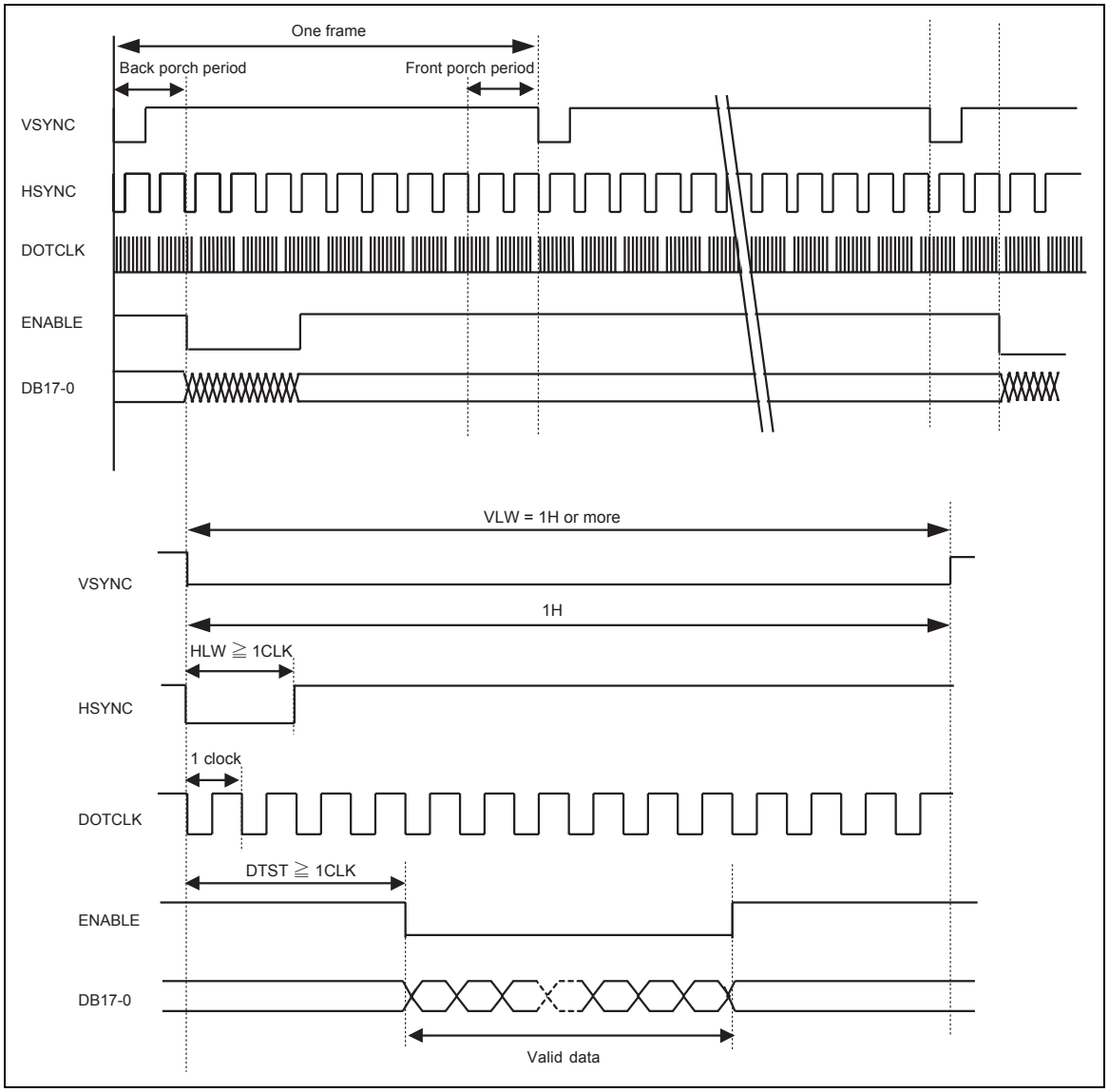


Figure 44

Notes: 1. VLW: VSYNC "Low" period
HLW: HSYNC "Low" period
DTST:data transfer setup time
2. Use high-speed write function (HWM = "1") when writing data via RGB interface.

Timing chart of signals in 6-bit RGB interface operation

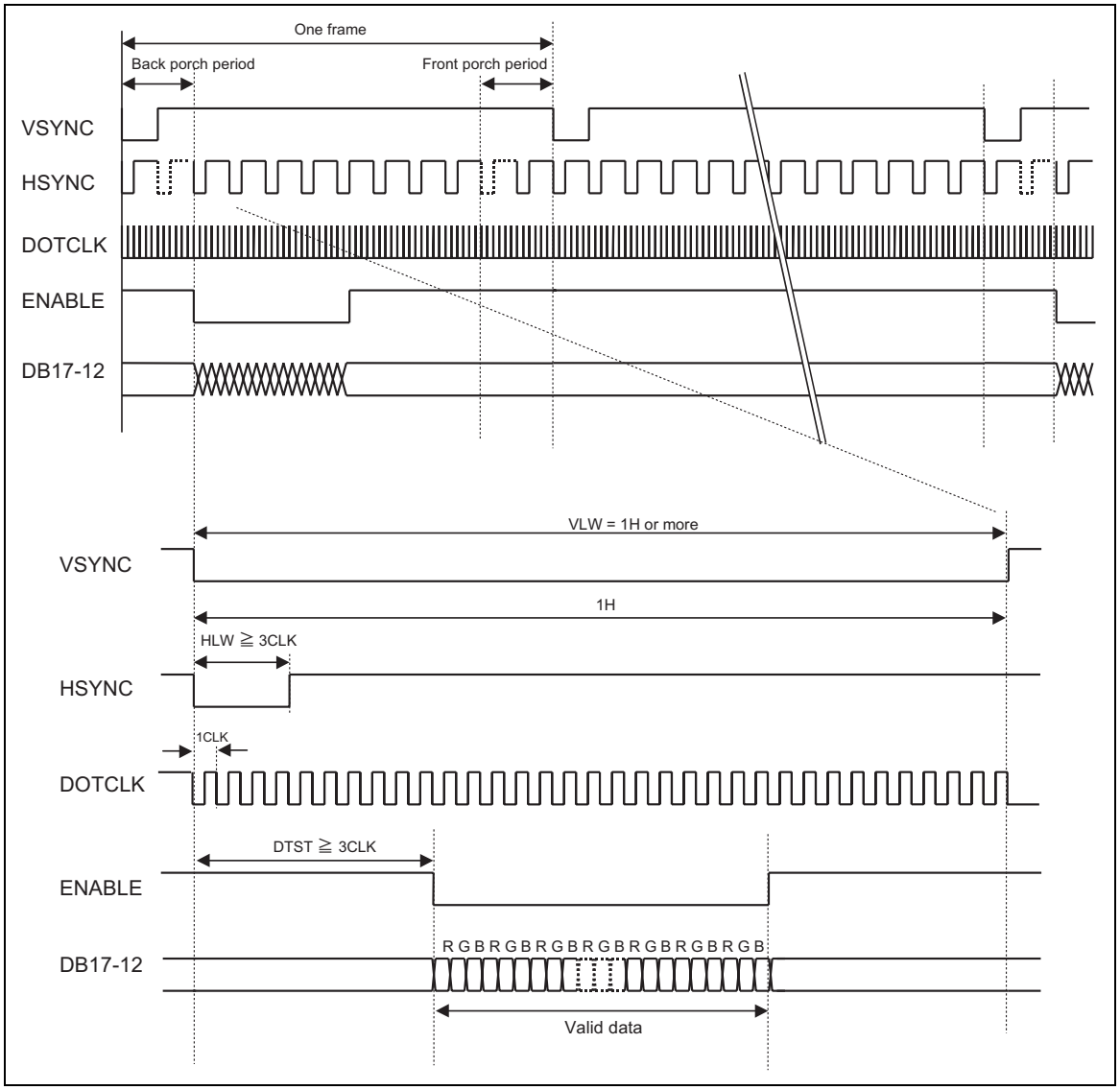


Figure 45

Notes: 1. VLW: VSYNC "Low" period
HLW: HSYNC "Low" period
DTST:data transfer setup time
2. Use high-speed write function (HWM = "1") when writing data via RGB interface.
3. In 6-bit RGB interface operation, set the cycles of VSYNC, HSYNC, ENABLE, DOTCLK so that one pixel data is transferred in units of three clocks via DB17-12.

Moving Picture Display via RGB Interface

The R61503U supports RGB interface for moving picture display and incorporates RAM for storing display data, which provides the following advantages in displaying a moving picture.

1. The window address function enables transferring data only within the moving picture area
2. The high-speed write function enables RAM access in high speed with low power consumption
3. It becomes possible to transfer only the data written over the moving picture area
4. By reducing data transfer, it can contribute to lowering the power consumption of the whole system
5. The data in still picture area (icons etc.) can be written over via system interface while displaying a moving picture via RGB interface

RAM access via system interface in RGB interface operation

The R61503U allows RAM access via system interface in RGB interface operation. In RGB interface operation, data is written to the internal RAM in synchronization with DOTCLK while ENABLE is “Low”. When writing data to the RAM via system interface, set ENABLE “High” to stop writing data via RGB interface. Then set RM = “0” to enable RAM access via system interface. When reverting to the RGB interface operation, wait for the read/write bus cycle time. Then, set RM = “1” and the index register to R22h to start accessing RAM via RGB interface. If there is a conflict between RAM accesses via two interfaces, there is no guarantee that the data is written in the RAM.

The following is an example of rewriting still picture data via system interface while displaying a moving picture via RGB interface.

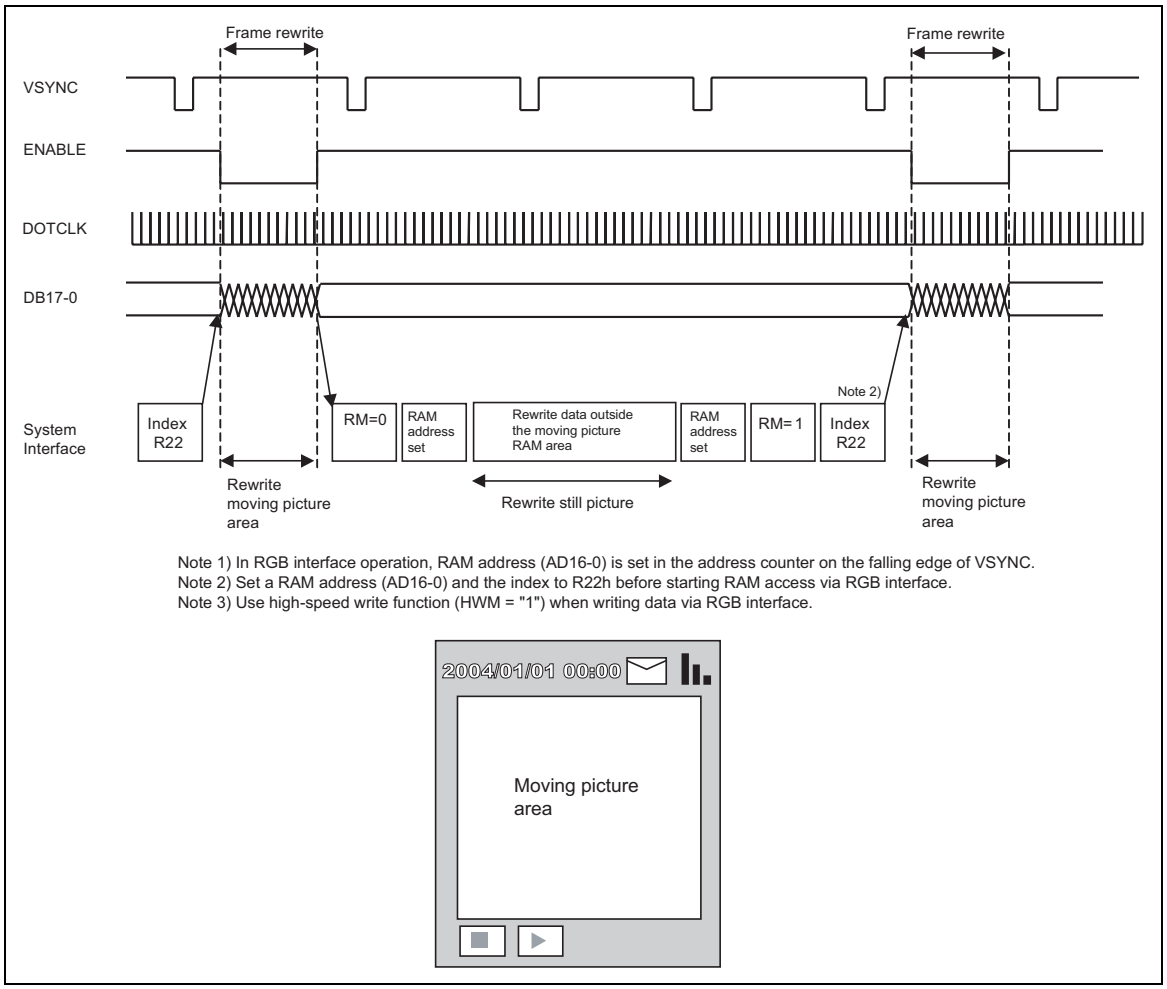


Figure 46 Updating a still picture area while displaying a moving picture

6-bit RGB interface

The 6-bit RGB interface is selected by setting the RIM1-0 bits to 10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 6-bit RGB data bus (DB17-12) while the data enable signal (ENABLE) allows RAM access via RGB interface. Unused pins (DB11 to 0) must be fixed at either IOVcc or GND level.

Instruction bits can be transferred only via system interface.

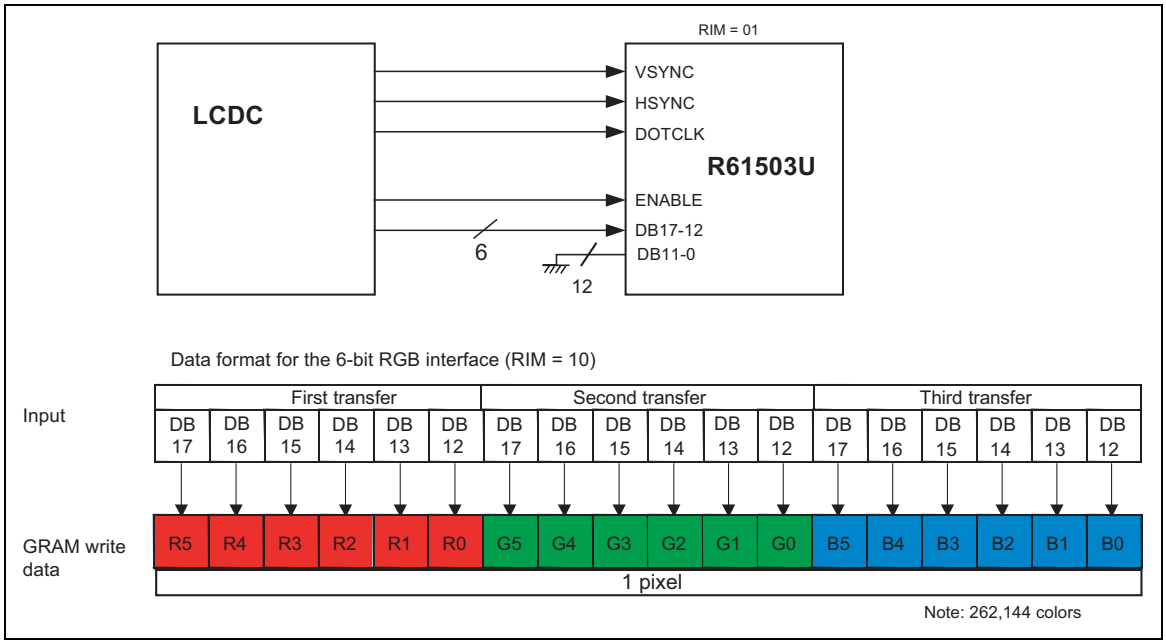


Figure 47 6-Bit RGB Interface and data format

Data transfer synchronization in 6-bit RGB interface operation

The R61503U has the counters, which count the first, second, third 6 bit transfers via 6-bit RBG interface. The counters are reset on the falling edge of VSYNC so that the data transfer will start from the first 6 bits of 18-bit RGB data from the next frame period. Accordingly, the data transfer via 6-bit interface can restart in correct order from the next frame period even if a mismatch occurs in transferring 6-bit data. This function can minimizes the effect from data transfer mismatch and help the display system return to normal display operation when data is transferred consecutively in moving picture operation.

Make sure the internal display operation within the R61503U is performed in units of pixels and input 3 DOTCLK to transfer one pixel data (RGB) via 6-bit interface. If the number of DOTCLK inputted in one frame period does not satisfy this condition, data transfer mismatch will occur and its effect will be carried over to the next frame.

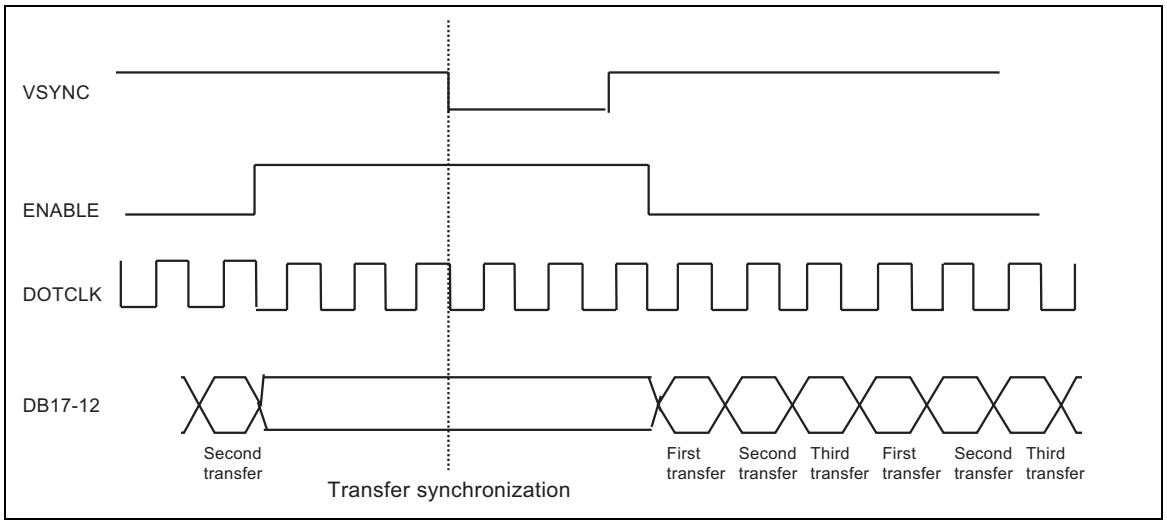


Figure 48 6-bit Transfer Synchronization

16-bit RGB interface

The 16-bit RGB interface is selected by setting the RIM1-0 bits to “01”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-10, DB8-1) while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

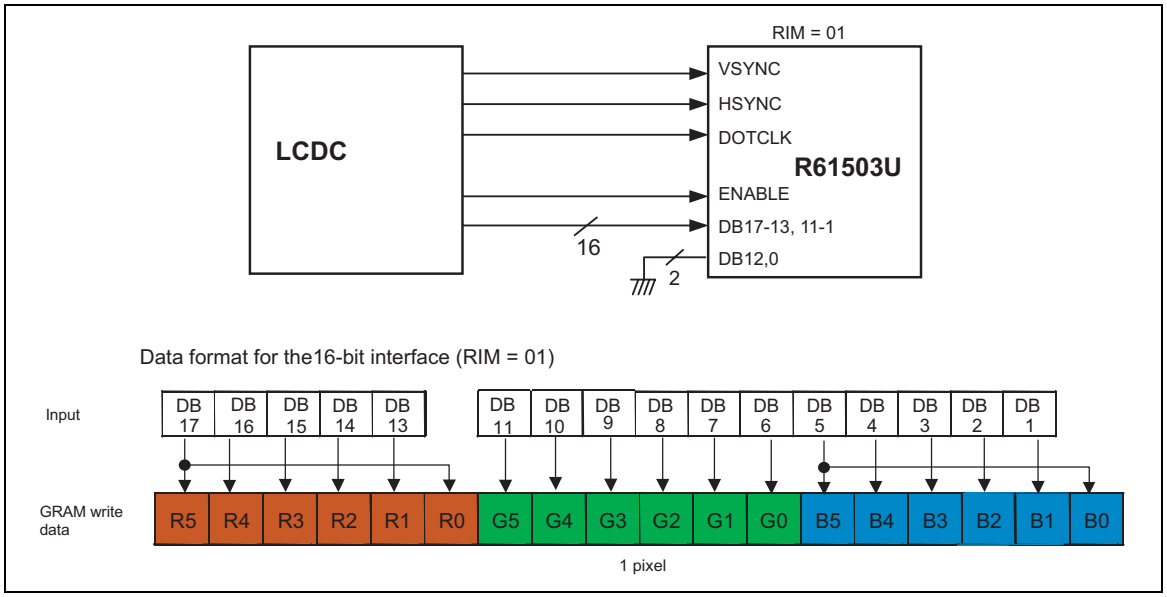


Figure 49 16-Bit RGB Interface and data format

18-bit RGB interface

The 18-bit RGB interface is selected by setting the RIM1-0 bits to “00”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB17-0) while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

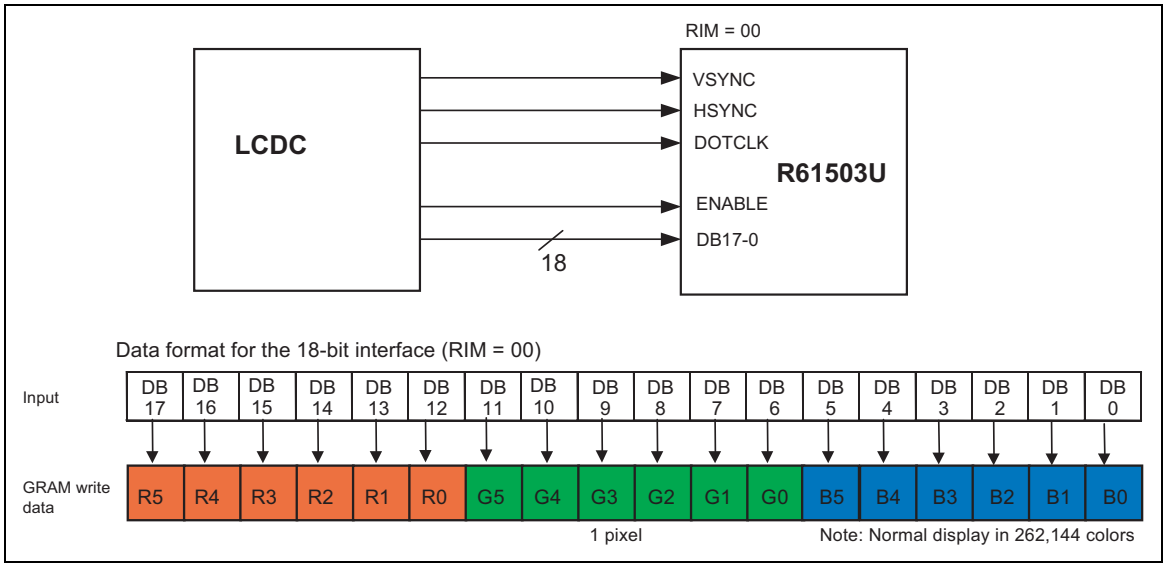


Figure 50 18-Bit RGB Interface and data format

Notes to external display interface operation

1. The following functions are not available in external display interface operation.

Table 61 Functions Not Available in External Display Interface operation

Function	External Display Interface	Internal Clock Operation
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied during display period.
3. The reference clock, which is used for determining the periods set by NOE[1:0], STDE[1:0] bits in RGB interface operation is DOTCLK, not the internal clock generated from the internal oscillator.
4. In 6-bit RGB interface operation, 6-bit dot data (R, G, and B) is transferred in synchronization with DOTCLK. In other words, it takes three DOTCLKs to transfer one pixel data.
5. In 6-bit RGB interface operation, make sure to set the cycles of VSYNC, HSYNC, DOTCLK, ENABLE signals so that the data transfer via DB17-12 is completed in units of pixels.
6. When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.
7. In RGB interface operation, a front porch period continues after the end of frame period until next VSYNC input is detected.
8. In RGB interface operation, use high-speed write function (HWM = 1) when writing data to GRAM.
9. In RGB interface operation, RAM address AD15-0 is set in the address counter every frame on the falling edge of VSYNC.

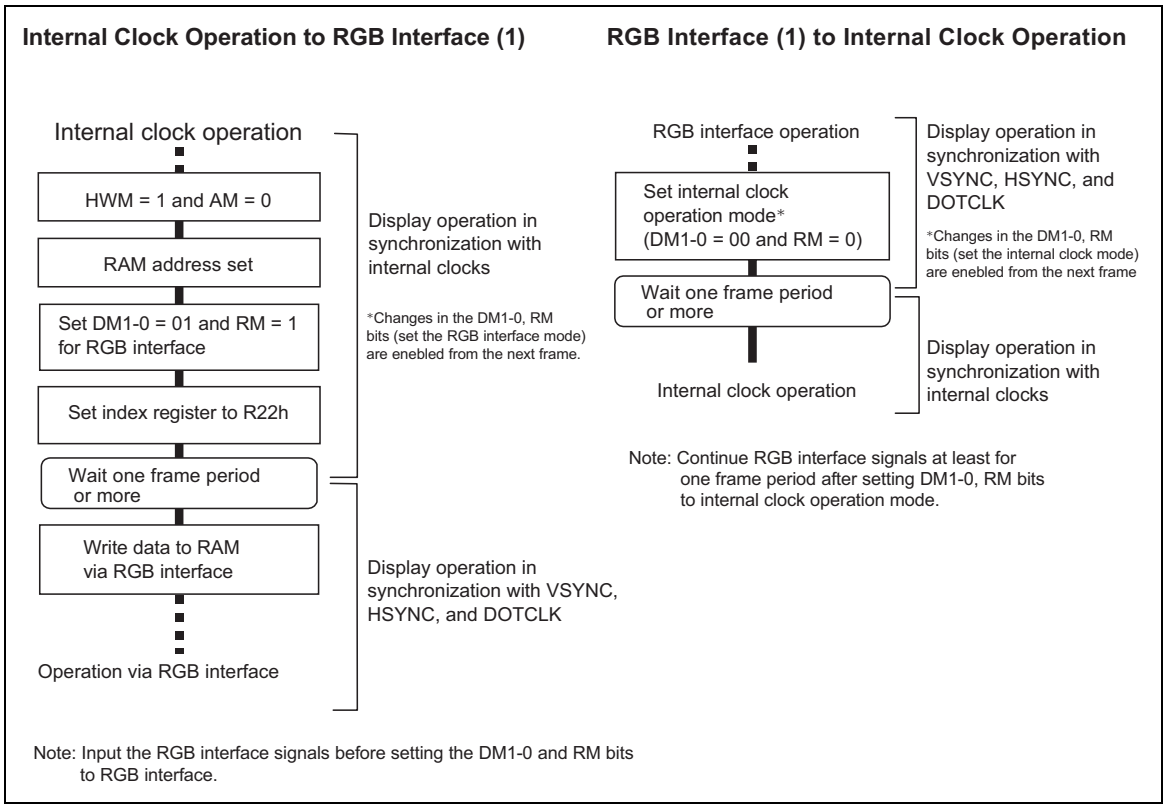


Figure 51 RGB interface operation and internal clock operation transition

RAM Address and Display Position on the Panel

The R61503U has memory to store the display data of 176RGB x 220 lines. The R61503U incorporates a circuit to control partial display, which allows switching the display driving mode between full-screen display mode and partial display mode.

The R61503U makes the display design setting and the panel driving position control setting separately and specifies the RAM area for each image displayed on the panel. For this reason, there is no need to take the mounting position of the panel into consideration when designing a display on the panel.

The following is the sequence of setting full-screen and partial display.

1. Set (PTSAx, PTEAx) to specify the RAM area for each partial image
2. Set the display position of each partial image on the base image by setting PTDPx.
3. Set NL to specify the number of lines to drive the liquid crystal panel to display the base image
4. After display ON, set display enable bits (BASEE, PTDE0/1) to display respective images

Normal display	BASEE = 1
Partial display	BASEE = 0, PTDE0/1 = 1

5. Change BASEE, PTDE0/1 setting to switch display modes (full-screen and partial display modes).

In driving the liquid crystal panel, the clock signal for gate line scan is supplied consecutively via interface in accordance with the number of lines to drive the liquid crystal panel (NL setting).

When switching the display position in horizontal direction, set SS bit when writing RAM data.

Table 62

	Display ENABLE	Numbers of lines	RAM area
Base image	BASEE	NL	(BSA, BEA) = (8'h00, 8'hDB)

Notes 1: The base image is displayed from the first line of the panel.

2: Make sure NL ≤ 220 (lines) = BEA – BSA when setting a base image RAM area. BSA and BEA are fixed to 8'h00, 8'hDB, respectively.

Table 63

	Display ENABLE	Display position	RAM area
Partial image 1	PTDE0	PTDP0	(PTSA0, PTEA0)
Partial image 2	PTDE1	PTDP1	(PTSA1, PTEA1)

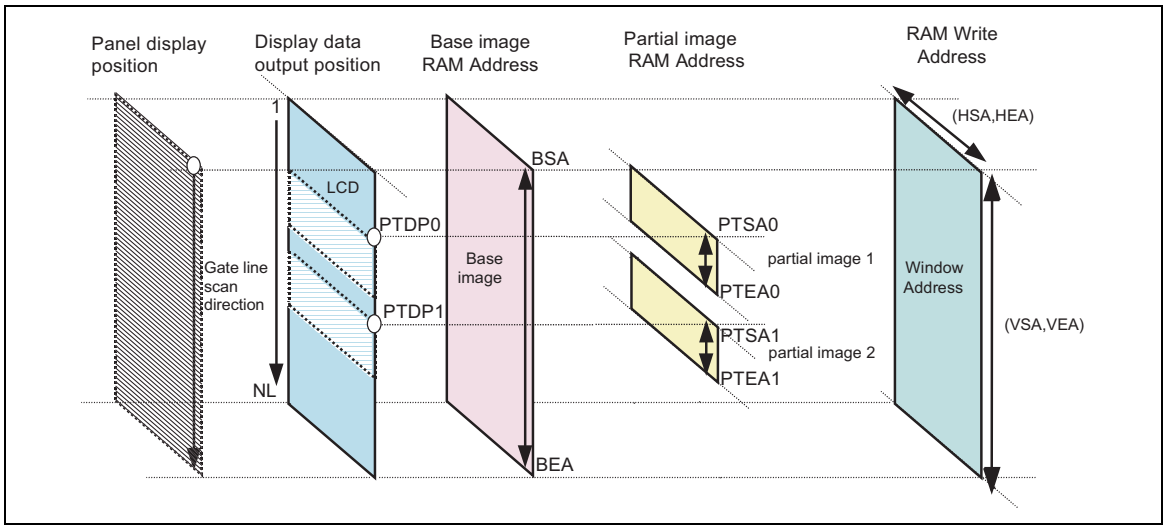


Figure 52 RAM Address, display position and drive position

Restrictions in setting display control instruction

Partial image display

Set the partial image RAM area setting registers (PTSAx, PTEAx bits) and the partial position setting registers (PTDPx bits) so that the RAM areas and the display positions of partial images do not overlap one another.

$$0 \leq \text{PTDP0} \leq \text{PTDP0} + (\text{PTEA0} - \text{PTSA0}) < \text{PTDP1} \leq \text{PTDP1} + (\text{PTEA1} - \text{PTSA1}) \leq \text{NL}$$

The following figure shows the relationship among the RAM address, display position, and the lines driven for the display.

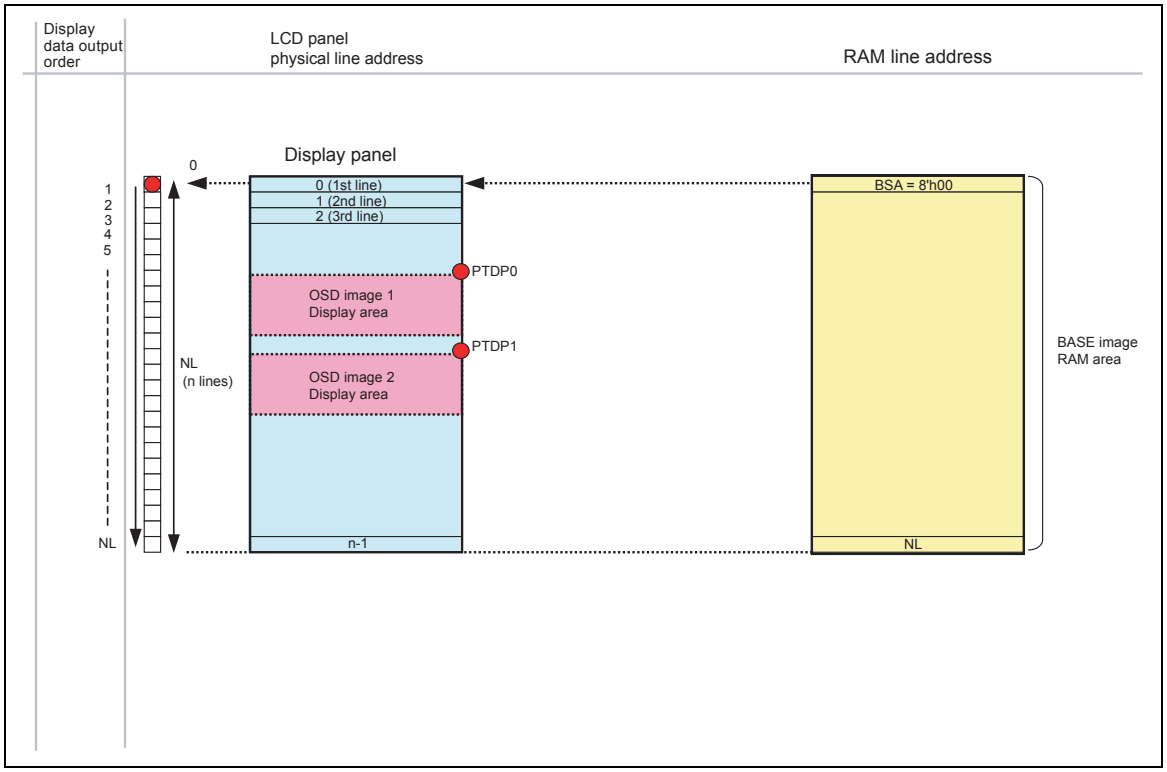


Figure 53 Display RAM Address and Panel Display Position

Note: This figure shows the relationship between RAM line address and the display position on the panel. In the R61503U's internal operation, the data is written in the RAM area specified by the window address setting (HEA/HSA[7:0], VEA/VES[8:0]).

Instruction setting example

The followings are examples of display design setting for 176(RGB) x 220(lines) panels.

1. Full screen display (no partial)

The following is an example of full screen display setting.

Table 64

Base image display instruction	
BASEE	1
NL[4:0]	5'h14

PTDE0	0
PTDE1	0

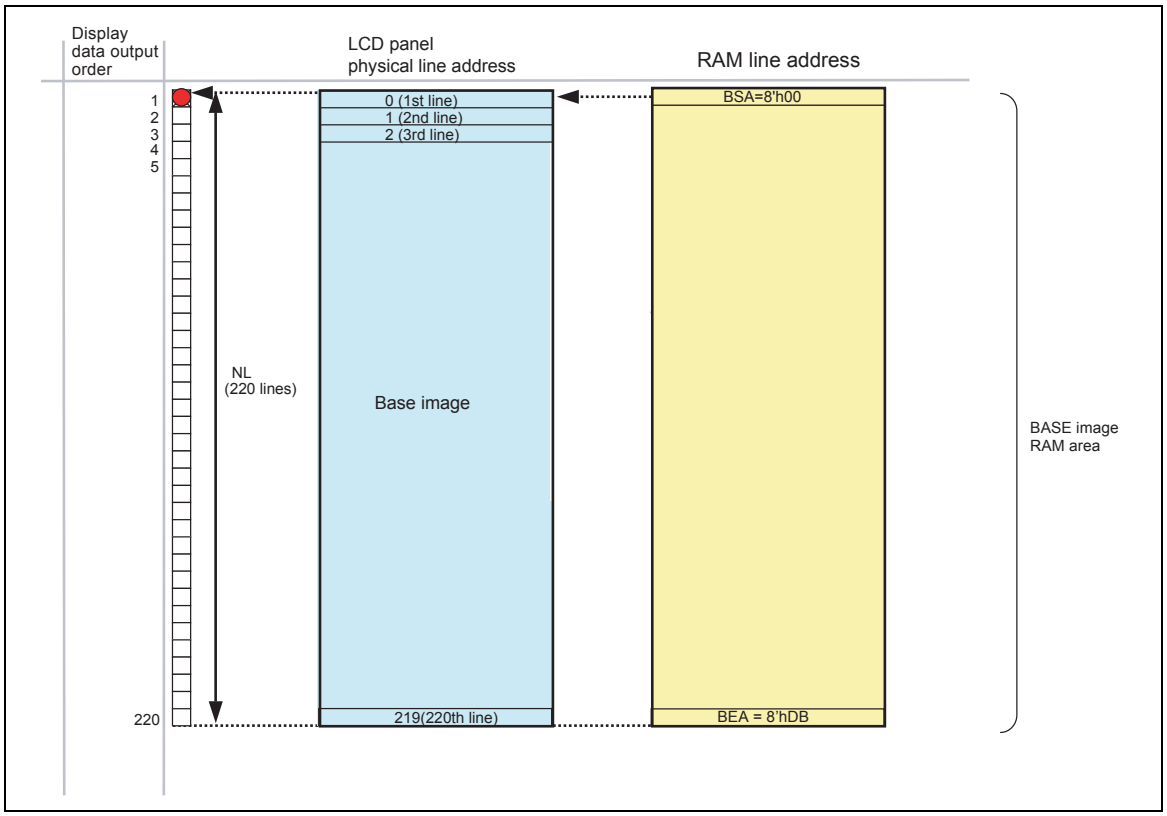


Figure 54 Full Screen Display (No Partial)

2. Partial only

The following is an example of setting for partial image 1 only and turning off the base image. The partial image 1 is displayed at the position specified by PTDP0 bit.

Table 65

Base image display instruction	
BASEE	0
NL[4:0]	5'h14

partial image 1 display instruction	
PTDE0	1
PTSA0[7:0]	8'h00
PTEA0[7:0]	8'h0F
PTDP0[7:0]	8'h80

partial image 2 display instruction	
PTDE1	0
PTSA1[7:0]	8'h00
PTEA1[7:0]	8'h00
PTDP1[7:0]	8'h00

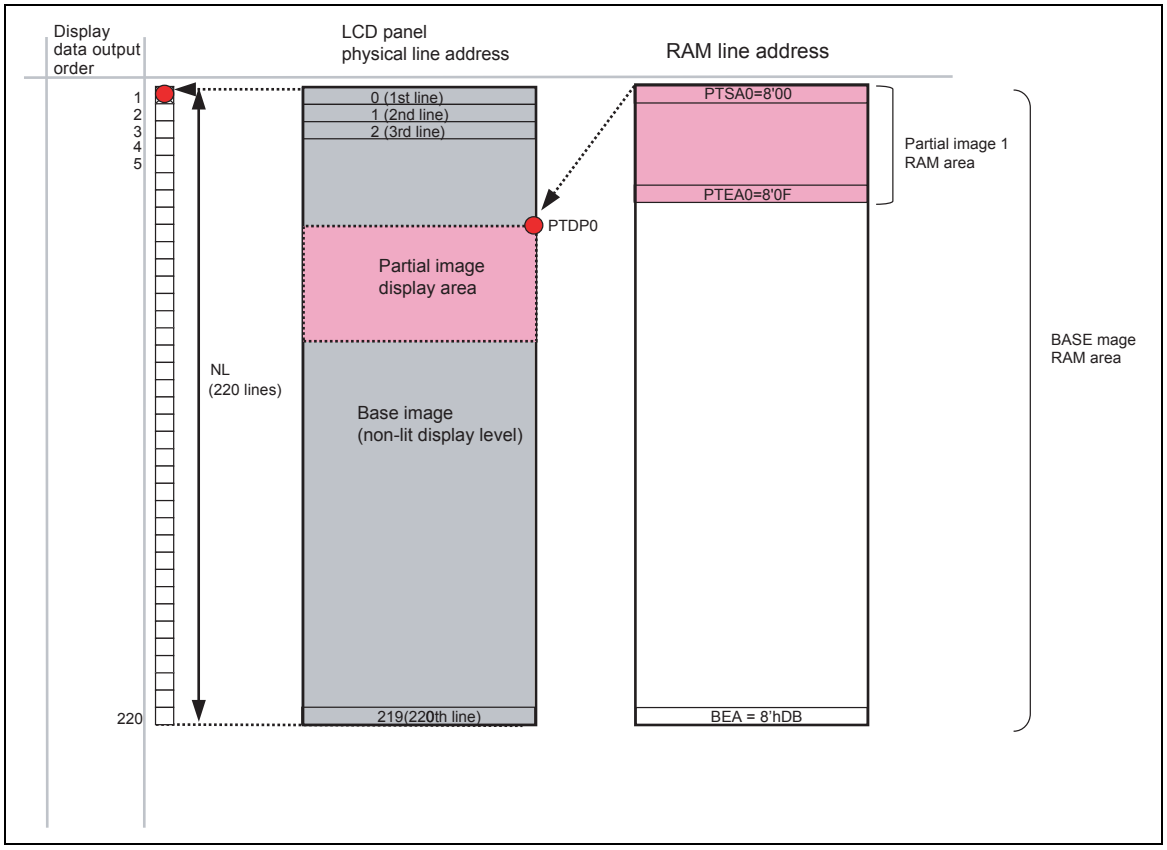


Figure 55 Partial display

High-Speed RAM Write Function

The R61503U supports high-speed RAM write function to write data to each line of window address area at a time. This function makes the R61503U available with the applications, which require high-speed, low-power-consumption data write operation such as color moving picture display.

When enabling high-speed RAM write function (HWM = "1"), the data is first stored in the internal register of the R61503U in order to rewrite the RAM data in each horizontal line of the window address area at a time. Also, when transferring the data from the internal register to the internal RAM, the data written in the next line of the window address area can be transferred to the internal register of the R61503U. The high-speed write function minimizes the number of RAM access in write operation and enables high-speed consecutive RAM write operation required for moving picture display with low power consumption.

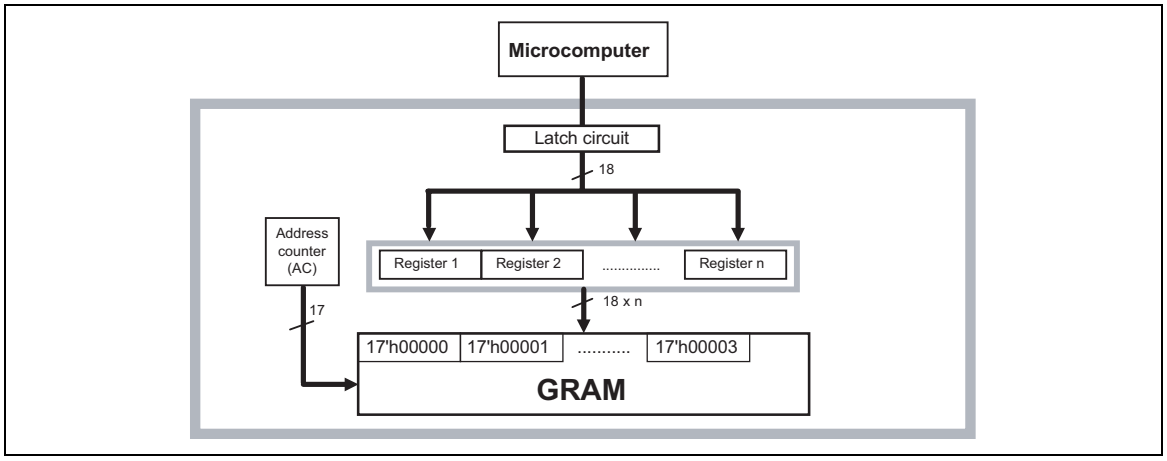


Figure 56 High-speed RAM Write Operation

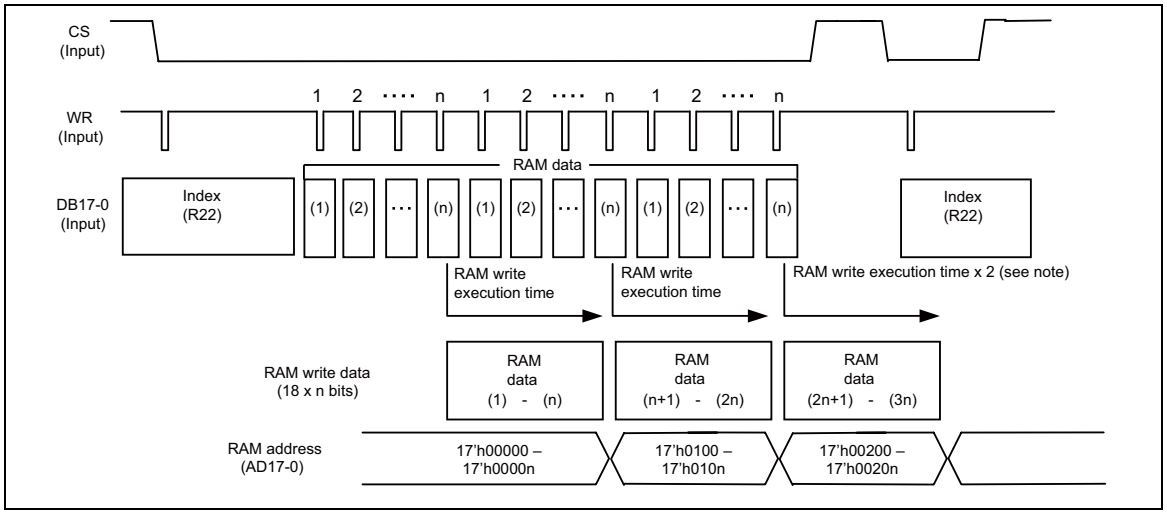


Figure 57 High-speed RAM Write Operation Timing Relationship

Note: When switching from high-speed RAM write operation to index write operation, wait at least for 2 bus cycle periods (2 x t_{cycw}) for normal RAM write operation before executing next instruction.

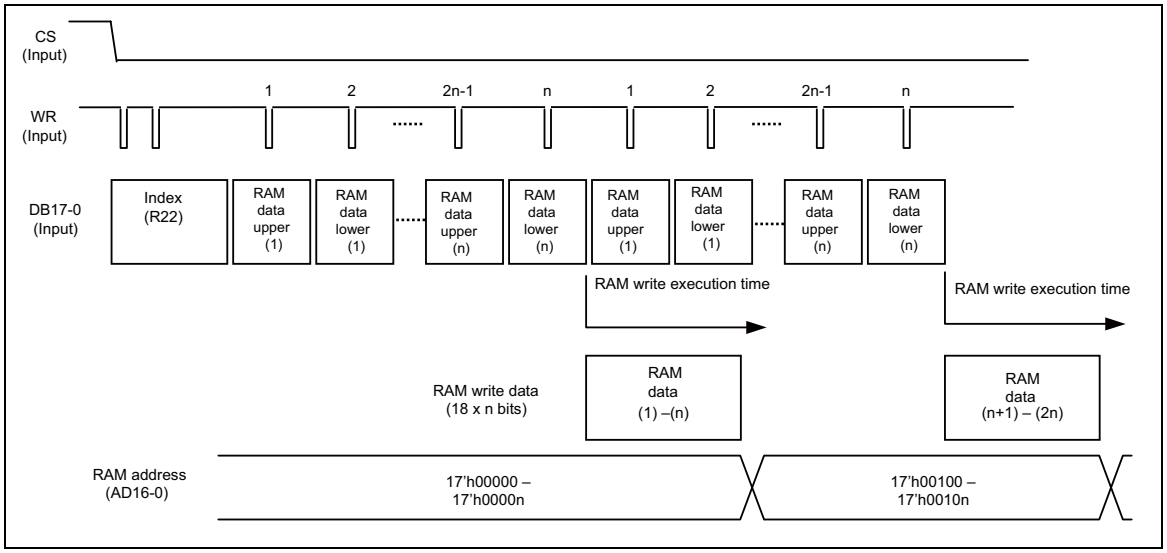


Figure 58 High-speed RAM Write Operation via 9-bit Interface

Note: In high-speed RAM write operation, the R61503U writes data in units of n words. When using 9-bit interface, the R61503U performs write operation 2 x n times in the internal register before writing the data in each line of the window address area.

Notes to high-speed RAM write function

1. In high-speed RAM write mode, the R61503U performs write operation to the internal RAM in units of lines. If the data inputted to the internal write register is not enough to rewrite the data in the horizontal line of the window address area, the data is not written correctly in that line address.

2. If the IR is set to 22h when HWM = "1", the R61503U always performs RAM write operation. With this setting, the R61503U does not perform RAM read operation. Make sure to set HWM = 0, when performing RAM read operation.

3. The high-speed RAM write function cannot be used when writing data in normal RAM write function mode. When switching form one write mode to the other, change the mode first and set AD16-0 (RAM address set) before starting write operation.

Table 66

	Normal RAM Write (HWM=0)	High-Speed RAM Write (HWM=1)
BGR function	Available	Available
RAM address set	In units of words	In units of words
RAM read	In units of words	Not Available
RAM write	In units of words	In units of horizontal lines
Window address	In units of words (minimum window address area: 1 word x 1 line)	In units of words (minimum window address area: 8 words x 1 line)
AM	AM = 1/0	AM = 0

High-speed RAM data write in a window address area

The R61503U can perform consecutive high-speed data rewrite operation within a rectangular area (minimum: 8 words x 1 line) made in the internal RAM with the following settings.

When writing data to the internal RAM using high-speed RAM write function, make sure each line of the window address area is overwritten at a time. If the data buffered in the internal register of the R61503U is not enough to overwrite the horizontal line in the window address area, the data is not written correctly in that line.

The following is an example of writing data in the window address area using high-speed write function when a window address area is made by setting HSA = 8'h12, HEA = 8'hA7, VSA = 9'h020, VEA = 9'h05B.

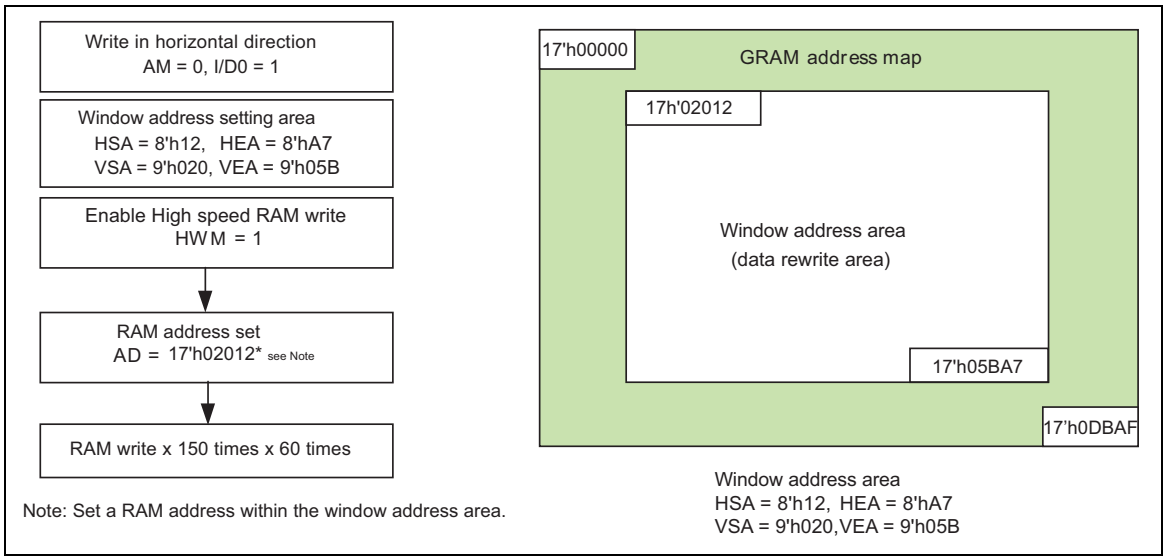


Figure 59

Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made in the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of RAM address (either increment or decrement, horizontal or vertical, respectively). Setting these bits enables the R61503U to write data including image data consecutively without taking the data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

[Window address area]
(horizontal direction) 8'h00 ≤ HSA ≤ HEA ≤ 8'hAF
(vertical direction) 9'h000 ≤ VSA ≤ VEA ≤ 9'h0DB

[RAM address (AD16-0)]
(RAM address) HSA ≤ AD7-0 ≤ HEA
VSA ≤ AD16-8 ≤ VEA

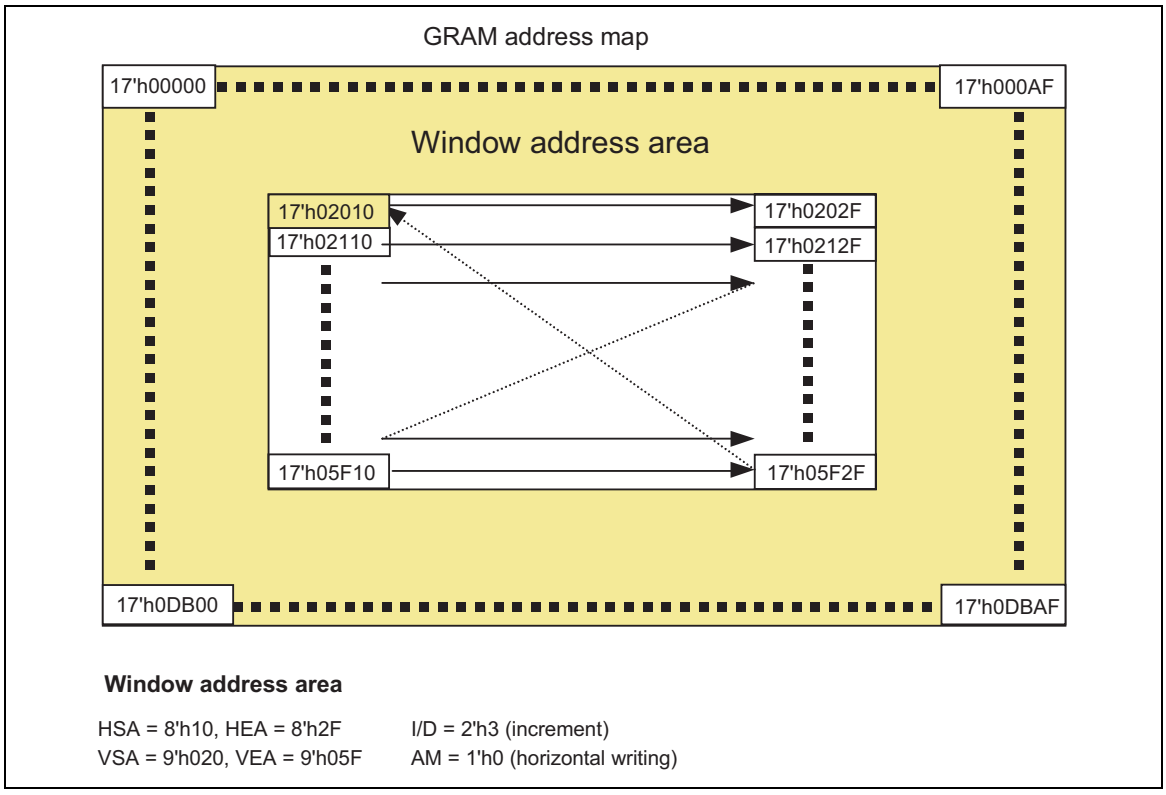
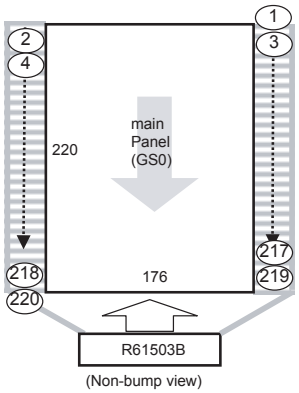
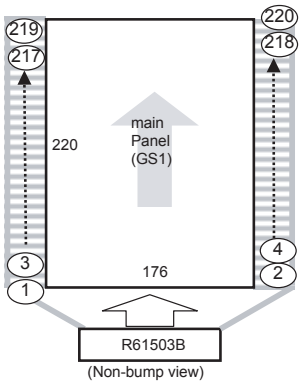


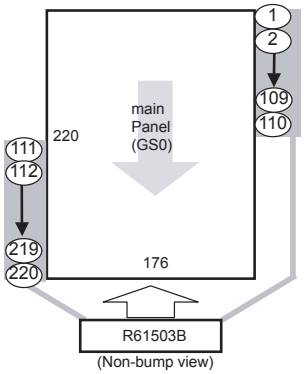
Figure 60 Automatic Address Update within a Window Address Area

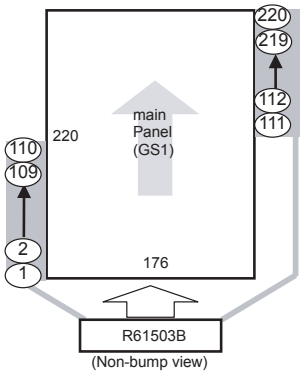
Scan Mode Setting

The R61503U allows for changing the gate-line/gate driver assignment and the shift direction of gate line scan in the following 4 different ways by combination of SM and GS bit settings. These combinations allow various connections between the R61503U and the LCD panel.

<table>
<tr><th>SM</th><th>Scan direction</th></tr>
<tr><td>0</td><td>
Interchanging forward direction (GS = 0)


Scan order (Gate line No.)
G1⇒G2⇒G3⇒G4... G217⇒G218⇒G219⇒G220
</td><td>
Interchanging backward direction (GS = 1)


Scan order (Gate line No.)
G220⇒G219⇒G218⇒G217... G4⇒G3⇒G2⇒G0
</td></tr>
<tr><td>1</td><td>
Left/right forward direction (GS = 0)


Scan order (Gate line No.)
G1⇒G3...G217⇒G219⇒G2⇒G4...G218⇒G220
</td><td>
Left/right backward direction (GS = 1)


Scan order (Gate line No.)
G220⇒G218... G4⇒G2⇒G219⇒G217... G3⇒G1
</td></tr>
</table>

Note: The numbers in the circles in the figure show the order of scan.

Figure 61

8-color Display Mode

The R61503U has a function to display in eight colors. In this display mode, only V0 and V31 are used and power supplies to other grayscales (V1 to V30) are turned off to reduce power consumption.

In 8-color display mode, the γ-adjustment registers P0KP0-P0KP5, P0KN0-P0KN5, P0RP0, P0RP1, P0RN0, P0RN1 are disabled and the power supplies to V1 to V30 are halted. The R61503U does not require GRAM data rewrite for 8-color display by writing the MSB to the rest in each dot data to display in 8 colors.

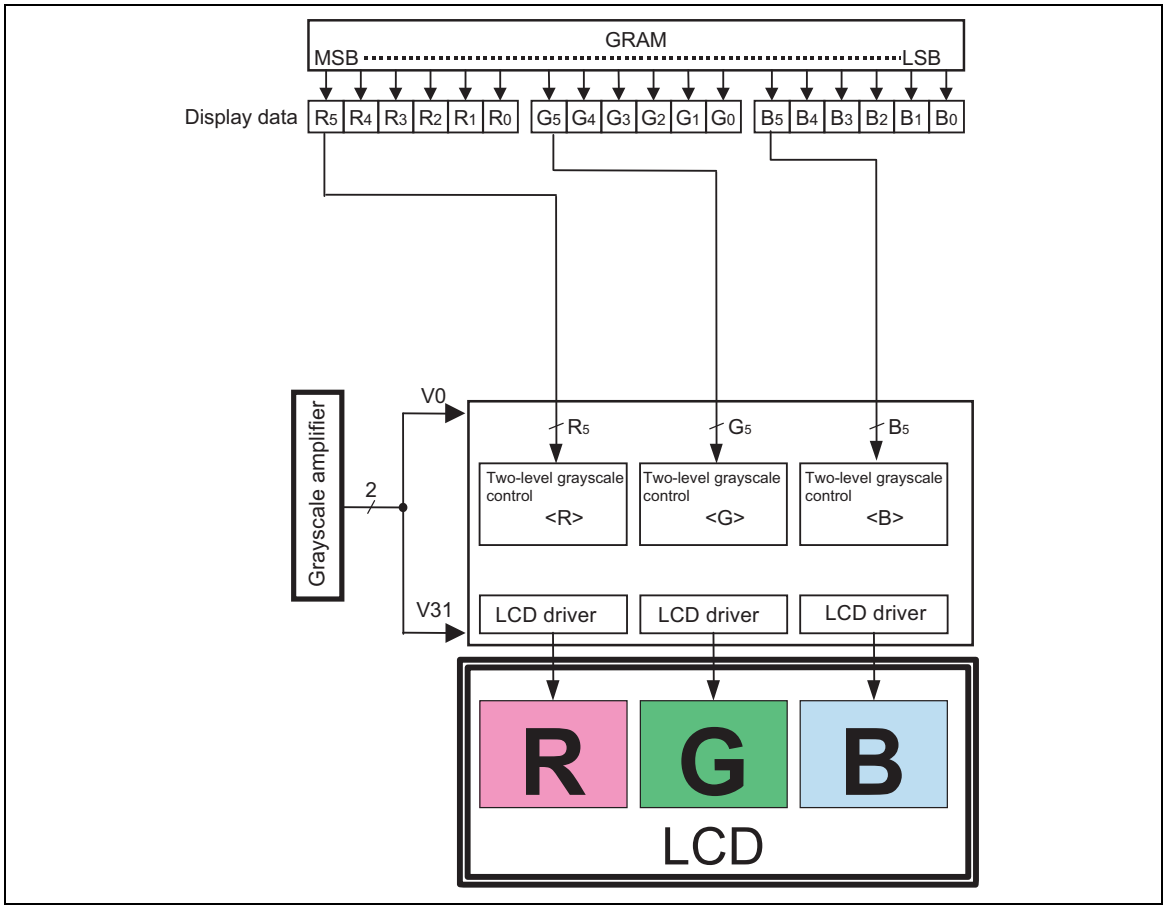
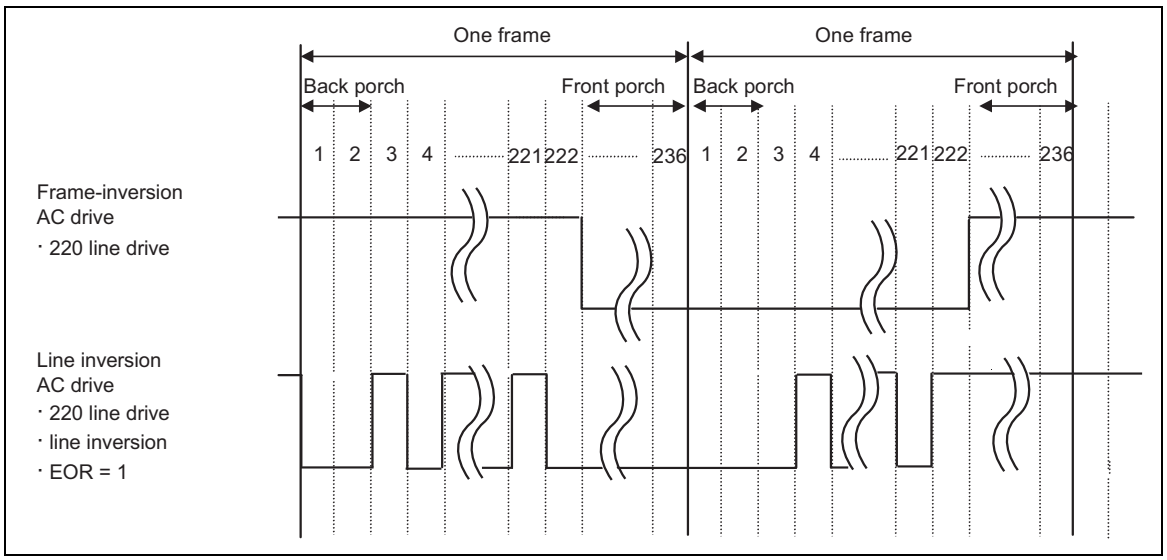


Figure 62

n-line Inversion AC Drive

The R61503U, in addition to the frame-inversion liquid crystal alternating current drive, supports the n-line inversion alternating current drive to invert the polarity of liquid crystal in every n-line periods, where n takes a number from 1 to 64. The n-line inversion can provide a solution when there is a need to improve the display quality.



Notes: 1. Make sure to set EOR = "1" to prevent direct bias on liquid crystal when selecting n-line inversion drive.

2. The n-line inversion is halted in blank period (back, front porch periods) and restarted at the first line of the display area.

Figure 63

Alternating Timing

The following figure illustrates the liquid crystal polarity inversion timing in different LCD driving methods. In case of frame-inversion AC drive, the polarity is inverted as the R61503U draws one frame, which is followed by a blank period lasting for (BP+FP) periods. In case of n-line inversion AC drive, polarity is inverted as the R61503U draws n line, and a blank period lasting for (BP+FP) periods is inserted when the R61503U draws one frame.

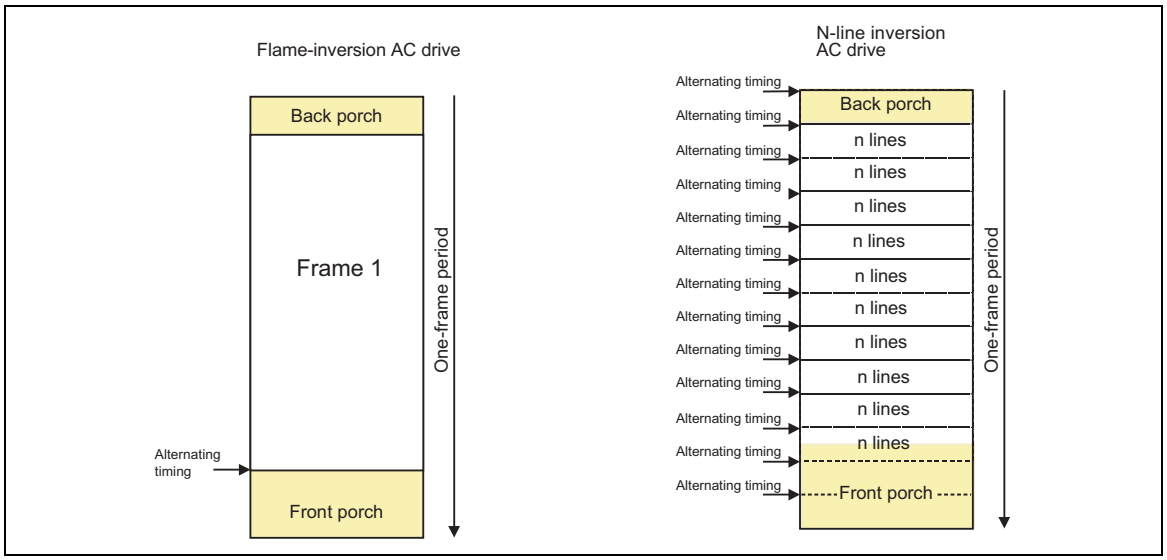


Figure 64

Frame-Frequency Adjustment Function

The R61503U supports a function to adjust frame frequency. The frame frequency for driving liquid crystal can be adjusted by setting the DIVI, RTNI bits without changing the oscillation frequency.

The R61503U allows changing the frame frequency depending on whether moving picture or still picture is displayed on the screen. In this case, set a high oscillation frequency. By changing the DIVI and RTNI settings, the R61503U can operate at high frame frequency when displaying a moving picture, which requires the R61503U to rewrite data in high speed, and it can operate at low frame frequency when displaying a still picture.

Relationship between liquid crystal drive duty and frame frequency

The following equation represent the relationship between liquid crystal drive duty and frame frequency. The frame frequency can be changed by setting the 1H period adjustment bit (RTNI) and the operation clock frequency division ratio setting bit (DIVI).

(Formula to calculate frame frequency)

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per line} \times \text{division ratio} \times (\text{Line+BP+FP})} \quad [\text{Hz}]$$

fosc: RC oscillation frequency
Line: number of lines to drive a panel (NL bits)
Clock cycles per line: RTNI bits
Division ratio: DIVI bits
Number of lines for front porch: FP
Number of lines for back porch: BP

Example of Calculation: when maximum frame frequency = 60 Hz

Number of lines to drive a panel: 220 lines
1H period: 16 clock cycles (RTNI3-0 = “0000”)
Operation clock division ratio: 1/1
Front porch (FP): 2 line periods
Back porch (BP): 14 line periods

$$\text{fosc} = 60\ (\text{Hz}) \times (0+16)\ (\text{clocks}) \times 1/1 \times (220 + 16)\ (\text{lines}) = 226\ (\text{kHz})$$

In this case, the RC oscillation frequency is 226kHz. Adjust the external resistor connected to the internal RC oscillator to set the frequency to 226kHz.

Partial Display Function

The partial display function allows the R61503U to drive lines selectively to display partial images by setting partial display control registers. The lines not used for displaying partial images are driven at non-lit display level to reduce power consumption.

The power efficiency can be enhanced in combination with 8-color display mode. Check the display quality when using low power consumption functions.

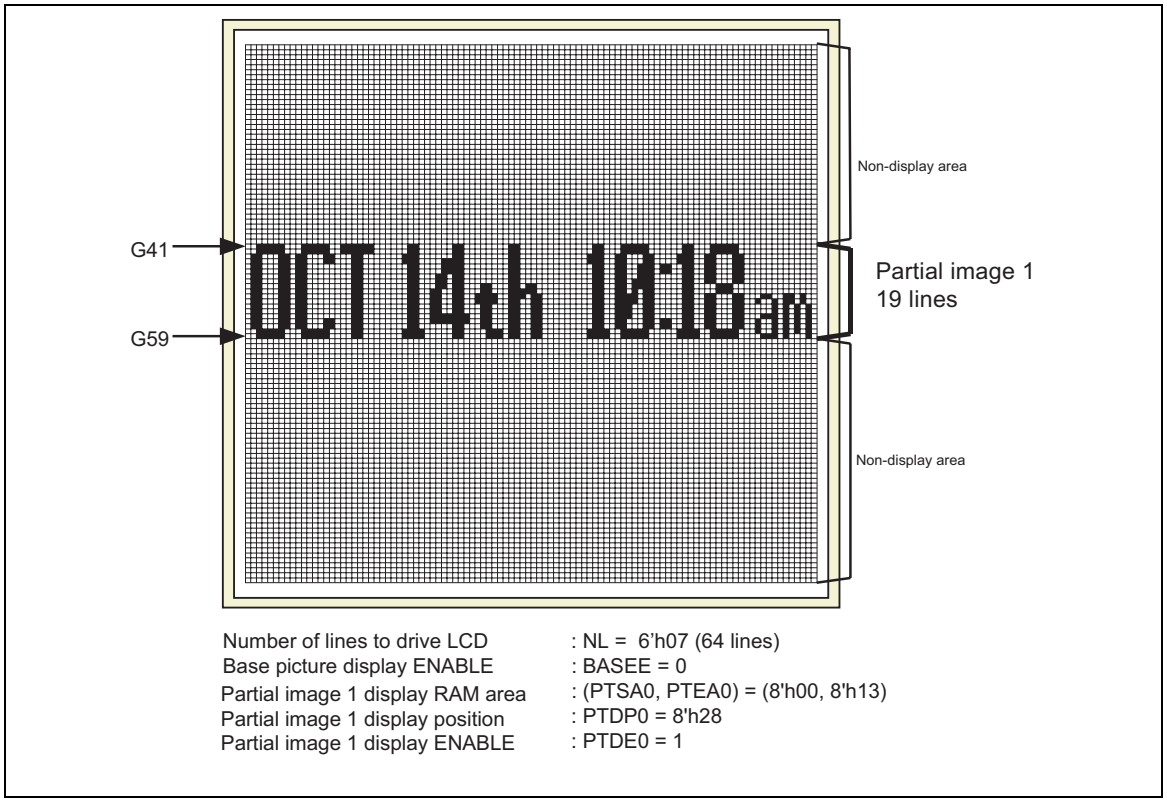


Figure 65

Note: See the "RAM Address and Display Position on the Panel" for details on the relationship between the display position on the panel and the RAM area setting for partial image.

Low power consumption drive settings

The R61503U supports the following low power consumption drive methods to drive the panel with less power requirement. Generally, there is a trade-off between power efficiency and quality of display. Also, the power efficiency depends on the characteristics of the panel. Check which of the following methods can achieve the optimal balance between power consumption and display quality.

1. 8-color display mode (COL)

In this mode (CL = "1"), the R61503U halts grayscale voltage generation except for V0 and V31. In this mode, the R61503U display in 8 colors to save power.

2. Partial display

In this mode, the data is displayed as partial image and the base image is turned off (BASEE = 0). The normal display operation is limited to the partial display area to save power.

The source output level in non-display area can be changed by instruction (PTS[2:0]). By setting PTS[2:0], it becomes possible to halt the amplifiers for generating grayscale voltage except for V0 and V31 and slow down the clock frequency for step-up operation to half the normal frequency.

Table 67 Source outputs in non-display area

PTS[2:0]	Source output in non-display area		Non-display area	Non-display area
	Positive polarity	Negative polarity	Grayscale amp operation	Step-up clock frequency
3'h0	V31	V0	V0 to V31	Set by DC0, DC1 bits
3'h1	Setting disabled	Setting disabled	-	-
3'h2	GND	GND	V0 to V31	Set by DC0, DC1 bits
3'h3	Hi-Z	Hi-Z	V0 to V31	Set by DC0, DC1 bits
3'h4	V31	V0	V0, V31	1/2 the frequency set by DC0, DC1 bits
3'h5	Setting disabled	Setting disabled	-	-
3'h6	GND	GND	V0, V31	1/2 the frequency set by DC0, DC1 bits
3'h7	Hi-Z	Hi-Z	V0, V31	1/2 the frequency set by DC0, DC1 bits

See also "Partial Display Function" for details.

3. Frame frequency setting

The R61503U allows changing the liquid crystal polarity inversion cycle by changing the frame frequency by setting DIVI, RTNI bits. To improve power efficiency, set a lower frequency in partial display operation, which requires small power consumption. See also “Frame-Frequency Adjustment Function” for details.

Generally, there is a trade-off between power efficiency and quality of display. The power efficiency also depends on the characteristics of the panel. Check the optimal balance between the quality of display on the panel and the power efficiency before use.

4. Liquid crystal inversion drive

The R61503U allows selecting liquid crystal inversion drive method from frame-inversion AC drive or line-inversion AC drive by setting B/C, NW bits. Select the optimal driving method according to the state of display. Also, see “n-line Inversion AC Drive” for details.

Generally, there is a trade-off between the power efficiency and the quality of display. The power efficiency also depends on the characteristics of the panel. Check the quality of display before use.

5. Optimizing step-up factor

There are cases that power loss in driving liquid crystal can be minimized by optimizing the step-up factor. Whether this method proves to be power-efficient or not depends on the characteristics of the liquid crystal panel. The step-up factor is set by BT[2:0].

LCD panel interface timing

The following are the relationships between RGB interface signals and LCD panel signals when the display operation is synchronized with the internal clock signal and RGB interface signals respectively.

Internal clock operation

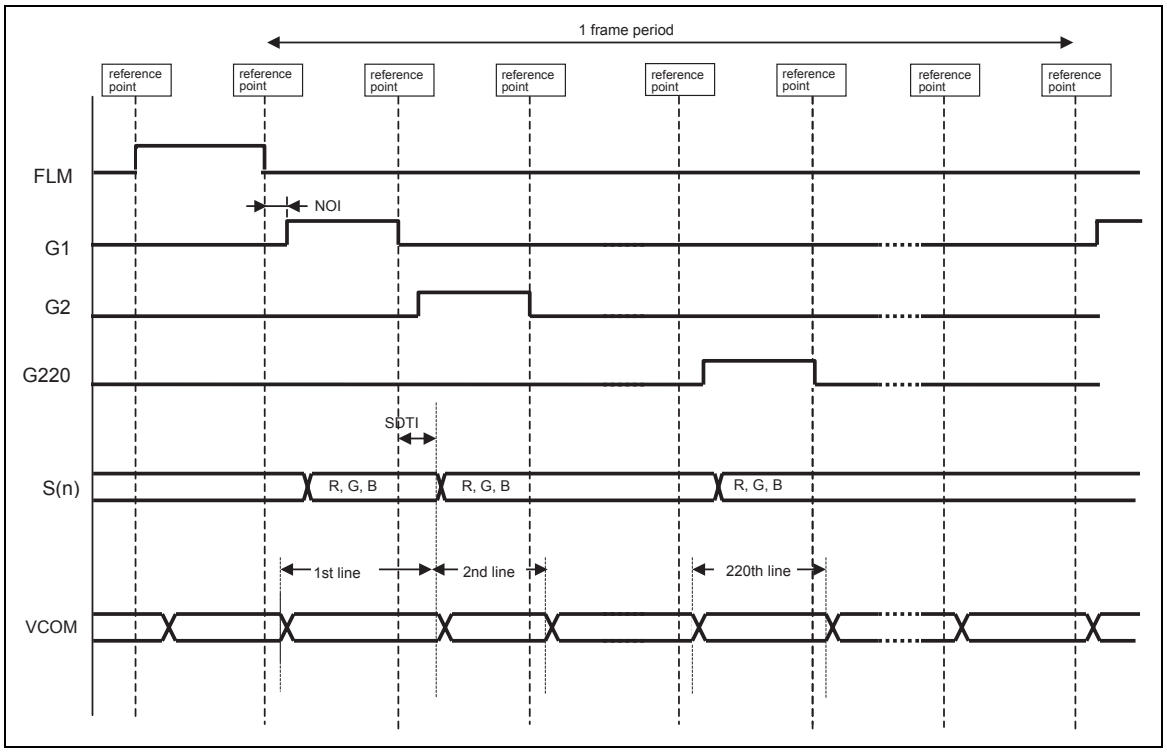


Figure 66

RGB interface signals

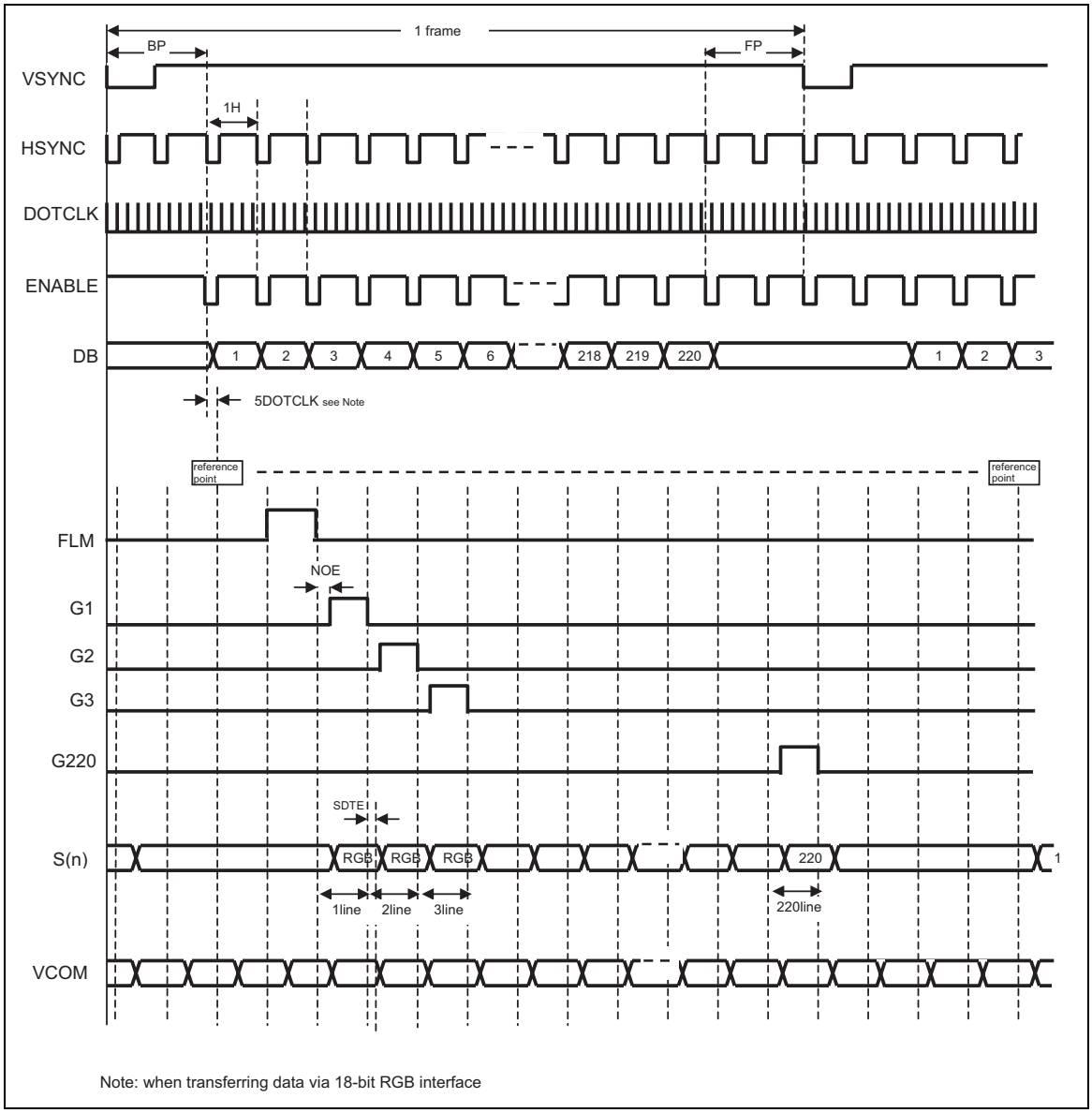


Figure 67

Oscillator

The R61503U generates RC oscillation using the internal RC oscillator to which an external oscillation resistor is connected between the OSC1 and OSC2 pins. The oscillation frequency varies depending on the value of external resistor, wiring length, operating power supply voltage. For example, the oscillation frequency can be lowered by connecting an external resistor of a larger resistance, or lowering supply voltage. See "Notes to electrical characteristics" for details on the relationship between Rf resistance and oscillation frequency (OSC).

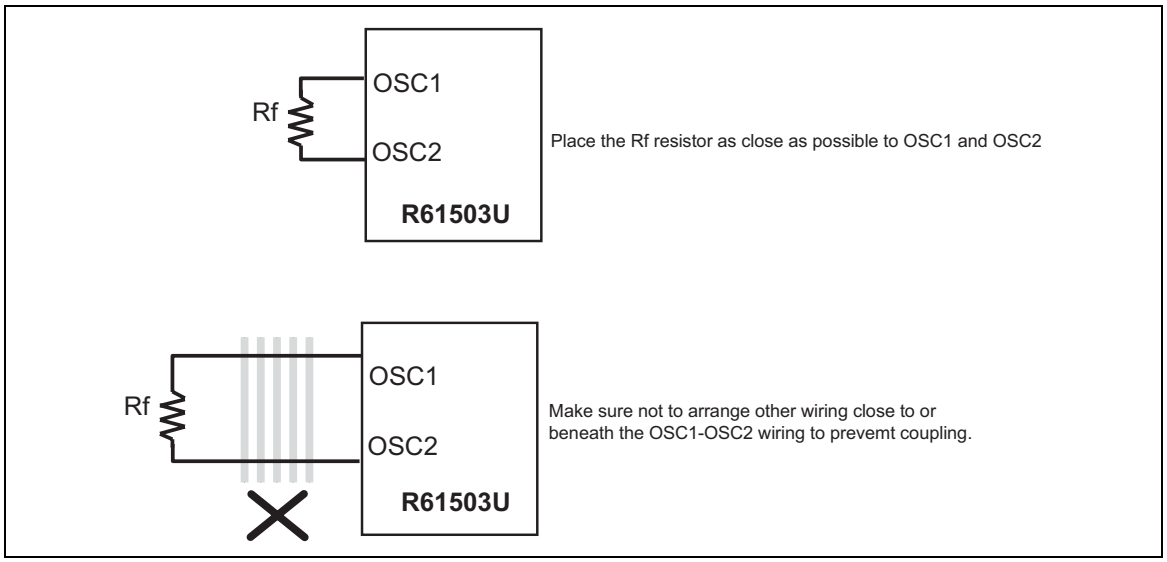


Figure 68

γ Correction function

The R61503U supports γ-correction function to display in 262,144 colors simultaneously using gradient-adjustment, amplitude-adjustment, fine-adjustment registers. Each register consists of positive-polarity register and negative-polarity register to allow different settings for positive and negative polarities and make the optimal gamma correction setting for the characteristics of the panel.

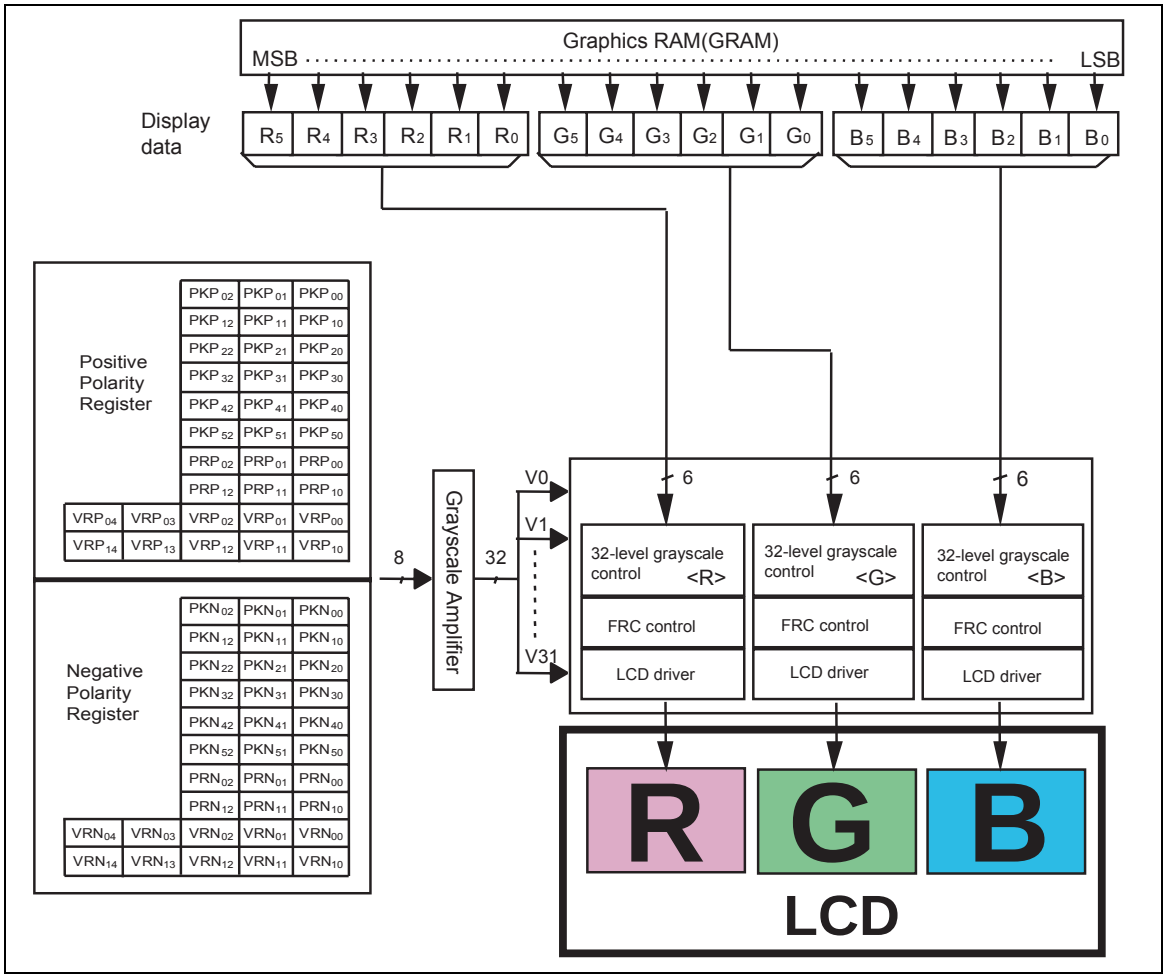


Figure 69

Grayscale amplifier unit

In grayscale amplifier unit, 8 levels VIN0 ~ VIN7 are determined by gradient and fine adjustment registers. Then, the 8 levels are divided by the internal ladder resistors between grayscale amplifiers and 32 grayscale levels (V0 ~ V31) are generated.

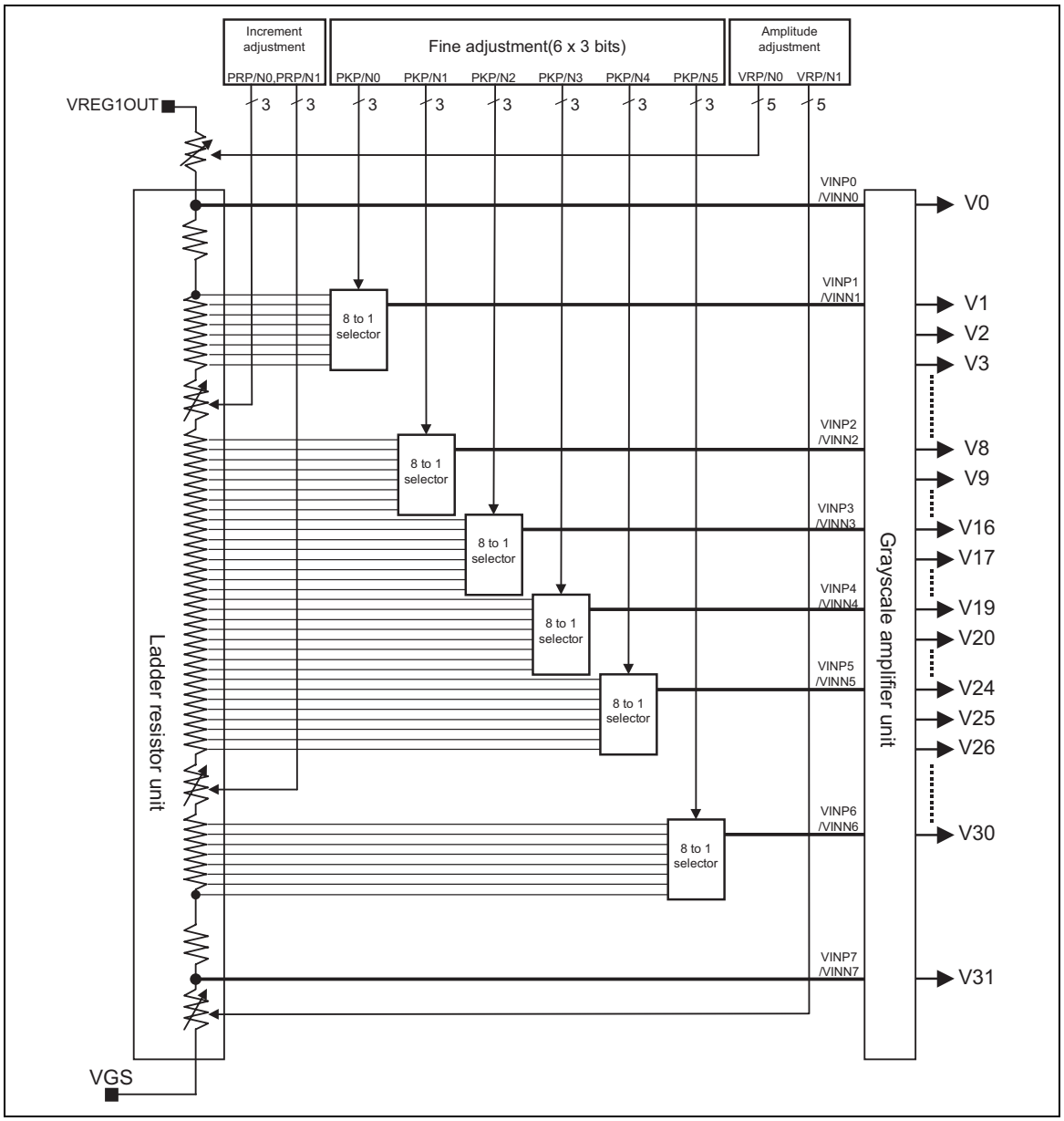


Figure 70

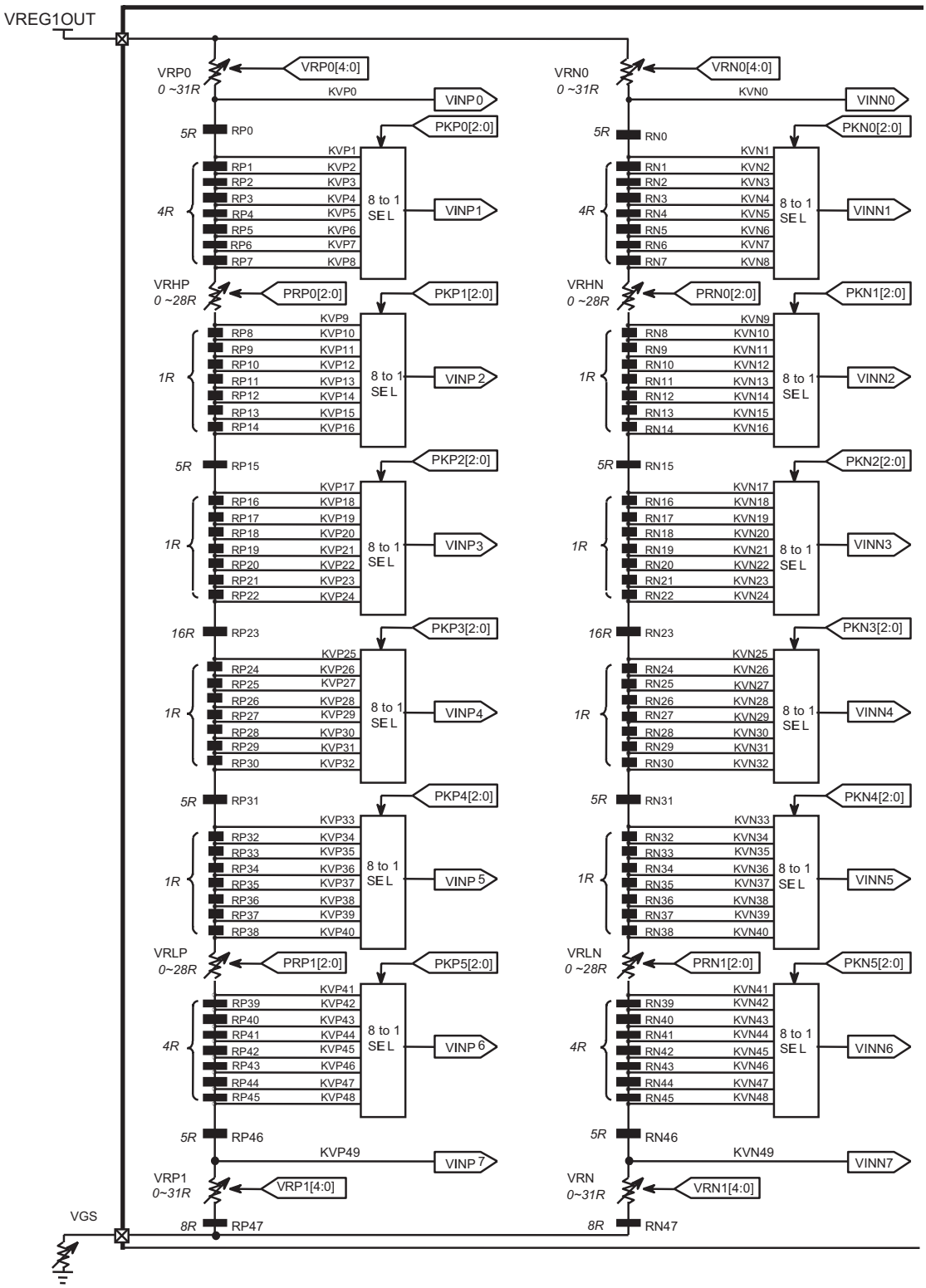


Figure 71 Reference voltage generating block (Ladder resistor units and 8-to-1 selectors)

γ Correction registers

The γ-correction registers of the R61503U consists of gradient-adjustment, amplitude-adjustment, fine-adjustment registers to correct grayscale voltage levels according to the gamma characteristics of the liquid crystal panel. These register settings make adjustments to the relationship between the grayscale number and its corresponding grayscale voltage level and the setting can be made differently for positive and negative polarities (the reference level and the register settings are the same for all RGB dots). The function of each register is as follows.

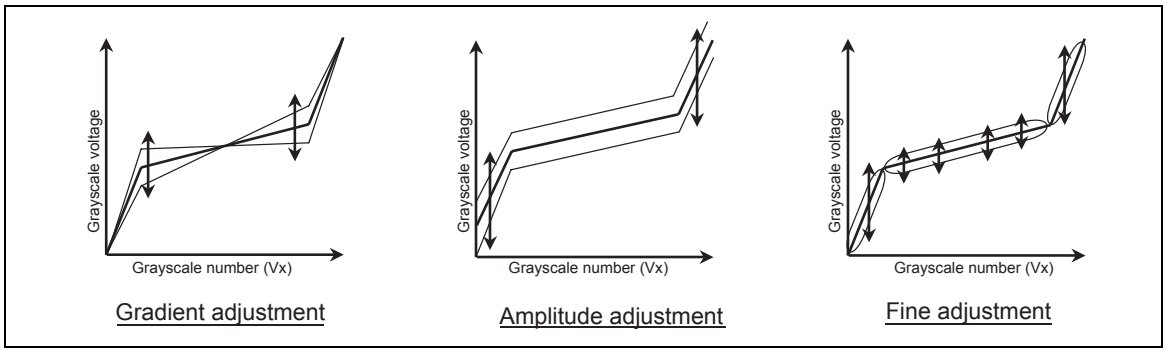


Figure 72

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradients in the middle grayscale range without changing the dynamic range. Adjustments are made by changing the resistance values of the resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit. The gradient adjustment registers consist of positive and negative polarity registers to allow asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of the grayscale voltage by changing the resistance values of the resistors (VRP(N)1/0) at both ends of the ladder resistor unit. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used for minute adjustment of grayscale voltage. The fine adjustment register represent one voltage level to be selected in the 8-to-1 selector among 8 levels generated from the ladder resistor unit. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Table 68 γ correction register

Register	Positive	Negative	Function
Gradient	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRLP(N)
Amplitude	VRP0[4:0]	VRN0[4:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Fine adjustment	PKP0[2:0]	PKN0[2:0]	8 to1 selector (grayscales1-3 voltage levels)
	PKP1[2:0]	PKN1[2:0]	8 to1 selector (grayscale 4 voltage level)
	PKP2[2:0]	PKN2[2:0]	8 to1 selector (grayscale 10 voltage level)
	PKP3[2:0]	PKN3[2:0]	8 to1 selector (grayscale 21 voltage level)
	PKP4[2:0]	PKN4[2:0]	8 to1 selector (grayscale 27 voltage level)
	PKP5[2:0]	PKN5[2:0]	8 to1 selector (grayscale 28-30 voltage levels)

Reference voltage generating block (Ladder resistor units and 8-to-1 selectors)

Block configuration

The ladder resistor and 8-to-1 selector unit shown in page 144 consists of two ladder resistor unit including variable resistors and 8-to-1 selectors which selects a voltage generated by the ladder resistor unit and output the reference voltage from which grayscale voltages are generated. The γ correction registers represent the resistance values of these resistors in the ladder resistor unit and the reference levels selected in the 8-to-1 selectors (see Table 68 γ correction register).

Variable resistors

The R61503U uses variable resistors for the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)); amplitude adjustment (1) (VRP(N)0); and amplitude adjustment (2) (VRP(N)1). The resistance values are determined by gradient adjustment and amplitude adjustment registers as below.

Table 69 Gradient adjustment

Register PRP(N) 0/1[2:0]	Resistance VRHP(N) VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 70 Amplitude adjustment (1)

Register VRP(N)0[4:0]	Resistance VRP(N)0
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

Table 71 Amplitude adjustment (2)

Register VRP(N)1[4:0]	Resistance VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 selector

The 8-to-1 selector selects one voltage level according to the fine adjustment register setting among the voltages generated by ladder resistors, and outputs the selected level as one of the reference voltages (VINP(N)1~6). The following table shows the correspondence between the selected voltage levels and the fine-adjustment register settings for respective reference voltage levels (VINP(N)1~6).

Table 72 Fine adjustment registers and selected voltage

Register bits	Selected Voltage level (reference grayscale voltage level)					
PKP(N)0/1[2:0]	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale levels V1 ~ V 31 is calculated from the following formula.

Table 73 Grayscale voltage calculation formula (positive polarity)

Pin	Formula	Fine-adjustment register	Reference voltage
KVP0	VREG1OUT-ΔV*VRP0/SUMRP	–	VINP0
KVP1	VREG1OUT-ΔV*(VRP0+5R)/SUMRP	PKP02-00="000"	VINP1
KVP2	VREG1OUT-ΔV*(VRP0+9R)/SUMRP	PKP02-00="001"	
KVP3	VREG1OUT-ΔV*(VRP0+13R)/SUMRP	PKP02-00="010"	
KVP4	VREG1OUT-ΔV*(VRP0+17R)/SUMRP	PKP02-00="011"	
KVP5	VREG1OUT-ΔV*(VRP0+21R)/SUMRP	PKP02-00="100"	
KVP6	VREG1OUT-ΔV*(VRP0+25R)/SUMRP	PKP02-00="101"	
KVP7	VREG1OUT-ΔV*(VRP0+29R)/SUMRP	PKP02-00="110"	
KVP8	VREG1OUT-ΔV*(VRP0+33R)/SUMRP	PKP02-00="111"	
KVP9	VREG1OUT-ΔV*（VRP0+33R+VRHP）/SUMRP	PKP12-10="000"	VINP2
KVP10	VREG1OUT-ΔV*（VRP0+34R+VRHP）/SUMRP	PKP12-10="001"	
KVP11	VREG1OUT-ΔV*（VRP0+35R+VRHP）/SUMRP	PKP12-10="010"	
KVP12	VREG1OUT-ΔV*（VRP0+36R+VRHP）/SUMRP	PKP12-10="011"	
KVP13	VREG1OUT-ΔV*（VRP0+37R+VRHP）/SUMRP	PKP12-10="100"	
KVP14	VREG1OUT-ΔV*（VRP0+38R+VRHP）/SUMRP	PKP12-10="101"	
KVP15	VREG1OUT-ΔV*（VRP0+39R+VRHP）/SUMRP	PKP12-10="110"	
KVP16	VREG1OUT-ΔV*（VRP0+40R+VRHP）/SUMRP	PKP12-10="111"	
KVP17	VREG1OUT-ΔV*（VRP0+45R+VRHP）/SUMRP	PKP22-20="000"	VINP3
KVP18	VREG1OUT-ΔV*（VRP0+46R+VRHP）/SUMRP	PKP22-20="001"	
KVP19	VREG1OUT-ΔV*（VRP0+47R+VRHP）/SUMRP	PKP22-20="010"	
KVP20	VREG1OUT-ΔV*（VRP0+48R+VRHP）/SUMRP	PKP22-20="011"	
KVP21	VREG1OUT-ΔV*（VRP0+49R+VRHP）/SUMRP	PKP22-20="100"	
KVP22	VREG1OUT-ΔV*（VRP0+50R+VRHP）/SUMRP	PKP22-20="101"	
KVP23	VREG1OUT-ΔV*（VRP0+51R+VRHP）/SUMRP	PKP22-20="110"	
KVP24	VREG1OUT-ΔV*（VRP0+52R+VRHP）/SUMRP	PKP22-20="111"	
KVP25	VREG1OUT-ΔV*（VRP0+68R+VRHP）/SUMRP	PKP32-30="000"	VINP4
KVP26	VREG1OUT-ΔV*（VRP0+69R+VRHP）/SUMRP	PKP32-30="001"	
KVP27	VREG1OUT-ΔV*（VRP0+70R+VRHP）/SUMRP	PKP32-30="010"	
KVP28	VREG1OUT-ΔV*（VRP0+71R+VRHP）/SUMRP	PKP32-30="011"	
KVP29	VREG1OUT-ΔV*（VRP0+72R+VRHP）/SUMRP	PKP32-30="100"	
KVP30	VREG1OUT-ΔV*（VRP0+73R+VRHP）/SUMRP	PKP32-30="101"	
KVP31	VREG1OUT-ΔV*（VRP0+74R+VRHP）/SUMRP	PKP32-30="110"	
KVP32	VREG1OUT-ΔV*（VRP0+75R+VRHP）/SUMRP	PKP32-30="111"	
KVP33	VREG1OUT-ΔV*（VRP0+80R+VRHP）/SUMRP	PKP42-40="000"	VINP5
KVP34	VREG1OUT-ΔV*（VRP0+81R+VRHP）/SUMRP	PKP42-40="001"	
KVP35	VREG1OUT-ΔV*（VRP0+82R+VRHP）/SUMRP	PKP42-40="010"	
KVP36	VREG1OUT-ΔV*（VRP0+83R+VRHP）/SUMRP	PKP42-40="011"	
KVP37	VREG1OUT-ΔV*（VRP0+84R+VRHP）/SUMRP	PKP42-40="100"	
KVP38	VREG1OUT-ΔV*（VRP0+85R+VRHP）/SUMRP	PKP42-40="101"	
KVP39	VREG1OUT-ΔV*（VRP0+86R+VRHP）/SUMRP	PKP42-40="110"	
KVP40	VREG1OUT-ΔV*（VRP0+87R+VRHP）/SUMRP	PKP42-40="111"	
KVP41	VREG1OUT-ΔV*（VRP0+87R+VRHP+VRLP）/SUMRP	PKP52-50="000"	VINP6
KVP42	VREG1OUT-ΔV*（VRP0+91R+VRHP+VRLP）/SUMRP	PKP52-50="001"	
KVP43	VREG1OUT-ΔV*（VRP0+95R+VRHP+VRLP）/SUMRP	PKP52-50="010"	
KVP44	VREG1OUT-ΔV*（VRP0+99R+VRHP+VRLP）/SUMRP	PKP52-50="011"	
KVP45	VREG1OUT-ΔV*（VRP0+103R+VRHP+VRLP）/SUMRP	PKP52-50="100"	
KVP46	VREG1OUT-ΔV*（VRP0+107R+VRHP+VRLP）/SUMRP	PKP52-50="101"	
KVP47	VREG1OUT-ΔV*（VRP0+111R+VRHP+VRLP）/SUMRP	PKP52-50="110"	
KVP48	VREG1OUT-ΔV*（VRP0+115R+VRHP+VRLP）/SUMRP	PKP52-50="111"	
KVP49	VREG1OUT-ΔV*（VRP0+120R+VRHP+VRLP）/SUMRP	–	VINP7

SUMRP : Sum of positive polarity ladder resistors = 128R+VRHP+VRLP+VRP0+VRP1
ΔV : Electrical potential between VREG1OUT and VGS

Table 74 Grayscale voltage calculation formula (positive polarity)

Grayscale	Formula
V0	VINP0
V1	V4+(VINP1-V4)*(15/24)
V2	V4+(VINP1-V4)*(8/24)
V3	V4+(VINP1-V4)*(4/24)
V4	VINP2
V5	V10+(V4-V10)*(20/24)
V6	V10+(V4-V10)*(16/24)
V7	V10+(V4-V10)*(12/24)
V8	V10+(V4-V10)*(8/24)
V9	V10+(V4-V10)*(4/24)
V10	VINP3
V11	V21+(V10-V21)*(21/24)
V12	V21+(V10-V21)*(19/24)
V13	V21+(V10-V21)*(17/24)
V14	V21+(V10-V21)*(15/24)
V15	V21+(V10-V21)*(13/24)
V16	V21+(V10-V21)*(11/24)
V17	V21+(V10-V21)*(9/24)
V18	V21+(V10-V21)*(7/24)
V19	V21+(V10-V21)*(5/24)
V20	V21+(V10-V21)*(3/24)
V21	VINP4
V22	V27+(V21-V27)*(20/24)
V23	V27+(V21-V27)*(16/24)
V24	V27+(V21-V27)*(12/24)
V25	V27+(V21-V27)*(8/24)
V26	V27+(V21-V27)*(4/24)
V27	VINP5
V28	VINP6+(V27-VINP6)*(20/24)
V29	VINP6+(V27-VINP6)*(16/24)
V30	VINP6+(V27-VINP6)*(9/24)
V31	VINP7

Make sure DDVDH – V0 > 0.5V and DDVDH – V8 >1.1V.

Table 75 Grayscale voltage calculation formula (negative polarity)

Pin	Formula	Fine-adjustment register	Reference voltage
KVN0	VREG1OUT-ΔV*VRN0/SUMRN	–	VINN0
KVN1	VREG1OUT-ΔV*(VRN0+5R)/SUMRN	PKN02-00="000"	VINN1
KVN2	VREG1OUT-ΔV*(VRN0+9R)/SUMRN	PKN02-00="001"	
KVN3	VREG1OUT-ΔV*(VRN0+13R)/SUMRN	PKN02-00="010"	
KVN4	VREG1OUT-ΔV*(VRN0+17R)/SUMRN	PKN02-00="011"	
KVN5	VREG1OUT-ΔV*(VRN0+21R)/SUMRN	PKN02-00="100"	
KVN6	VREG1OUT-ΔV*(VRN0+25R)/SUMRN	PKN02-00="101"	
KVN7	VREG1OUT-ΔV*(VRN0+29R)/SUMRN	PKN02-00="110"	
KVN8	VREG1OUT-ΔV*(VRN0+33R)/SUMRN	PKN02-00="111"	
KVN9	VREG1OUT-ΔV*（VRN0+33R+VRHN）/SUMRN	PKN12-10="000"	VINN2
KVN10	VREG1OUT-ΔV*（VRN0+34R+VRHN）/SUMRN	PKN12-10="001"	
KVN11	VREG1OUT-ΔV*（VRN0+35R+VRHN）/SUMRN	PKN12-10="010"	
KVN12	VREG1OUT-ΔV*（VRN0+36R+VRHN）/SUMRN	PKN12-10="011"	
KVN13	VREG1OUT-ΔV*（VRN0+37R+VRHN）/SUMRN	PKN12-10="100"	
KVN14	VREG1OUT-ΔV*（VRN0+38R+VRHN）/SUMRN	PKN12-10="101"	
KVN15	VREG1OUT-ΔV*（VRN0+39R+VRHN）/SUMRN	PKN12-10="110"	
KVN16	VREG1OUT-ΔV*（VRN0+40R+VRHN）/SUMRN	PKN12-10="111"	
KVN17	VREG1OUT-ΔV*（VRN0+45R+VRHN）/SUMRN	PKN22-20="000"	VINN3
KVN18	VREG1OUT-ΔV*（VRN0+46R+VRHN）/SUMRN	PKN22-20="001"	
KVN19	VREG1OUT-ΔV*（VRN0+47R+VRHN）/SUMRN	PKN22-20="010"	
KVN20	VREG1OUT-ΔV*（VRN0+48R+VRHN）/SUMRN	PKN22-20="011"	
KVN21	VREG1OUT-ΔV*（VRN0+49R+VRHN）/SUMRN	PKN22-20="100"	
KVN22	VREG1OUT-ΔV*（VRN0+50R+VRHN）/SUMRN	PKN22-20="101"	
KVN23	VREG1OUT-ΔV*（VRN0+51R+VRHN）/SUMRN	PKN22-20="110"	
KVN24	VREG1OUT-ΔV*（VRN0+52R+VRHN）/SUMRN	PKN22-20="111"	
KVN25	VREG1OUT-ΔV*（VRN0+68R+VRHN）/SUMRN	PKN32-30="000"	VINN4
KVN26	VREG1OUT-ΔV*（VRN0+69R+VRHN）/SUMRN	PKN32-30="001"	
KVN27	VREG1OUT-ΔV*（VRN0+70R+VRHN）/SUMRN	PKN32-30="010"	
KVN28	VREG1OUT-ΔV*（VRN0+71R+VRHN）/SUMRN	PKN32-30="011"	
KVN29	VREG1OUT-ΔV*（VRN0+72R+VRHN）/SUMRN	PKN32-30="100"	
KVN30	VREG1OUT-ΔV*（VRN0+73R+VRHN）/SUMRN	PKN32-30="101"	
KVN31	VREG1OUT-ΔV*（VRN0+74R+VRHN）/SUMRN	PKN32-30="110"	
KVN32	VREG1OUT-ΔV*（VRN0+75R+VRHN）/SUMRN	PKN32-30="111"	
KVN33	VREG1OUT-ΔV*（VRN0+80R+VRHN）/SUMRN	PKN42-40="000"	VINN5
KVN34	VREG1OUT-ΔV*（VRN0+81R+VRHN）/SUMRN	PKN42-40="001"	
KVN35	VREG1OUT-ΔV*（VRN0+82R+VRHN）/SUMRN	PKN42-40="010"	
KVN36	VREG1OUT-ΔV*（VRN0+83R+VRHN）/SUMRN	PKN42-40="011"	
KVN37	VREG1OUT-ΔV*（VRN0+84R+VRHN）/SUMRN	PKN42-40="100"	
KVN38	VREG1OUT-ΔV*（VRN0+85R+VRHN）/SUMRN	PKN42-40="101"	
KVN39	VREG1OUT-ΔV*（VRN0+86R+VRHN）/SUMRN	PKN42-40="110"	
KVN40	VREG1OUT-ΔV*（VRN0+87R+VRHN）/SUMRN	PKN42-40="111"	
KVN41	VREG1OUT-ΔV*（VRN0+87R+VRHN+VRLN）/SUMRN	PKN52-50="000"	VINN6
KVN42	VREG1OUT-ΔV*（VRN0+91R+VRHN+VRLN）/SUMRN	PKN52-50="001"	
KVN43	VREG1OUT-ΔV*（VRN0+95R+VRHN+VRLN）/SUMRN	PKN52-50="010"	
KVN44	VREG1OUT-ΔV*（VRN0+99R+VRHN+VRLN）/SUMRN	PKN52-50="011"	
KVN45	VREG1OUT-ΔV*（VRN0+103R+VRHN+VRLN）/SUMRN	PKN52-50="100"	
KVN46	VREG1OUT-ΔV*（VRN0+107R+VRHN+VRLN）/SUMRN	PKN52-50="101"	
KVN47	VREG1OUT-ΔV*（VRN0+111R+VRHN+VRLN）/SUMRN	PKN52-50="110"	
KVN48	VREG1OUT-ΔV*（VRN0+115R+VRHN+VRLN）/SUMRN	PKN52-50="111"	
KVN49	VREG1OUT-ΔV*（VRN0+120R+VRHN+VRLN）/SUMRN	–	VINN7

SUMRN : Sum of negative polarity ladder resistors = 128R+VRHN+VRLN+VRN0+VRN1
ΔV : Electrical potential between VREG1OUT and VGS

Table 76 Grayscale voltage calculation formula (negative polarity)

Grayscale	Formula
V0	VINN0
V1	V4+(VINN1-V4)*(15/24)
V2	V4+(VINN1-V4)*(8/24)
V3	V4+(VINN1-V4)*(4/24)
V4	VINN2
V5	V10+(V4-V10)*(20/24)
V6	V10+(V4-V10)*(16/24)
V7	V10+(V4-V10)*(12/24)
V8	V10+(V4-V10)*(8/24)
V9	V10+(V4-V10)*(4/24)
V10	VINN3
V11	V21+(V10-V21)*(21/24)
V12	V21+(V10-V21)*(19/24)
V13	V21+(V10-V21)*(17/24)
V14	V21+(V10-V21)*(15/24)
V15	V21+(V10-V21)*(13/24)
V16	V21+(V10-V21)*(11/24)
V17	V21+(V10-V21)*(9/24)
V18	V21+(V10-V21)*(7/24)
V19	V21+(V10-V21)*(5/24)
V20	V21+(V10-V21)*(3/24)
V21	VINN4
V22	V27+(V21-V27)*(20/24)
V23	V27+(V21-V27)*(16/24)
V24	V27+(V21-V27)*(12/24)
V25	V27+(V21-V27)*(8/24)
V26	V27+(V21-V27)*(4/24)
V27	VINN5
V28	VINN6+(V27-VINN6)*(20/24)
V29	VINN6+(V27-VINN6)*(16/24)
V30	VINN6+(V27-VINN6)*(9/24)
V31	VINN7

Make sure DDVDH – V0 > 0.5V and DDVDH – V8 >1.1V.

RAM Data (RGB Dot Data Bits) and the Source Output Level

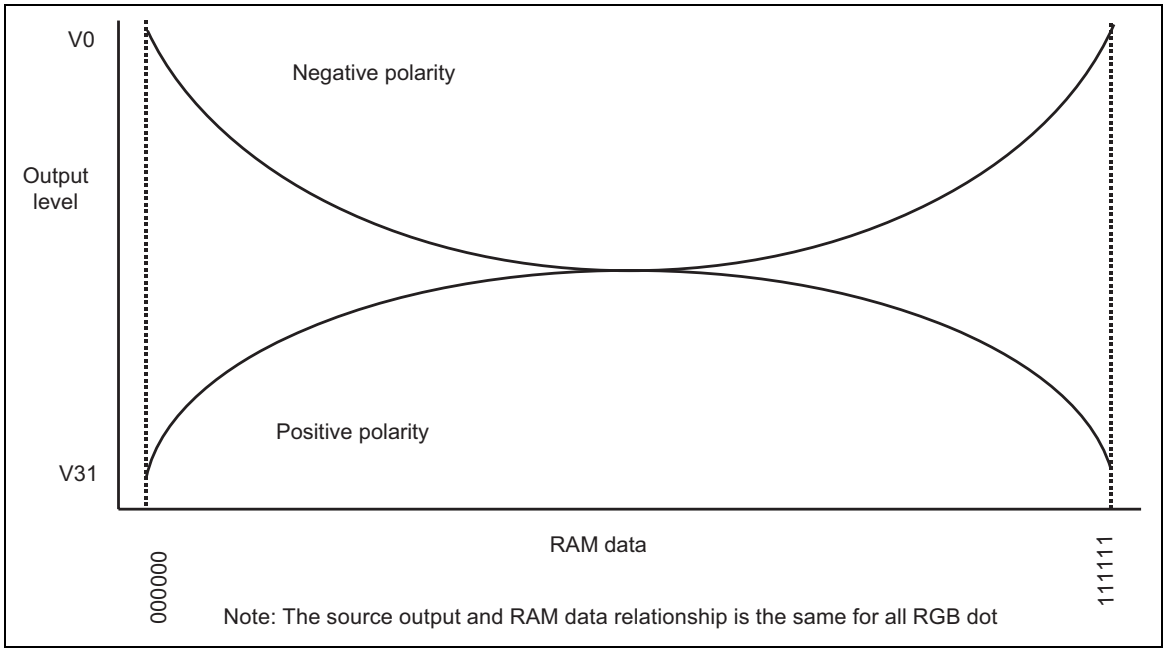


Figure 73

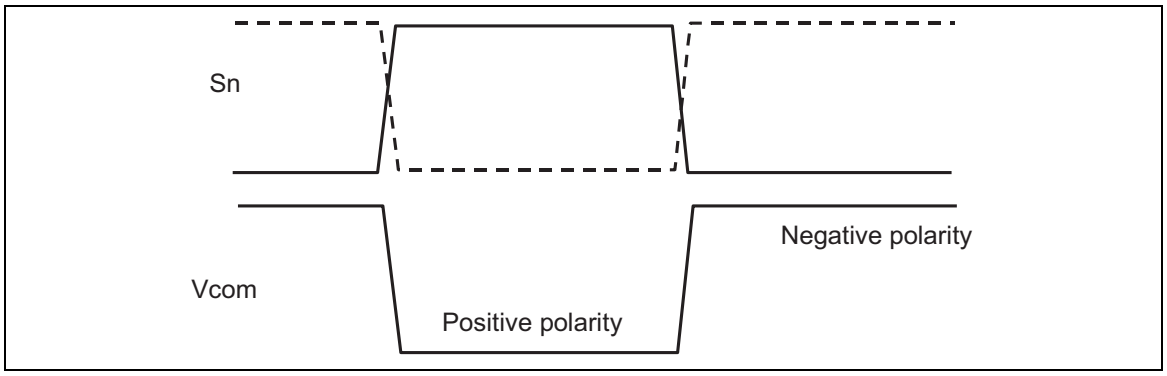


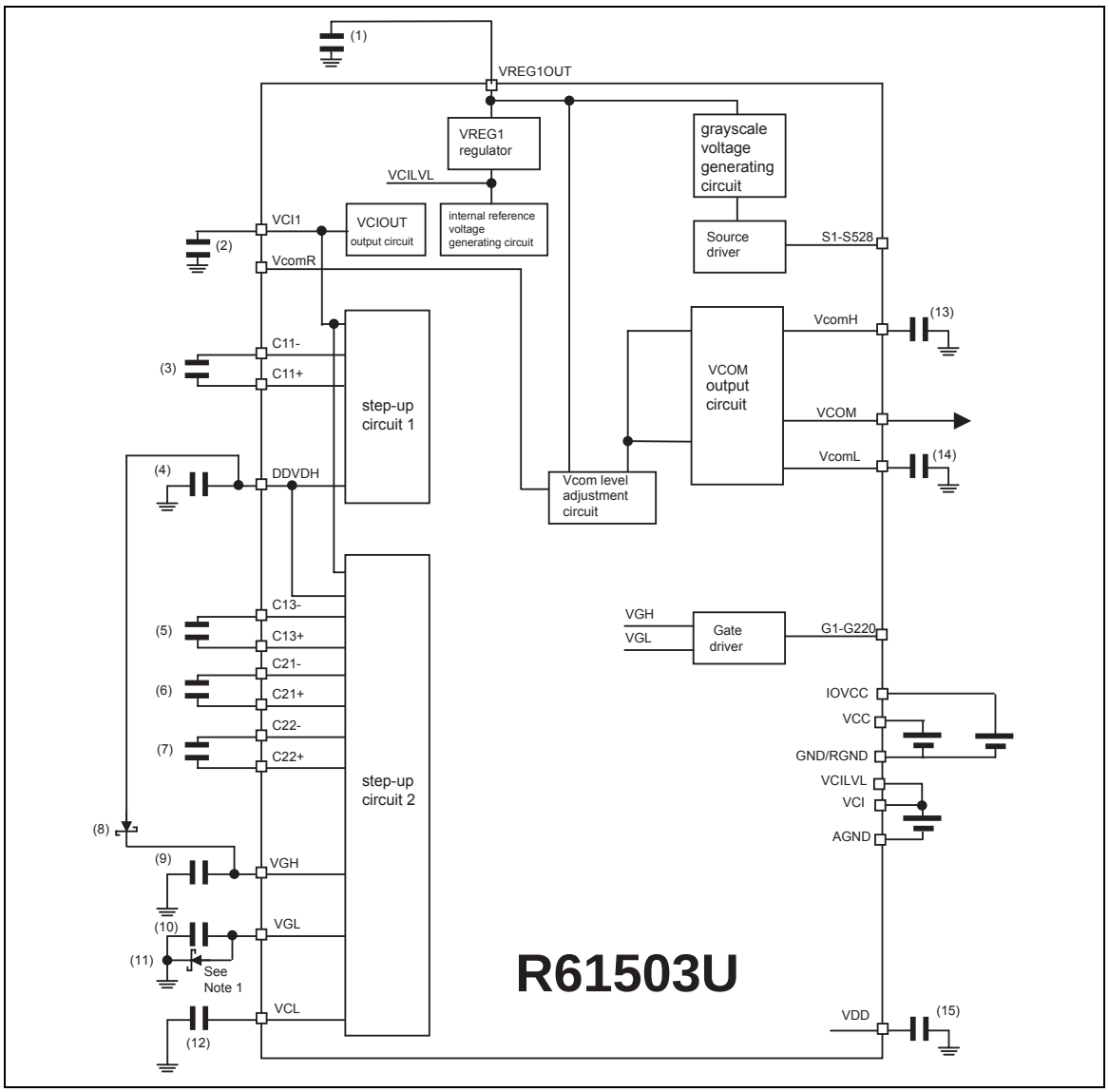
Figure 74 Source Output Waveform and Vcom Polarity

Power Supply Generating Circuit

The following is the configuration of LCD drive voltage generating circuit of the R61503U.

Power supply circuit connection example1 (Vci1=VciOUT)

The VciOUT output circuit changes the VciOUT level in this example.



Notes: 1. The wiring resistances between GND/VGL to the schottky diodes must be 10Ω or less.

2. When directly applying Vci to Vci1, set VC = 3'h7. Capacitor connection is not required for VciOUT output.

Figure 75

Specifications of external elements for the power supply circuit

The specifications of external elements connected to the power supply circuit of the R61503U are as follows.

Table 77 Capacitor

Capacitance	Upper voltage limit	Pin connection
1μF Characteristics B	6V	(2) Vci1, (3) C11+/- (5) C13+/-, (12) VCL, (14) VcomL
	10V	(4) DDVDH, (13) VcomH
	25V	(10) VGL
0.47μF Characteristics B	10V	(6) C21+/-, (7) C22+/-
	25V	(9) VGH
0.1μF Characteristics B	10V	(1) VREG1OUT

Notes: 1. Check the capacitor by connecting it on the LC module.
2. The numbers in the parentheses correspond to the numbers in Figure 74.

Table 78 Schottky diode

Specification	Pin connection
VF ＜ 0.4V/20mA@25℃, VR≧25V (Recommended diode: HSC226)	(8) DDVDH-VGH (11) GND-VGL

Table 79 Variable resistor

Specification	Pin connection
＞200kΩ	(2) VcomR

Table 80 Internal logic power supply

Capacitor	Recommended voltage proof	Pin connection
1μF (B characteristics)	6V	(15) VDD

Table 81 Oscillator

Resistance	Condition of usage	Pin connection
Rf	Rf ≥ 1mW ≥ ± 1%	OSC1-OSC2

Voltage generation diagram

The following are the diagrams of voltage generation in the R61503U and the TFT display application voltage waveforms and electrical potential relationship.

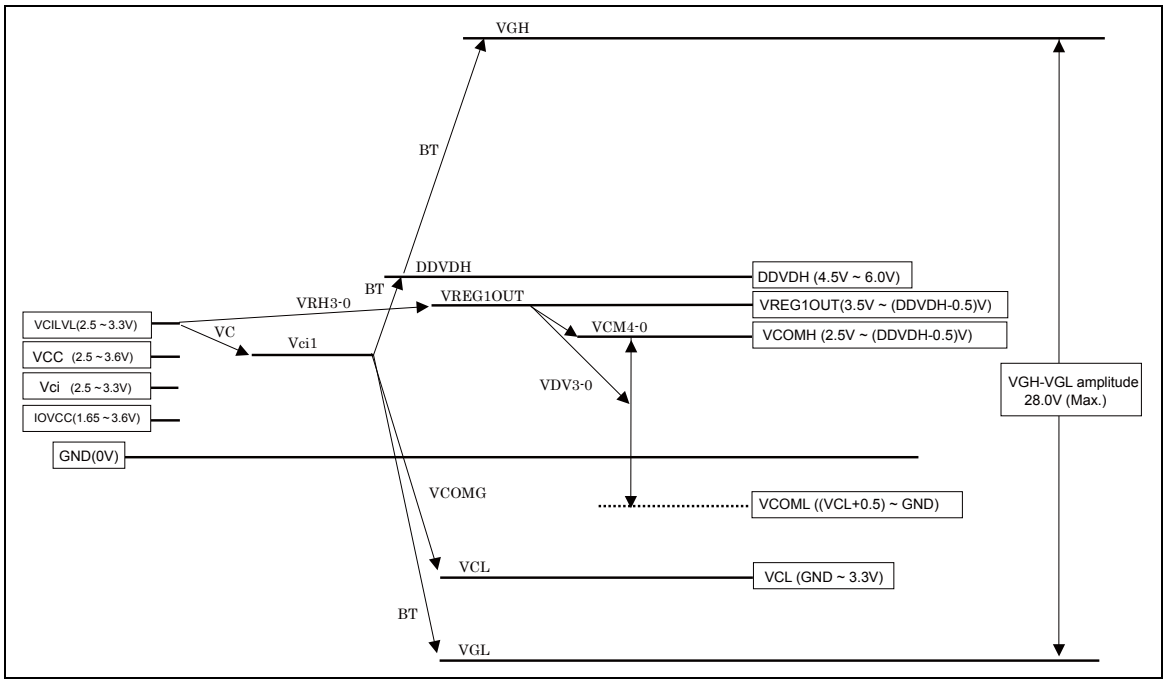


Figure 76 Pattern Diagram for Voltage Setting

Notes: 1. The DDVDH, VGH, VGL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at respective outputs. Make sure that output voltage levels in operation do not conflict with the following conditions: (DDVDH – VREG1OUT) > 0.5V, (DDVDH – VcomH) > 0.5V, (VcomL – VCL) > 0.5V. When the alternating cycle of Vcom is high (e.g. polarity inverts every line cycle), current consumption will increase. In this case, check the voltage before use.

2. The operating voltage ranges must be determined with due care so that the absolute maximum ratings are maintained.

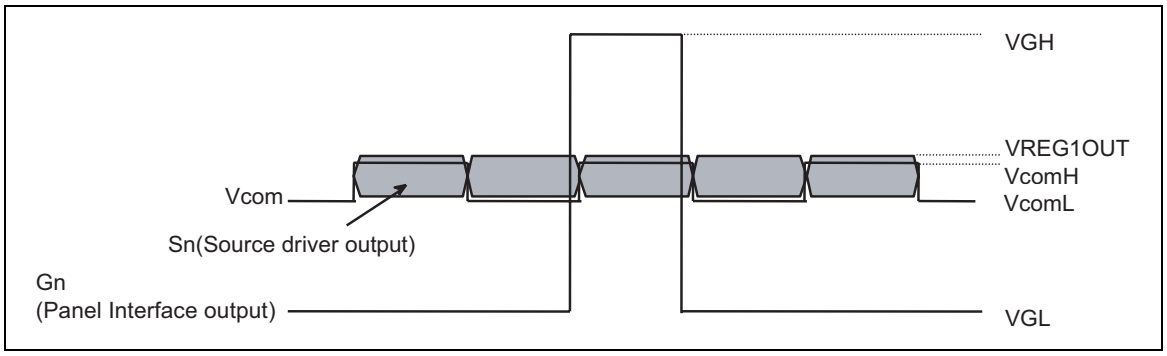


Figure 77 TFT display application voltage waveform and electrical potential

Power Supply Setting sequence

The following are the sequences for setting power supply ON/OFF instructions. Set power supply ON/OFF instructions according to the following sequences in Display ON/OFF, Sleep set/exit sequences.

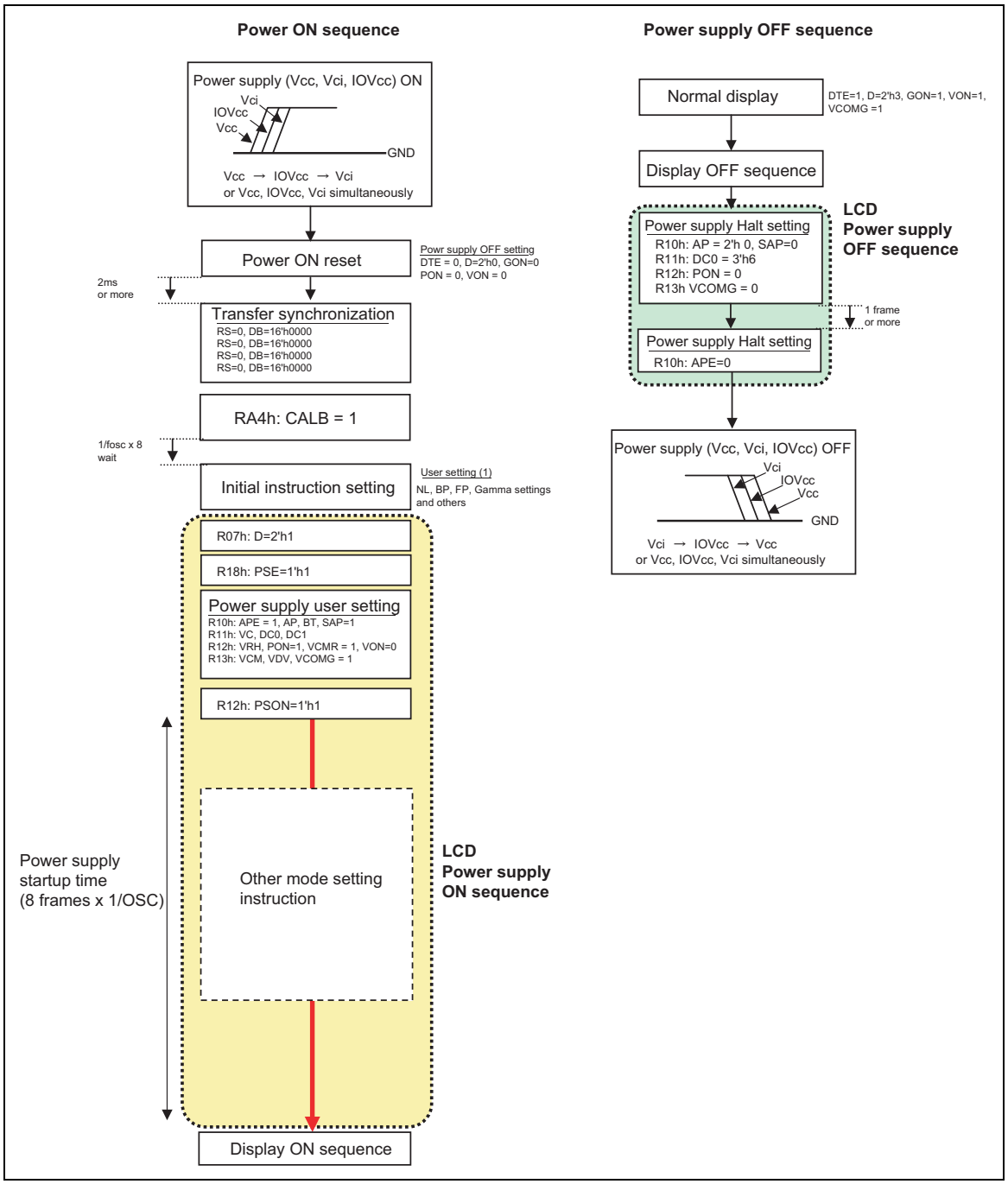


Figure 78

Instruction Setting

The following are the sequences for various instruction settings. When setting instruction in the R61503U, follow the sequence below.

Display ON/OFF

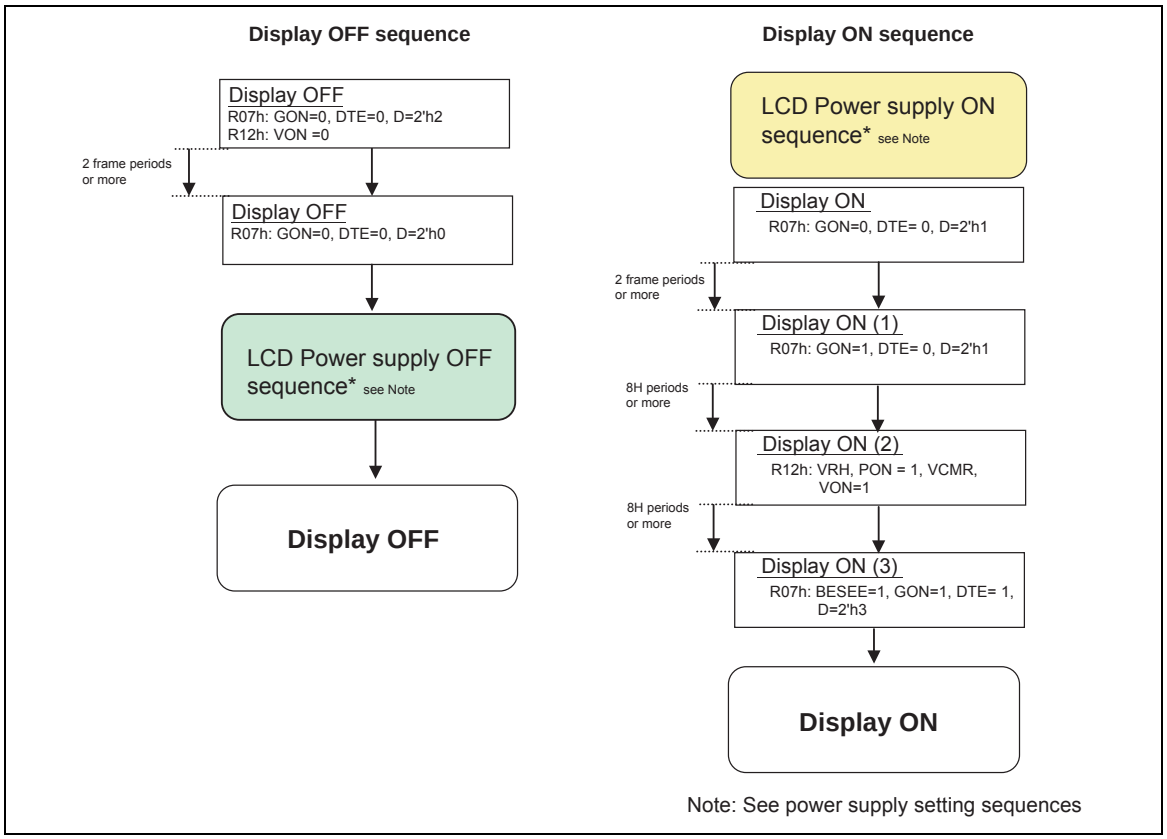


Figure 79

Sleep/Standby Mode

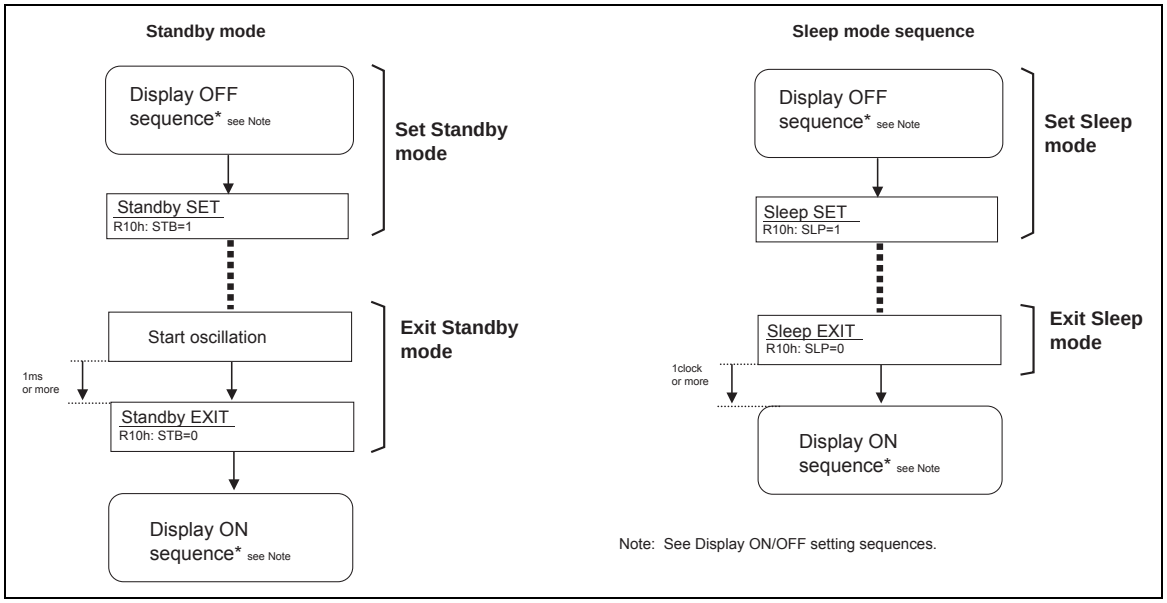


Figure 80

Deep Standby Mode

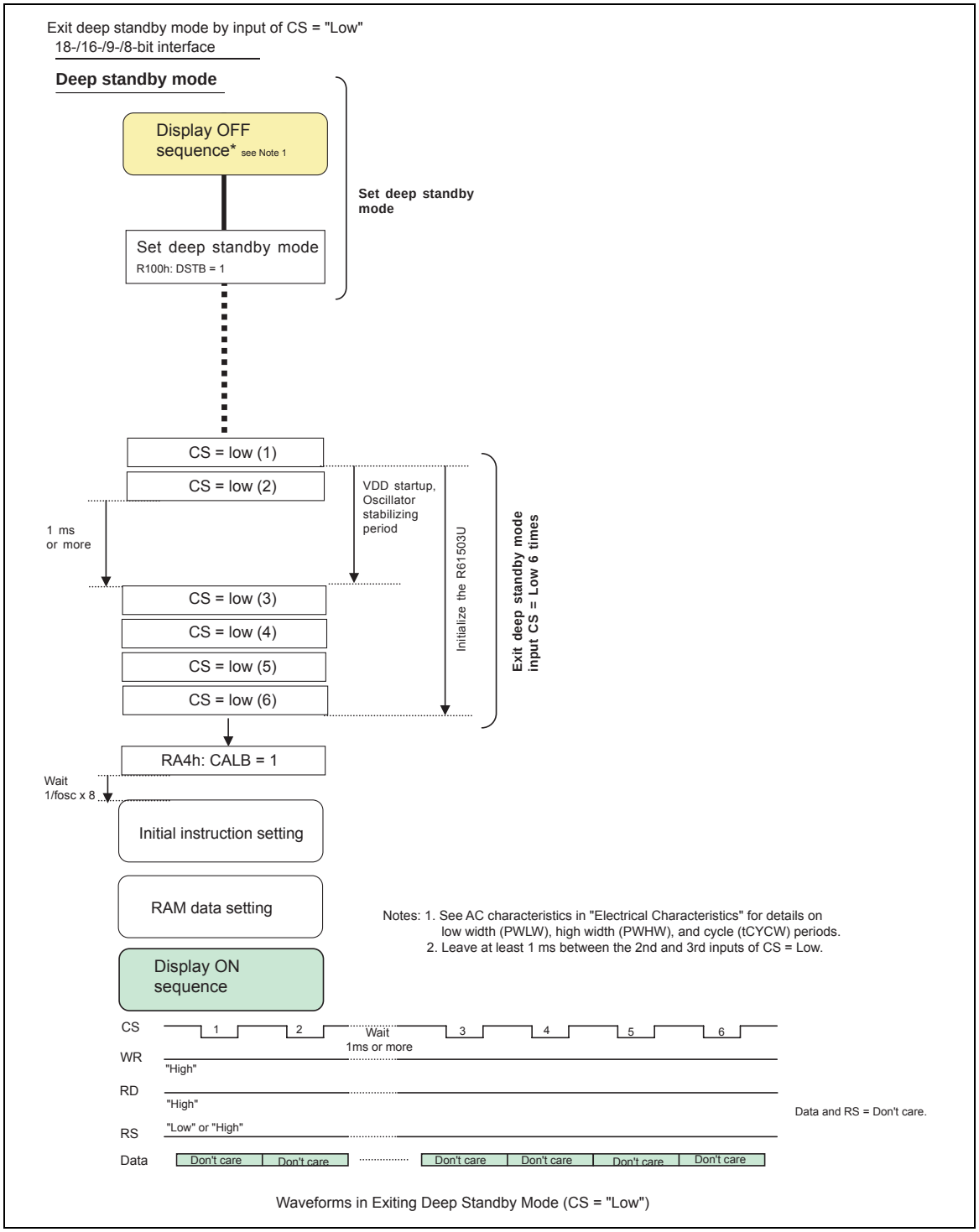
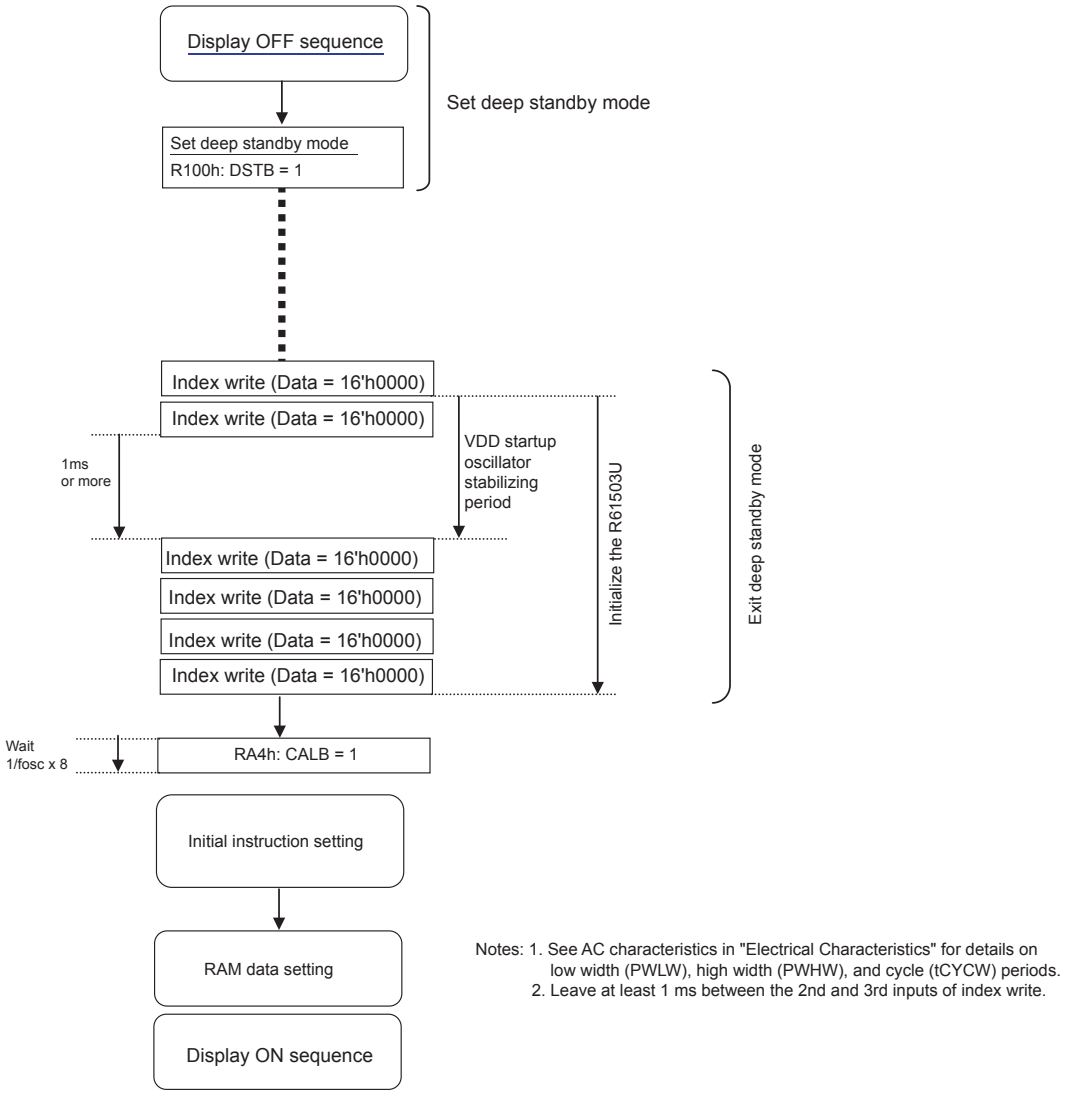


Figure 81

Exit deep standby mode by index write of CS = "Low" and of WR = "Low".

(1) 18-/16-bit interface operation



Waveforms in Exiting Deep Standby Mode (RS = "Low", index write)

Figure 82

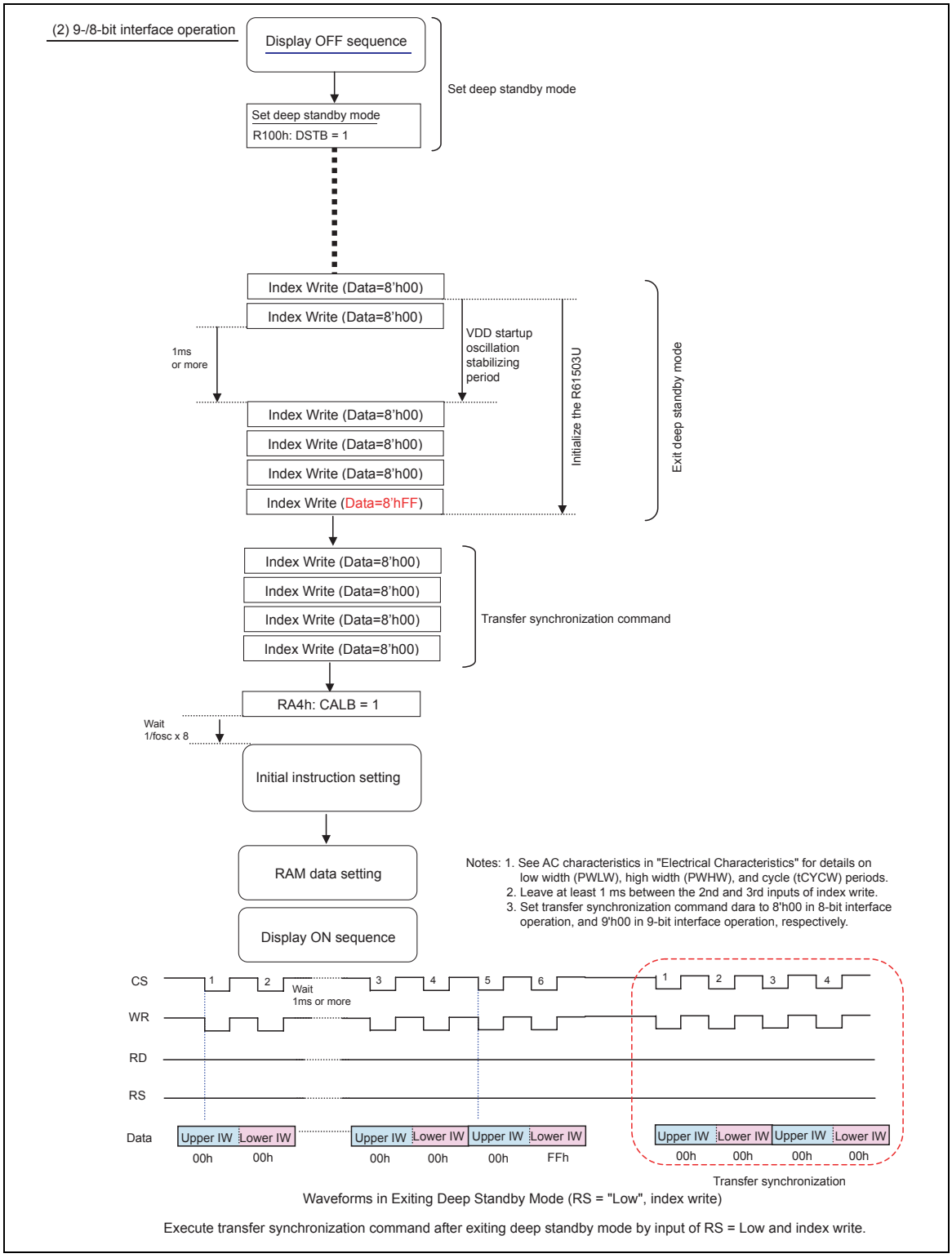

(2) 9-/8-bit interface operation
Display OFF sequence
Set deep standby mode
Set deep standby mode
R100h: DSTB = 1
Index Write (Data=8'h00)
Index Write (Data=8'h00)
1ms
or more
VDD startup
oscillation
stabilizing
period
Index Write (Data=8'h00)
Index Write (Data=8'h00)
Index Write (Data=8'h00)
Index Write (Data=8'hFF)
Initialize the R61503U
Exit deep standby mode
Index Write (Data=8'h00)
Index Write (Data=8'h00)
Index Write (Data=8'h00)
Index Write (Data=8'h00)
Transfer synchronization command
RA4h: CALB = 1
Wait
1/fosc x 8
Initial instruction setting
RAM data setting
Display ON sequence
Notes: 1. See AC characteristics in "Electrical Characteristics" for details on
low width (PWLW), high width (PWHW), and cycle (tCYCW) periods.
2. Leave at least 1 ms between the 2nd and 3rd inputs of index write.
3. Set transfer synchronization command dara to 8'h00 in 8-bit interface
operation, and 9'h00 in 9-bit interface operation, respectively.
CS
WR
RD
RS
Data
Wait
1ms or more
Upper IW
Lower IW
00h
FFh
Transfer synchronization
Waveforms in Exiting Deep Standby Mode (RS = "Low", index write)
Execute transfer synchronization command after exiting deep standby mode by input of RS = Low and index write.

Figure 83

NV Memory Control

The R61503U incorporates 8-bits x 3 address NV memory. User identification code is written in the NV memory address 0'h. VcomH setting instruction is written in the NV memory addresses 1'h, 2'h. The R61503U's NV memory has two addresses for VcomH setting to allow changing the VcomH setting. When writing the VcomH setting for the first time, write the setting in the address 1'h. Write the setting in the address 2'h when writing the setting for the second time. Make sure to write "1" to EVCM0 and EVCM1 bits. When the second VcomH setting is written in the address 2'h, the second setting is enabled.

The VCMSEL bit in the R13h register determines whether the setting in the NV memory or the VCM[4:0] setting (externally inputted instruction) is enabled to set the VcomH level. Set VCMSEL = 1, when enabling the NV memory setting. Set VCMSEL = 0, when not using the NV memory setting.

When writing the setting to the NV memory, make sure to follow the NV memory write sequence.

By performing an NV memory read operation, the setting written in NV memory is read out. In this case, follow the NV memory read sequence. In case of setting CALB = 1 (RA4h: calibration to internal operation) after power-on reset, the data written in the NV memory is stored in the NV memory read register.

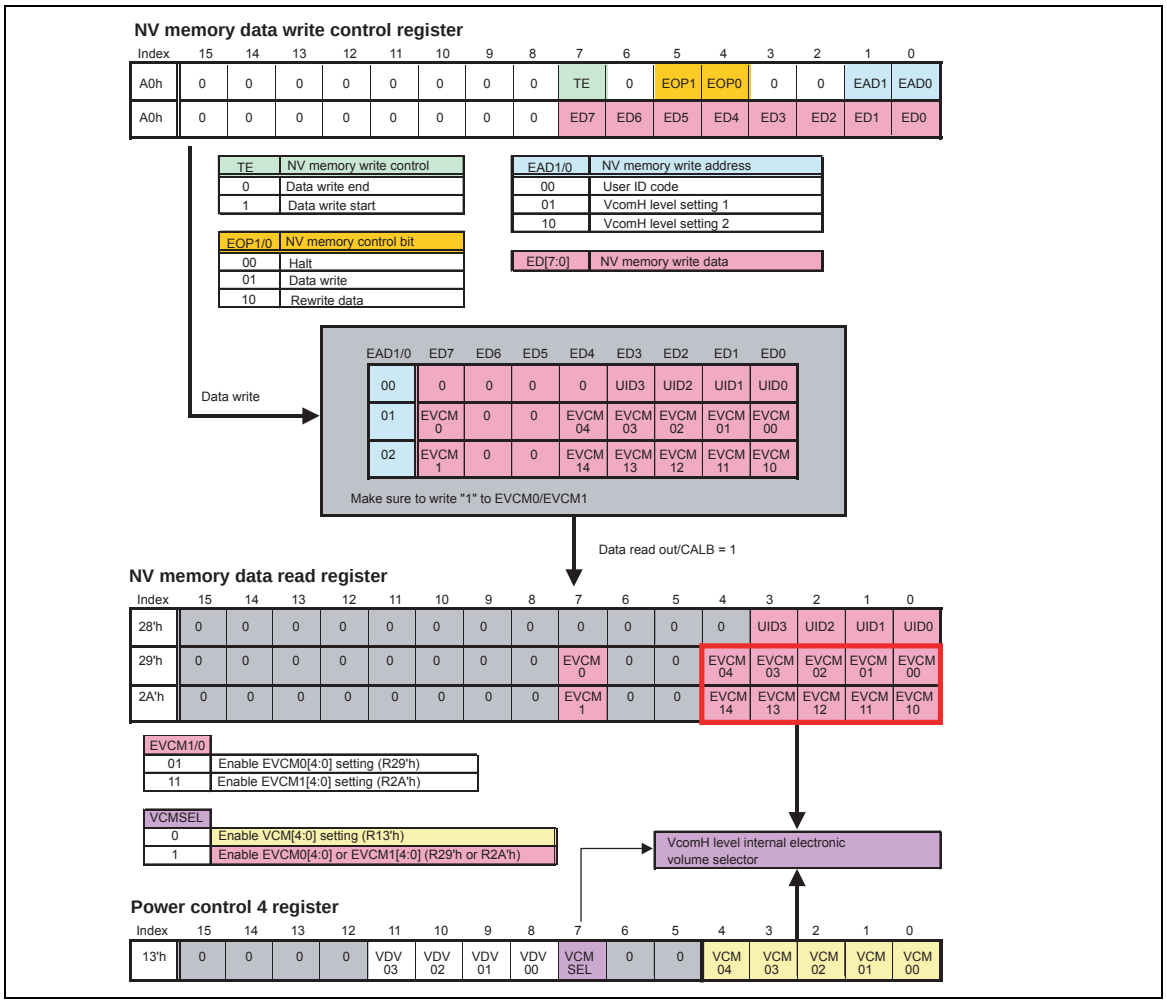
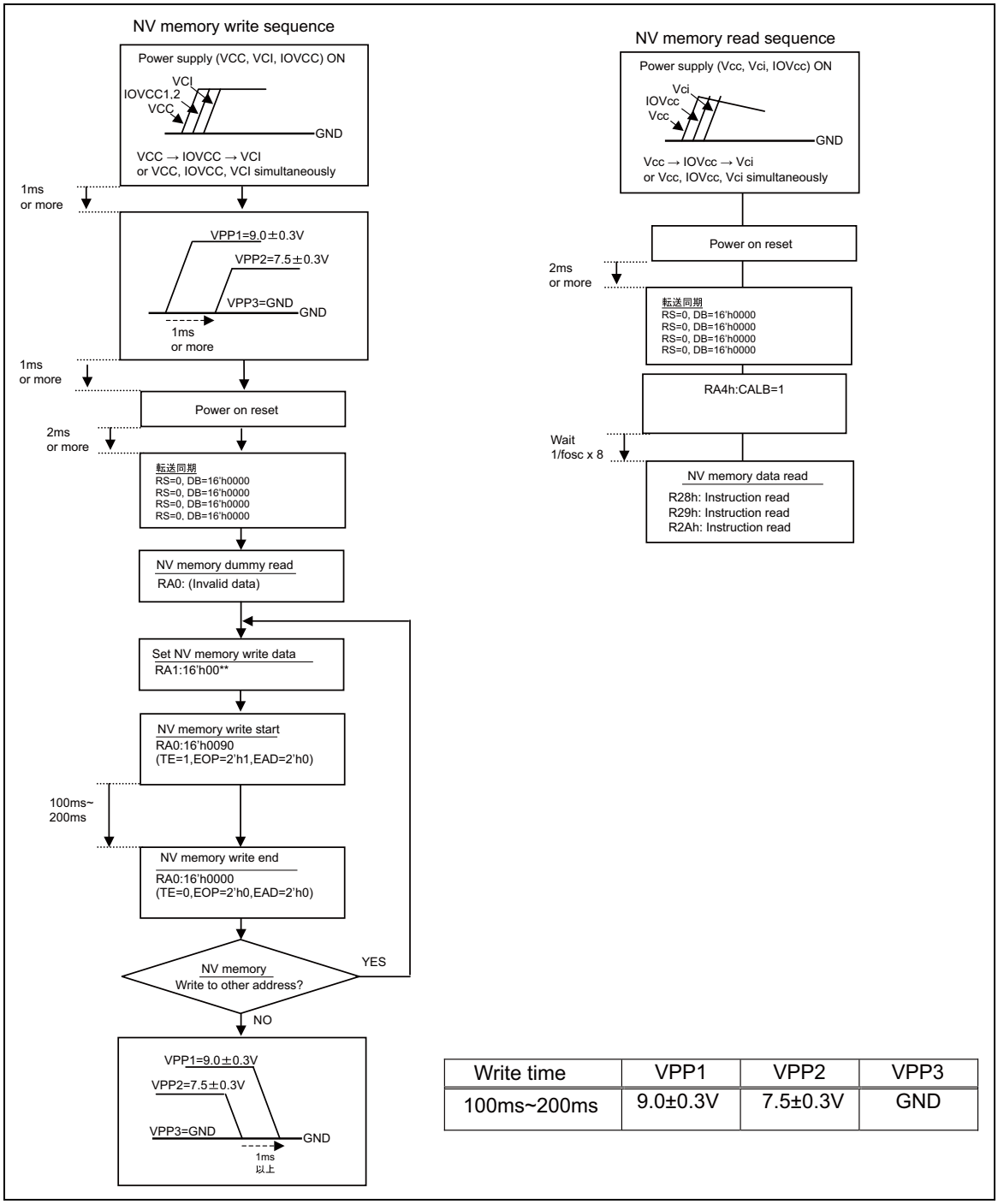


Figure 84 NV Memory System Configuration

NV Memory Write/Read Sequences

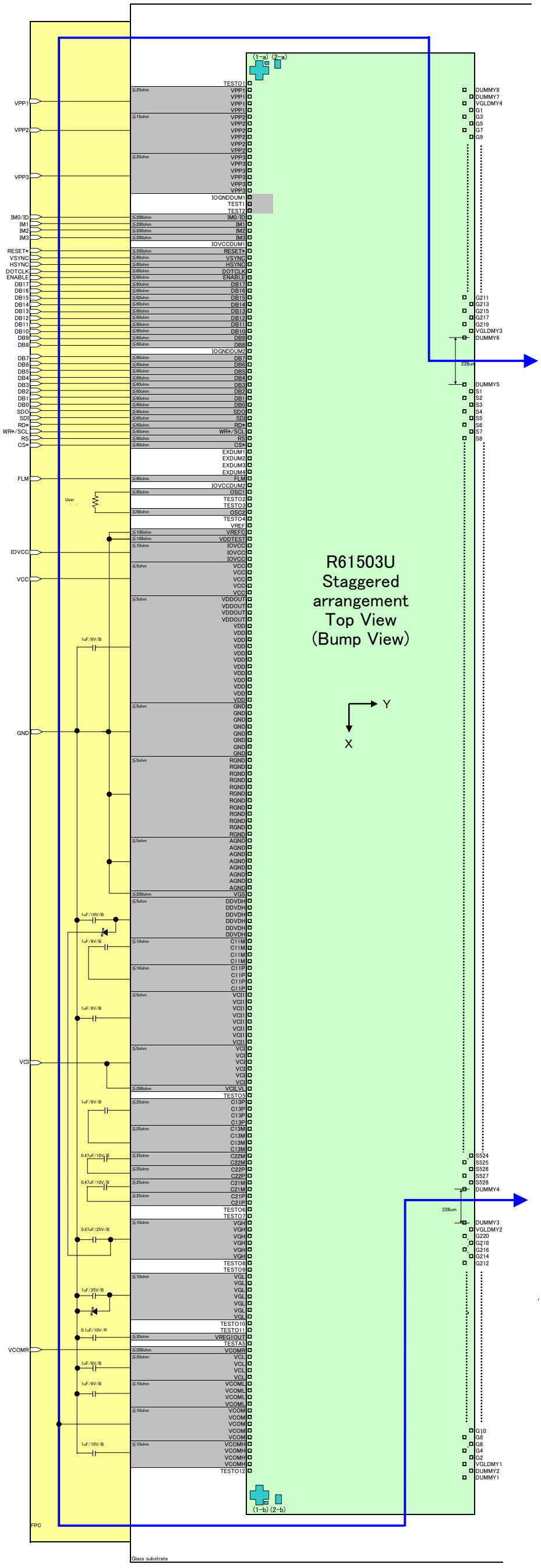


Write time	VPP1	VPP2	VPP3
100ms~200ms	9.0±0.3V	7.5±0.3V	GND

Figure 85 NV Memory Write/Read Sequences

R61503U Recommended Resistance/Connection Example

Rev0.2 2006.06.26



Absolute Maximum Ratings

Table 82

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	Vcc, IOVcc	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (2)	Vci - AGND	V	-0.3 ~ + 4.6	1, 3
Power supply voltage (3)	DDVDH - AGND	V	-0.3 ~ + 6.5	1, 4
Power supply voltage (4)	VGH - VGL	V	+11.0 ~ + 30.0	1, 4
Power supply voltage (5)	AGND - VGL	V	+3.0 ~ +13.0	1, 7
Power supply voltage (6)	DDVDH - VGL	V	+7.0 ~ +19.0	1, 5
Power supply voltage (7)	Vci - VGL	V	+5.5 ~ +16.8	1, 7
Input voltage	Vt	V	-0.3 ~ Vcc + 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	1, 8
Storage temperature	Tstg	°C	-55 ~ + 110	1

Notes: 1. If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI under the condition within the electrical characteristics in normal operation. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

2. Make sure Vcc (high) ≥ GND (low) and IOVcc (high) ≥ GND (low).
3. Make sure Vci (high) ≥ AGND (low).
4. Make sure DDVDH (high) ≥ AGND (low).
5. Make sure DDVDH (high) ≥ VGL (low).
6. Make sure VGH (high) ≥ AGND (low).
7. Make sure AGND (high) ≥ VGL (low).
8. The DC/AC characteristics of die and wafer products are guaranteed at 85 ºC.

Electrical Characteristics

DC Characteristics

Table 83 (Vcc = 2.5V ~ 3.6V, IOVcc = 1.65V ~ 3.6V, Ta = -40°C ~ 85°C) see Note 1

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Notes
Input high-level voltage	V_{IH}	V	IOV_{CC} = 1.65V ~ 3.6 V	0.8 x IOV_{CC}	—	IOV_{CC}	2, 3
Input low-level voltage	V_{IL}	V	IOV_{CC} = 1.65V ~ 3.6 V	– 0.3	—	0.2 x IOV_{CC}	2, 3
Output high voltage (DB0-17 pins, FLM)	V_{OH}	V	IOV_{CC} = 1.65V ~ 3.6 V I_{OH} = -0.1mA	0.8 x IOVcc	—	—	2
Output low voltage (DB0-17 pins, FLM)	V_{OL}	V	IOV_{CC} = 1.65 ~ 3.6 V I_{OL} = 0.1mA	—	—	0.2 x IOVcc	2
I/O leak current	I_{Li}	µA	Vin = 0 ~ IOVcc	–1	—	1	4
Current consumption: (IOVcc-GND)+(Vcc-GND) Normal operation mode	I_{OP1}	µA	fosc = 289kHz (220 line drive), fFLM=70Hz, IOVcc=Vcc=RVcc=3.0V, Ta=25°C, RAM data: “0000”h	—	120	190	5, 6
Current consumption: (IOVcc-GND)+(Vcc-GND) 8-color mode, 24-line partial display	I_{OP2}	µA	fosc = 289kHz (24 line partial drive), fFLM=40Hz, IOVcc=Vcc=RVcc=3.0V, Ta=25°C, RAM data: “0000”h	—	110	—	6
Current consumption: (IOVcc-GND)+(Vcc-GND) RAM access mode 1 normal operation mode (HWM= “0”)	I_{RAM1}	mA	tCYCW=250ns, IOVcc=2.40V, Vcc=3.0V, Ta=25°C, 80-8bit I/F, Consecutive RAM access during display	—	5	—	6
Current consumption: (IOVcc-GND)+(Vcc-GND) RAM access mode 2 high-speed write function (HWM= “1”)	I_{RAM2}	mA	tCYCW=250ns, IOVcc=2.40V, Vcc=3.0V, Ta=25°C, 80-8bit I/F, Consecutive RAM access during display	—	1.2	—	6
Current consumption: (IOVcc-GND)+(Vcc-GND) Standby mode	I_{ST}	µA	IOVcc=Vcc=Vci=3.0V, Ta=50°C	—	30	110	5
Current consumption: (IOVcc-GND)+(Vcc-GND) Deep standby mode	I_{DST}	µA	IOVcc=Vcc=Vci=3.0V, Ta=50°C	—	0.1	1.0	5
LCD power supply current (VCI-GND) 260k color display	I_{ci1}	mA	IOVcc=Vcc=3.0V, Vci=3.0V fosc =289kHz (220 lines), fFLM=70Hz, Ta=25°C, RAM data:”0000”h, AP=11, DC0=000, DC1=010, B/C =EOR=1, NW=000000, BT=000, VC=100, VRH=1000, VCM=010110, VDV=1110, Panel Load: None	—	1.0	1.5	5, 6
LCD power supply current (VCI-GND) 8-color mode	I_{ci2}	mA	IOVcc=Vcc=3.0V, Vci=3.0V fosc =289kHz (24-line partial), fFLM=40Hz, Ta=25°C, RAM data:”0000”h, AP=11, DC0=000, DC1=010, B/C =EOR=1, NW=000000, BT=000, VC=100, VRH=1000, VCM=010110, VDV=1110, CL=1, PTS=111, Panel Load: None	—	0.4	—	5, 6
Output voltage dispersion	ΔVo	mV	—	—	5	—	7
Average output voltage variance	ΔV	mV	—	—	—	35	8

Step-up circuit Characteristics

Table 84

Item		Unit	Test Condition	Min	Typ	Max	Notes
Step-up output voltage	DDVDH	V	IOVcc=Vcc=Vci=3.0V fosc =226kHz, Ta=25°C, AP=11, BT=000, DC0=000, DC1=010, VC=100, C11=C13=C21=C22=1[μF] / B Characteristics, DDVDH=VGH=VGL=VCL=1[μF] / B Characteristics, Panel load: None, I_{load1} = -1[mA]	4.0	4.2	—	10
	VGH	V	IOVcc=Vcc=Vci=3.0V fosc =226kHz, Ta=25°C, AP=11, BT=000, DC0=000, DC1=010, VC=100, C11=C13=C21=C22=1[μF] / B Characteristics, DDVDH=VGH=VGL=VCL=1[μF] / B Characteristics, Panel load: None, I_{load1} = -100[μA]	12.6	13.1	—	10
	VGL	V	IOVcc=Vcc=Vci=3.0V fosc =226kHz, Ta=25°C, AP=11, BT=000, DC0=000, DC1=010, VC=100, C11=C13=C21=C22=1[μF] / B Characteristics, DDVDH=VGH=VGL=VCL=1[μF] / B Characteristics, Panel load: None, I_{load1} = 100[μA]	-10.5	-11.1	—	10
	VCL	V	IOVcc=Vcc=Vci=3.0V fosc =226kHz, Ta=25°C, AP=11, BT=000, DC0=000, DC1=010, VC=100, C11=C13=C21=C22=1[μF] / B Characteristics, DDVDH=VGH=VGL=VCL=1[μF] / B Characteristics, Panel load: None, I_{load1} = +200[μA]	-1.98	-2.0	—	10
Input voltage	Vci	V		2.5	—	3.3	—

AC Characteristics

(Vcc=2.5V ~ 3.6V, IOVcc = 1.65V ~ 3.6V, Ta = – 40°C ~ +85°C*) * see Note 1

Table 85 Clock Characteristics

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
RC oscillation clock	f_{OSC}	kHz	Rf = 260 kΩ Vcc=3.0V	192	226	271	9

80-system Bus Interface Timing Characteristics (18/16-bit I/F)

Table 86 Normal write operation (HWM= "0"), IOVcc = 1.65V ~ 3.6V, Vcc = 2.5V ~ 3.6V

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 89	120	—	—
	Read	t_{CYCR}	ns	Figure 89	450	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 89	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 89	200	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 89	50	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 89	250	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 89	—	—	25
Setup time	Write (RS~CS*, WR*)	t_{AS}	ns	Figure 89	0	—	—
	Read (RS~CS*, RD*)				10		
Address hold time		t_{AH}	ns	Figure 89	2	—	—
Write data setup time		t_{DSW}	ns	Figure 89	25	—	—
Write data hold time		t_H	ns	Figure 89	5	—	—
Read data delay time		t_{DDR}	ns	Figure 89	—	—	100
Read data hold time		t_{DHR}	ns	Figure 89	5	—	—

Table 87 High-Speed Write function (HWM= "1"), IOVcc = 1.65V ~ 3.6V, Vcc = 2.5V ~ 3.6V

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 89	80	—	—
	Read	t_{CYCR}	ns	Figure 89	450	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 89	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 89	250	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 89	40	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 89	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 89	—	—	25
Setup time	Write (RS~CS*, WR*)	t_{AS}	ns	Figure 89	0	—	—
	Read (RS~CS*, RD*)				10		
Address hold time		t_{AH}	ns	Figure 89	2	—	—
Write data setup time		t_{DSW}	ns	Figure 89	25	—	—
Write data hold time		t_H	ns	Figure 89	5	—	—
Read data delay time		t_{DDR}	ns	Figure 89	—	—	100
Read data hold time		t_{DHR}	ns	Figure 89	5	—	—

80-system Bus Interface Timing Characteristics (9/8-bit I/F)

Table 88 Normal/High-speed Write function (HWM= "0/1"), IOVcc = 1.65V ~ 3.6V, Vcc = 2.5V ~ 3.6V

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 89	70	—	—
	Read	t_{CYCR}	ns	Figure 89	400	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 89	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 89	200	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 89	30	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 89	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 89	—	—	25
Setup time	Write (RS~CS*, WR*)	t_{AS}	ns	Figure 89	0	—	—
	Read (RS~CS*, RD*)				10		
Address hold time		t_{AH}	ns	Figure 89	2	—	—
Write data setup time		t_{DSW}	ns	Figure 89	25	—	—
Write data hold time		t_{H}	ns	Figure 89	5	—	—
Read data delay time		t_{DDR}	ns	Figure 89	—	—	100
Read data hold time		t_{DHR}	ns	Figure 89	5	—	—

Serial interface Timing Characteristics

Table 89 IOVcc = 1.65V ~ 3.6V, Vcc = 2.5V ~ 3.6V

Item		Symbol	Unit	Timing Diagram	Min.	Typ.	Max.
Serial clock cycle time	Write (received)	t_{SCYC}	ns	Figure 90	100	-	20,000
	Read (transmitted)	t_{SCYC}	ns	Figure 90	350	-	20,000
Serial clock high-level pulse width	Write (received)	t_{SCH}	ns	Figure 90	40	-	-
	Read (transmitted)	t_{SCH}	ns	Figure 90	150	-	-
Serial clock low-level pulse width	Write (received)	t_{SCL}	ns	Figure 90	40	-	-
	Read (transmitted)	t_{SCL}	ns	Figure 90	150	-	-
Serial clock rise/fall time		t_{SCr}, t_{SCf}	ns	Figure 90	-	-	20
Chip select setup time		t_{CSU}	ns	Figure 90	20	-	-
Chip select hold time		t_{CH}	ns	Figure 90	60	-	-
Serial input data setup time		t_{SISU}	ns	Figure 90	30	-	-
Serial input data hold time		t_{SIH}	ns	Figure 90	30	-	-
Serial output data delay time		t_{SOD}	ns	Figure 90	-	-	130
Serial output data hold time		t_{SOH}	ns	Figure 90	5	-	-

Reset Timing Characteristics

Table 90 (IOVcc = 1.65V ~ 3.6V, Vcc = 2.5V ~ 3.6V)

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
Reset low-level width	t_{RES}	ms	Figure 91	1	—	—
Reset rise time	t_{rRES}	μs	Figure 91	—	—	10

RGB Interface timing characteristics

Table 91 18/16-bit I/F, High-speed Write function (HWM= "1"), IOVcc = 1.65V ~ 3.6V, Vcc = 2.5V ~ 3.6V

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
VSYNC/HSYNC setup time	tSYNCS	clocks	Figure 92	0	—	1
ENABLE setup time	tENS	ns	Figure 92	10	—	—
ENABLE hold time	tENH	ns	Figure 92	20	—	—
DOTCLK "Low" level pulse width	PW_{DL}	ns	Figure 92	40	—	—
DOTCLK "High" level pulse width	PW_{DH}	ns	Figure 92	40	—	—
DOTCLK cycle time	tCYCD	ns	Figure 92	100	—	—
Data setup time	tPDS	ns	Figure 92	10	—	—
Data hold time	tPDH	ns	Figure 92	40	—	—
DOTCLK, VYSNC, HSYNC rise/fall time	Trgbr, trgbf	ns	Figure 92	—	—	25

Table 92 6-bit I/F, High-speed Write function (HWM= "1"), IOVcc = 1.65V ~ 3.6V, Vcc= 2.5V ~ 3.6V

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
VSYNC/HSYNC setup time	tSYNCS	clocks	Figure 92	0	—	1
ENABLE setup time	tENS	ns	Figure 92	10	—	—
ENABLE hold time	tENH	ns	Figure 92	20	—	—
DOTCLK "Low" level pulse width	PW_{DL}	ns	Figure 92	30	—	—
DOTCLK "High" level pulse width	PW_{DH}	ns	Figure 92	30	—	—
DOTCLK cycle time	tCYCD	ns	Figure 92	80	—	—
Data setup time	tPDS	ns	Figure 92	10	—	—
Data hold time	tPDH	ns	Figure 92	30	—	—
DOTCLK, VYSNC, HSYNC rise/fall time	Trgbr, trgbf	ns	Figure 92	—	—	25

LCD driver output Characteristics

Table 93

Item	Symbol	Unit	Test condition	Min	Typ	Max	Note
Driver output delay time	t_{dd}	μs	Vcc=3.0V, DDVDH=5.5V, VREG1OUT=5.0V, fosc =226kHz, 220 line drive, Ta=25°C REV=0, AP=010, VRP14-00=0, VRN14-00=0, PKP52-00=0, PKN52-00=0 PRP12-00=0, PRN12-00=0 Load resistance R=10kΩ, Load capacitance C=20pF Time to reach the target voltage level ±35mV from the Vcom polarity inversion timing Transition from the same grayscale level at all source pins	—	38	—	11

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.

2. The following figures illustrate the configurations of input, I/O, and output pins.

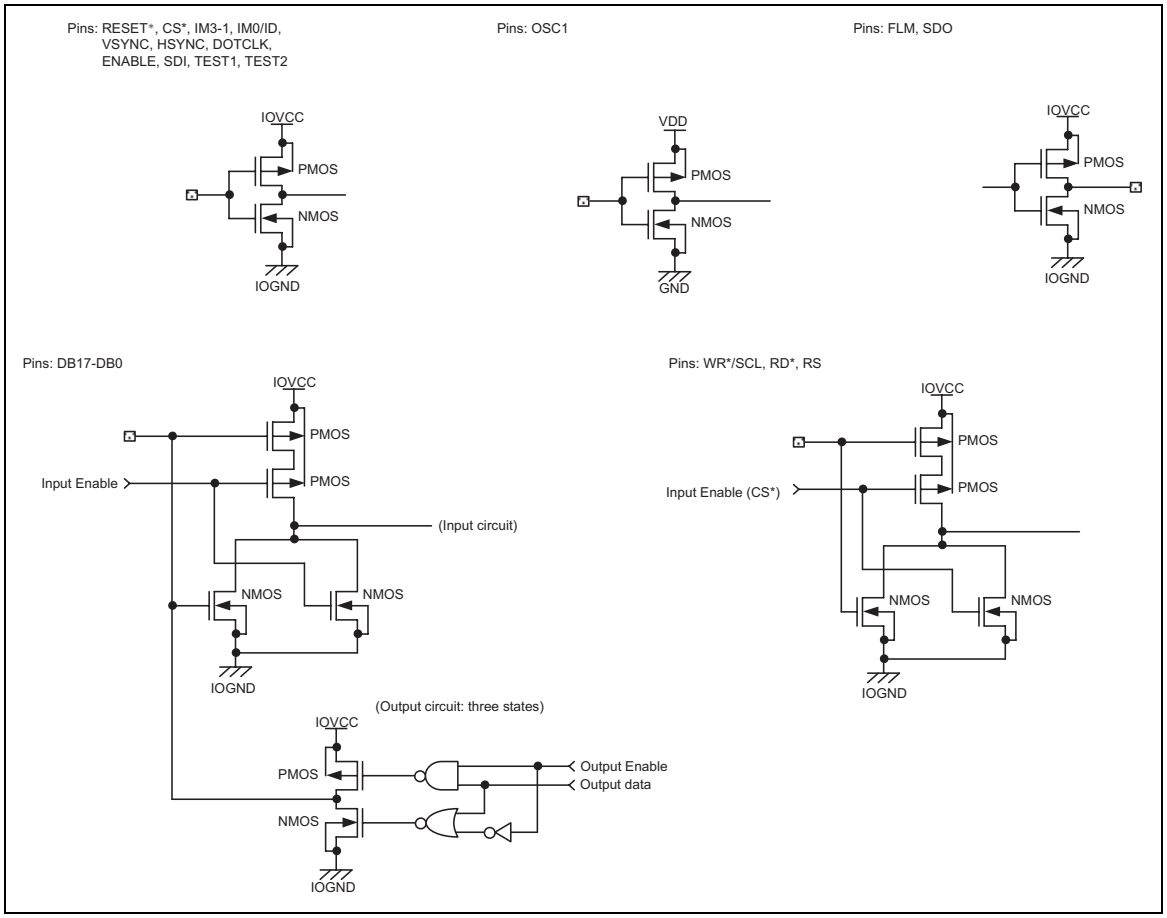


Figure 86

3. The TEST1, TEST2 pins must be grounded (GND). The IM3/2/1 and IM0/ID pins must be fixed at either IOVcc or GND.

4. This excludes the current in the output-drive MOS.

5. This excludes the current in the input/output units. Make sure that the input level is fixed because through current will increase in the input circuit when the CMOS input level takes a middle range level. The current consumption is unaffected by whether the CS*pin is “High” or “Low” while not accessing via interface pins.

6. The relationship between voltages and the current consumption is as follows.

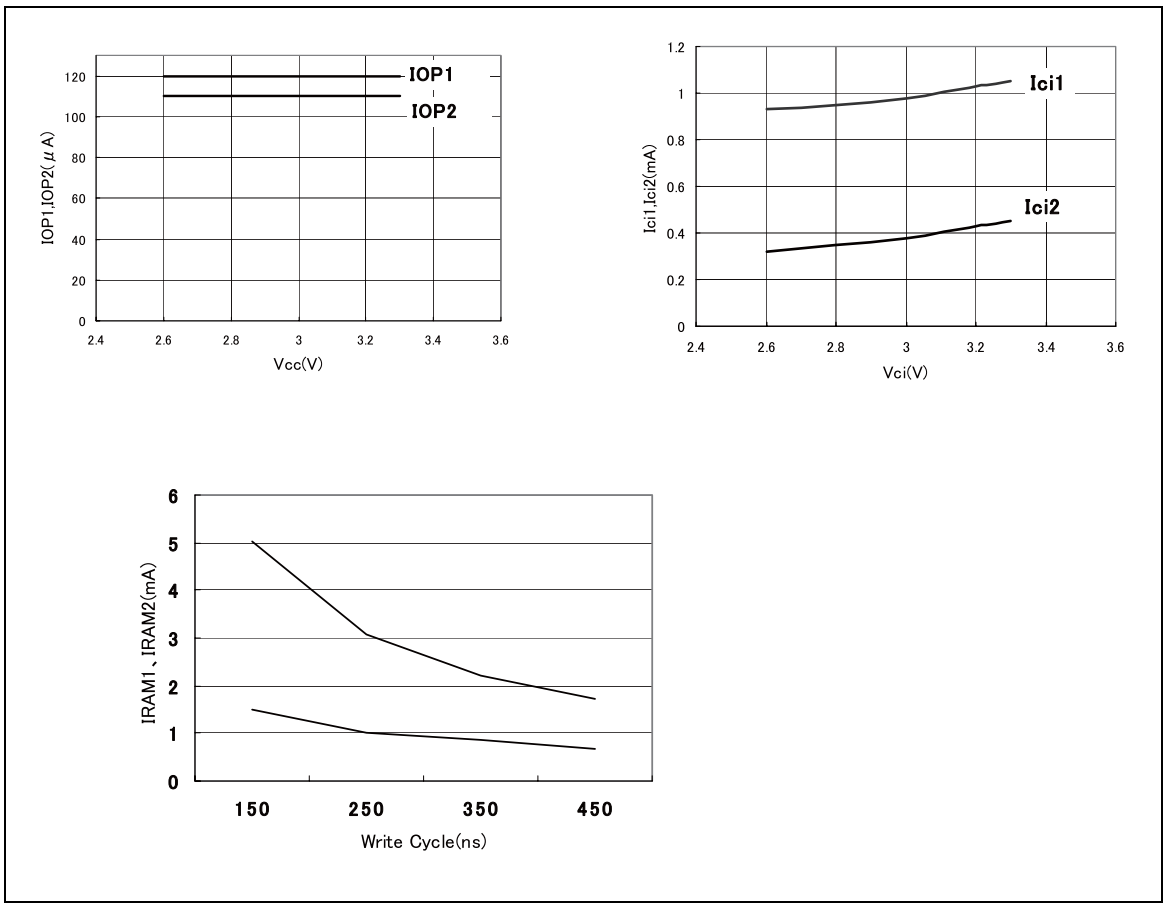


Figure 87

7. The output voltage deviation is the difference in the voltages from adjacent source pins for the same display data. This value is shown just for reference.

8. The average output voltage dispersion is the variance of average source-output voltage of different chips of the same product. The average source output voltage is measured for each chip with same display data.

9. This applies to internal oscillators when using external oscillation resistor Rf.

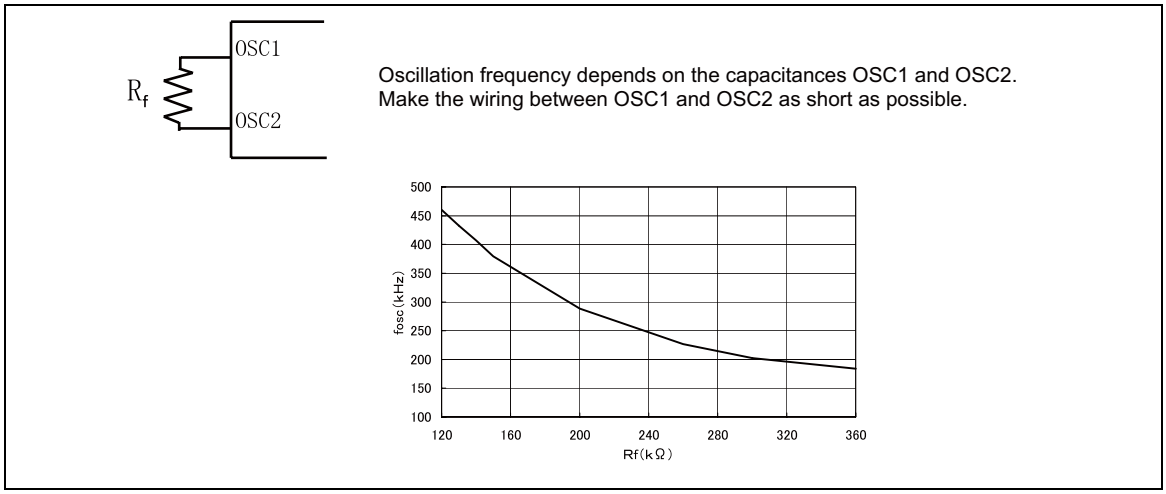


Figure 88

10. The wiring resistance when the R61503U is mounted on the glass substrate is not taken into consideration. No load is applied on pins except those for measurement. See the reference data “Load current characteristics”.

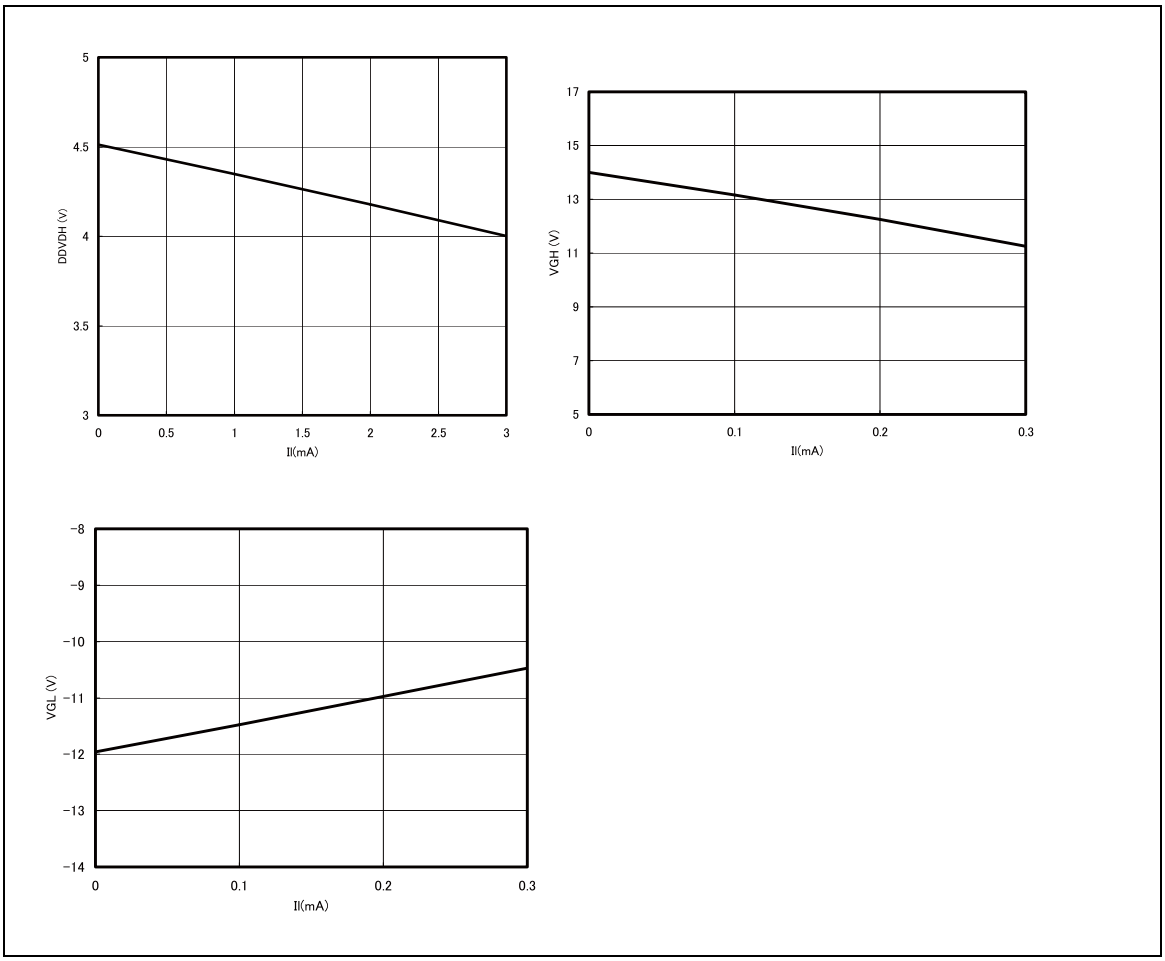

5
4.5
4
3.5
3
DDVDH (V)
0
0.5
1
1.5
2
2.5
3
II(mA)
17
15
13
11
9
7
5
VGH (V)
0
0.1
0.2
0.3
II(mA)
−8
−9
−10
−11
−12
−13
−14
VGL (V)
0
0.1
0.2
0.3
II(mA)

Figure 89

11. The liquid crystal driver output delay time depends on the load on the liquid crystal panel. Adjust the frame frequency and the cycle per line by checking the quality of display on the actual panel in use.

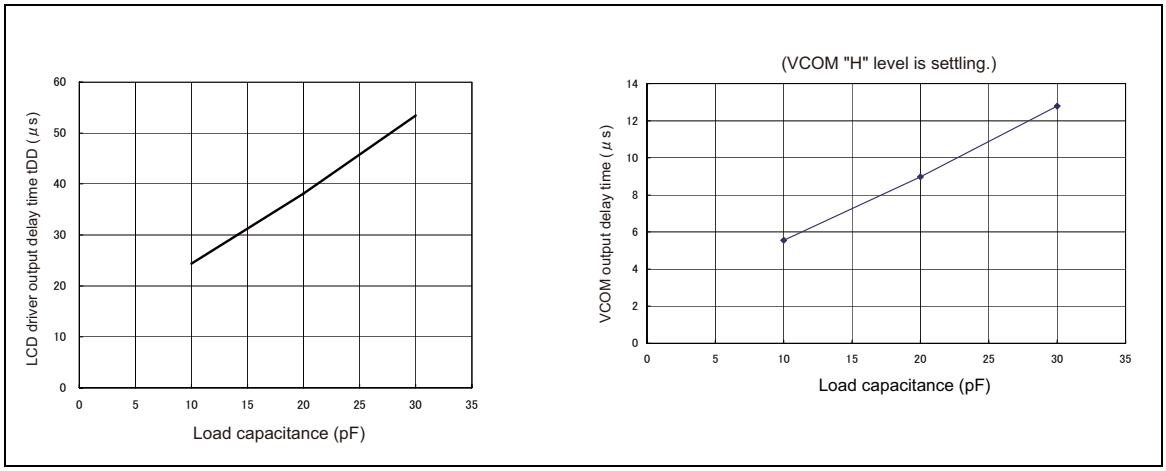


Figure 90

Test Circuits

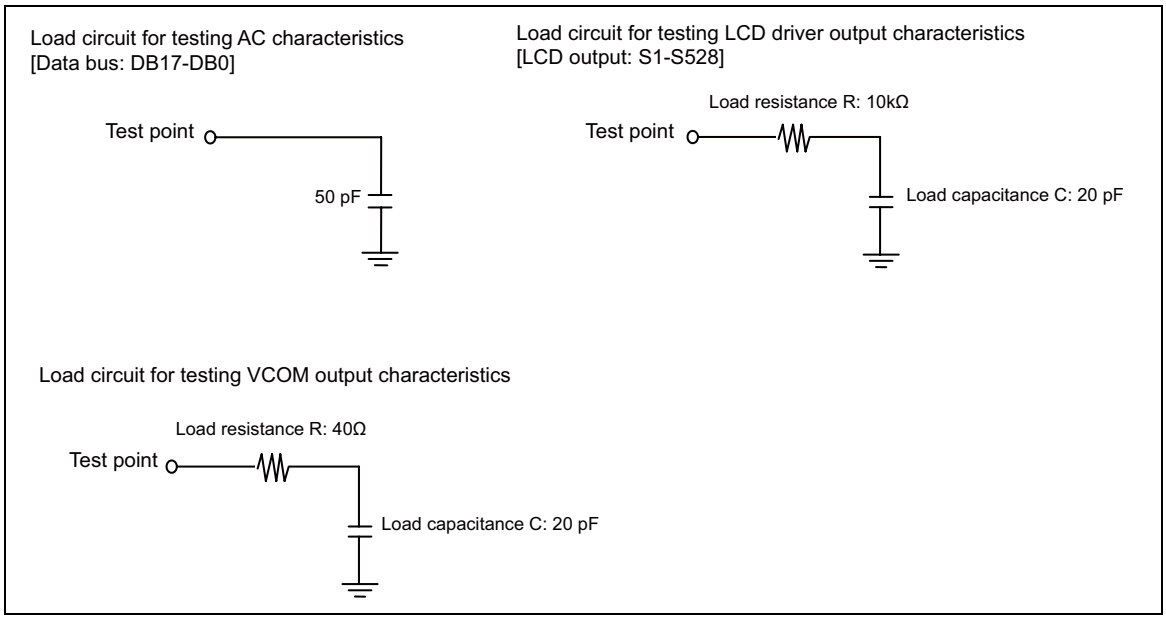


Figure 91

Timing Characteristics

80-system Bus Interface

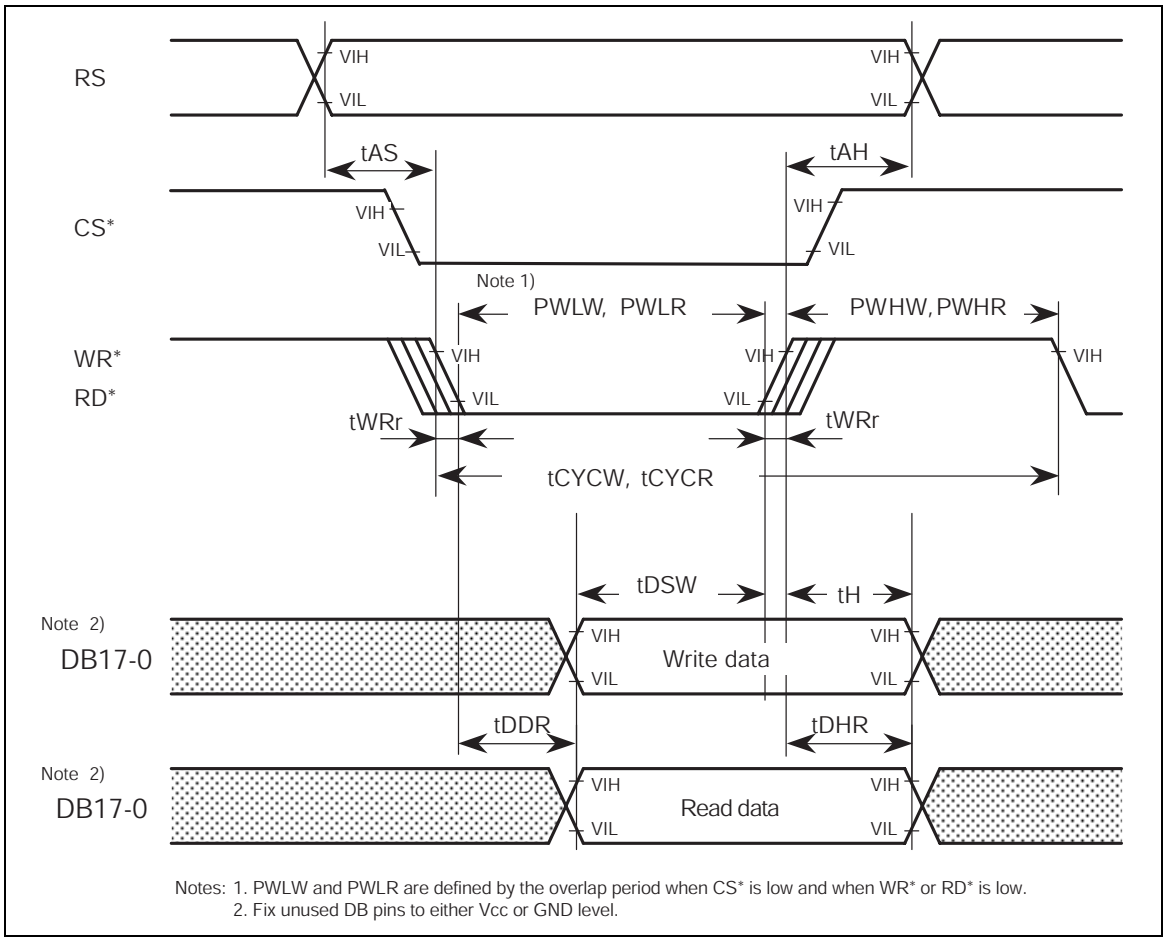


Figure 92

Clock synchronous serial interface

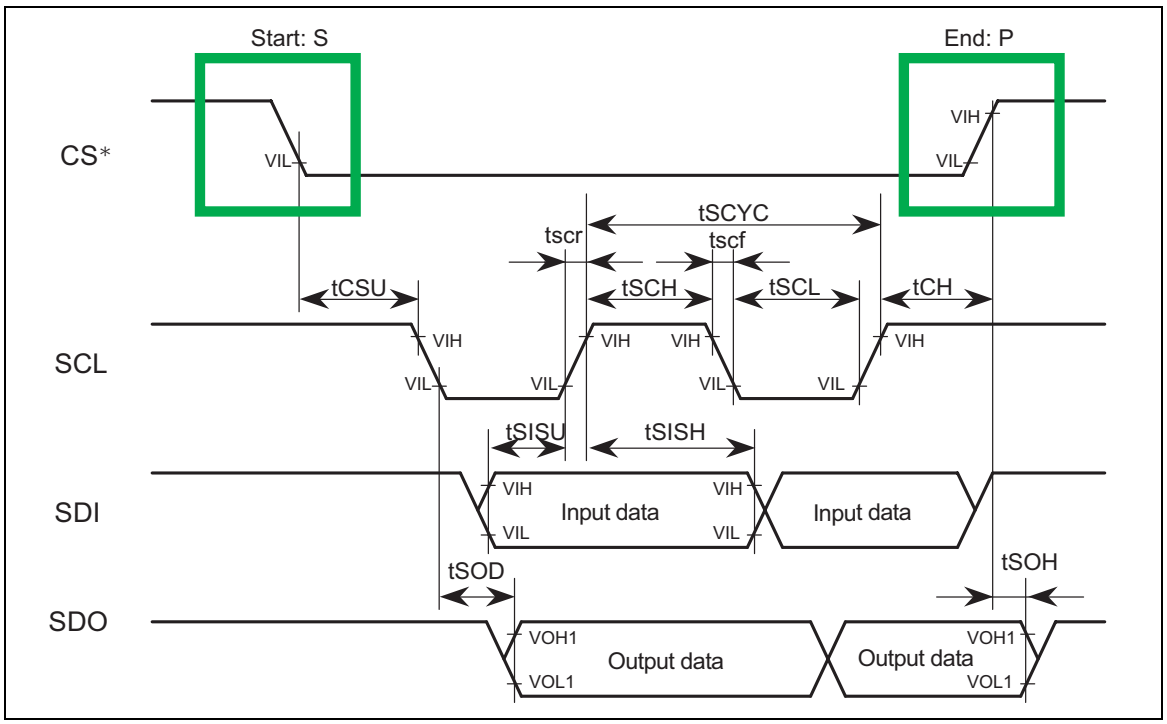


Figure 93

Reset operation

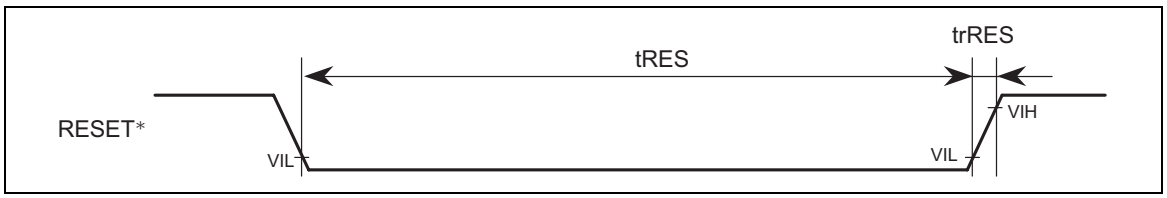


Figure 94

RGB interface

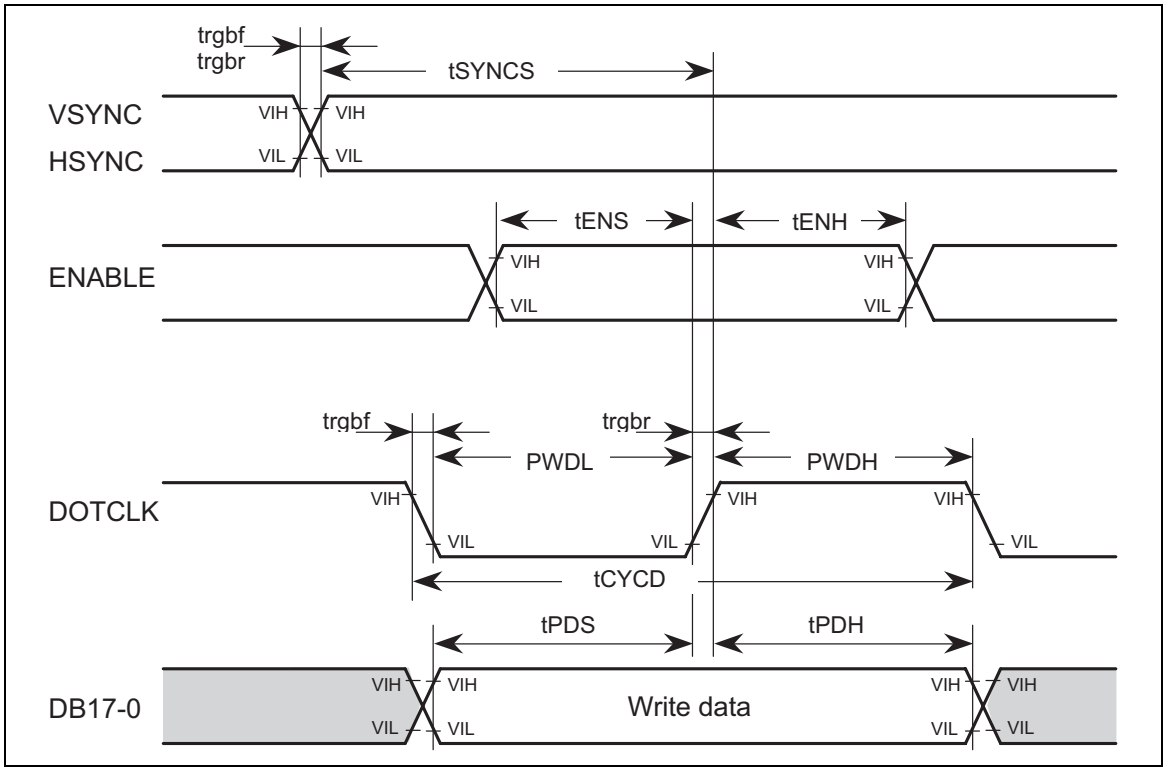


Figure 95

LCD driver output

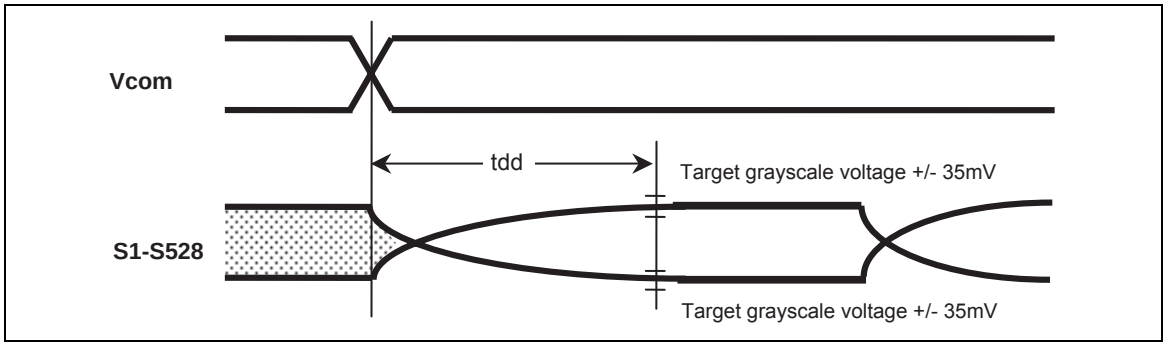


Figure 96

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.21	Jun.28.2006	First issue		
0.22	Aug.25.2006	p.11 Error correction (DB17-10, 8-1 → DB17-13, 11-1) p.13 Vci1→ Vci1 x 2, delete "Connect capacitors where they are required according to the step-up factor." from C13+ ~ C22-. p.14 COM → VON. p.15 AGND → GND. p.78 Error correction (IB9: 0 → DIVI[1], IB8: DIVI[1] → DIVI[0], IB7: DIVI[0] → 0) p.132 Error correction. pp.140-141 Add FLM. p.164 Error correction (7.0±0.3V → 7.5±0.3V), add the write period setting.		
0.23	Sept.4.2006	p.161 Change deep standby sequence. pp.162-163 Add deep standby sequence. p.175 GND → IOGND p.181 Change LCD driver output.		
0.24	Dec.14, 2006	p.42 L7-0 → 0 (IB15-8), 0 → L7-0 (IB7-0) pp.46-47 Change the formats, and add notes. p.174 18 → 38 p.178 Change the chart of driver output delay time, and add a load circuit for testing VCOM output characteristics.		
1.0	Mar.19, 2007	pp.1, 2, 4, 7, 9, 12, 31, 40, 62, 71, 84, 86, 87, 165, 166, 167 EPROM → NV memory. p.7 Change the description of liquid crystal drive. p.10 Change the description of RS. p.11 Change the connection of RESET. p.14 Change the description of VREG1OUT and Vcom. p.17 400 μm → 280 μm. p.48 Add PTDE setting in the table. p.62 Change the range of VREG1OUT. pp.64-65 Correct the order of "Power Control 5" and "Power Control 6". pp.73-74 W/R → W. p.86 Power control 5 → Power control 6, and Power control 6 → Power control 5. p.108 Change the calculation formulas, and add clocks per line in the example. p.125 Change the figure. p.128 Reverse the waveform in the lower figure.		

Rev.	Date	Contents of Modification	Drawn by	Approved by
		p.129 Reverse the waveform and change the numbers in the figure.		
		p.130 17'h0DBA → 17'h0DBAF		
		p.153 VINN → VINN1.		
		p.157 Change the range of VREG1OUT.		
		pp.162-164 Add "RA4h: CALB = 1" and "Wait 1ms or more".		
		p.167 Change the sequences.		
		p.170 Change the specs for IOP1, IOP2, IST, Ici1, and Ici2.		
		p.171 Change the specs for VGH.		
		p.172 Change the specs for tCYCR and PWLR in the tables.		
		pp.177-179 Change the charts.		
1.1	Mar. 29, 2007	p.16 Delete the description of chip and pad.		
		p.130 Delete the description of external display interface from the table.		
		p.172 Change write high-level pulse width (HWM = "1") (50 → 40).		