mosaic

Mosaic Semiconductor Inc.

1M x 32 DRAM

MD321000FKX-80/10/12

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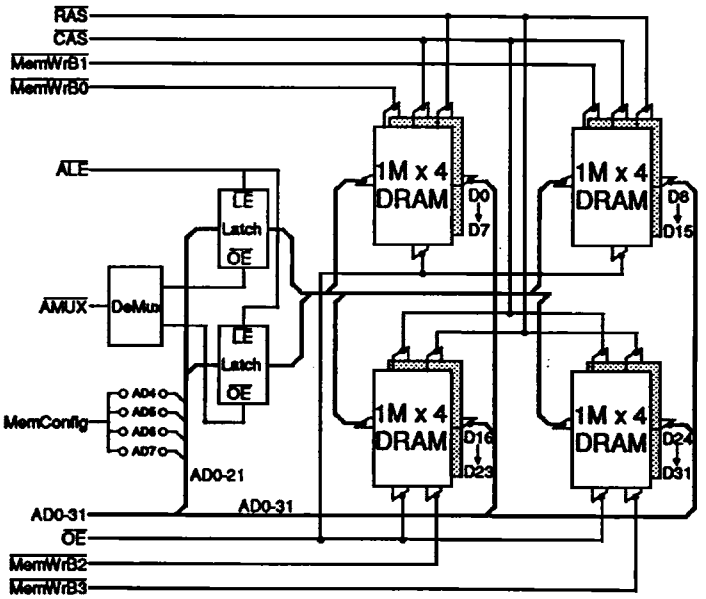
ADVANCE PRODUCT INFORMATION

1,048,576 x 32 CMOS High Speed Dynamic RAM

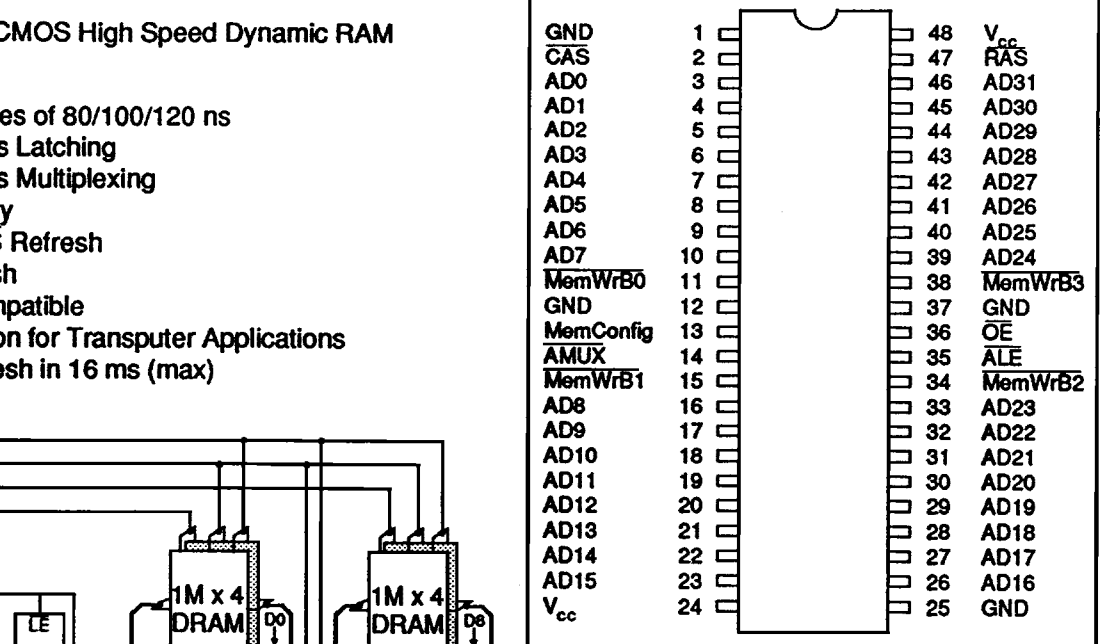
Features

Row Access Times of 80/100/120 ns
Onboard Address Latching
Onboard Address Multiplexing
Byte Write Facility
$\overline{CAS}$ Before $\overline{RAS}$ Refresh
$\overline{RAS}$ Only Refresh
Directly TTL Compatible
MemConfig Option for Transputer Applications
1024 Cycle Refresh in 16 ms (max)

Block Diagram



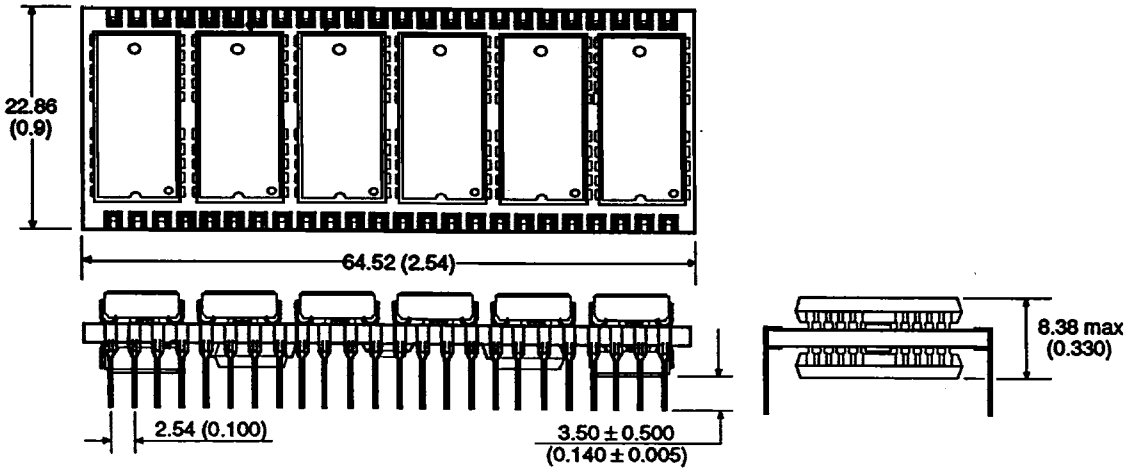
Pin Definition



Pin Functions

AD0-AD31	Address/Data I/O
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{MemWrB0-3}$	Byte Write
$\overline{OE}$	Output Enable
$\overline{AMUX}$	Address Multiplex
$\overline{ALE}$	Address Latch Enable
MemConfig	Configure Memory
V_{cc}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



Absolute Maximum Ratings (1)

Voltage Range on any pin	-1 to $V_{CC}^{+0.3}$	V
Voltage Range on V_{CC}	0 to 7	V
Short Circuit Output Current	50	mA
Power Dissipation	8	W
Storage Temperature	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	-	$V_{CC}^{+0.3}$	V
Input Low Voltage	V_{IL}	-1	-	0.8	V
Output High Voltage	V_{OH}	2.4	-	$V_{CC}^{+0.3}$	V
Output Low Voltage	V_{OL}	-1	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (321000FKXI)

DC Electrical Characteristics (V_{CC}=5V±10%, T_A=0°C to +70°C)

Parameter	*Symbol*	*Test Condition*	*-80*		*-10*		*-12*		*Unit*
			min	*max*	*min*	*max*	*min*	*max*	
Input Leakage Current									
$\overline{CAS}$, $\overline{RAS}$, MemWrB0-3, $\overline{OE}$	I_{IL1}		-80	+80	-80	+80	-80	+80	µA
AD2 - AD19	I_{IL2}		-600	+20	-600	+20	-600	+20	µA
$\overline{ALE}$	I_{IL3}		-1200	+40	-1200	+40	-1200	+40	µA
$\overline{AMUX}$	I_{IL4}		-1800	+60	-1800	+60	-1800	+60	µA
I/O Leakage Current	I_{LIO}		-80	+80	-80	+80	-80	+80	µA
Read/Write Cycle Current	I_{CC1}		-	805	-	725	-	645	mA
Standby Current	I_{CC2}	V_{IH}=5.5V	-	110	-	110	-	110	mA
Average Refresh Current	I_{CC3}		-	805	-	725	-	645	mA

Capacitance (V_{CC}=5V±10%, T_A=25°C)

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
I/P Capacitance	$\overline{CAS}$, $\overline{RAS}$, $\overline{OE}$	C_{IN1}	V_{IN1} = 0V	-	56	pF
	MemWrB0-3	C_{IN2}	V_{IN2} = 0V	-	14	pF
	$\overline{ALE}$	C_{IN3}	V_{IN3} = 0V	-	10	pF
	$\overline{AMUX}$	C_{IN4}	V_{IN4} = 0V	-	15	pF
I/O Capacitance	AD0 - AD31	$C_{I/O}$	$V_{I/O}$ = 0V	-	17	pF

AC Test Conditions

* Input pulse levels: Gnd to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* Vcc=5V±10%

Electrical Characteristics & Recommended AC Operating Conditions

Parameter	Symbol	-80 min	-80 max	-10 min	-10 max	-12 min	-12 max	Unit	Notes
Read Cycle Time	t_{RC}	160	-	190	-	220	-	ns	2
Transition Time	t_T	3	50	3	50	3	50	ns	
Non-static Column Decode Mode									
Pulse Duration, $\overline{RAS}$ Low	t_{RAS}	80	10000	100	10000	120	10000	ns	
Delay Time, $\overline{RAS}$ Low to $\overline{CAS}$ Low	t_{RCD}	22	55	25	75	25	90	ns	8,10
Delay Time, $\overline{CAS}$ Low to $\overline{RAS}$ High	t_{RSH}	25	-	25	-	25	-	ns	8
Pulse Duration, $\overline{RAS}$ High (Precharge)	t_{RP}	70	-	80	-	90	-	ns	
Delay Time, $\overline{RAS}$ Low to $\overline{CAS}$ High	t_{CSH}	80	-	100	-	120	-	ns	
Delay Time, $\overline{CAS}$ High to $\overline{RAS}$ Low	t_{CRP}	10	-	10	-	10	-	ns	
Pulse Duration, $\overline{CAS}$ Low	t_{CAS}	25	10000	25	10000	30	10000	ns	
Column Address Setup Time Before $\overline{CAS}$ Low	t_{ASC}	20	-	20	-	20	-	ns	
Pulse Duration, $\overline{CAS}$ High	t_{CP}	10	-	10	-	10	-	ns	
Row Address Hold Time After $\overline{RAS}$ Low	t_{RAH}	12	-	15	-	15	-	ns	
Row Address Setup Time Before $\overline{RAS}$ Low	t_{ASR}	10	-	10	-	10	-	ns	
Delay Time, Column Address to $\overline{RAS}$ High	t_{RAL}	60	-	65	-	75	-	ns	
Column Address Hold Time After $\overline{RAS}$ Low	t_{AR}	75	-	85	-	110	-	ns	7
Read Hold Time After $\overline{RAS}$ High	t_{RRH}	10	-	10	-	10	-	ns	
Read Setup Time Before $\overline{CAS}$ Low	t_{RCS}	0	-	0	-	0	-	ns	
Column Address Hold Time After $\overline{CAS}$ Low	t_{CAH}	15	-	20	-	25	-	ns	
Read Hold Time After $\overline{CAS}$ High	t_{RCH}	0	-	0	-	0	-	ns	
Access Time From $\overline{CAS}$ Low	t_{CAC}	-	25	-	25	-	30	ns	
Output Disable Time After $\overline{CAS}$ High	t_{OFF}	0	20	0	25	0	30	ns	1
Access Time From $\overline{RAS}$ Low	t_{RAC}	-	80	-	100	-	120	ns	
Access Time From $\overline{OE}$ Low	t_{GAC}	-	25	-	25	-	30	ns	
Output Disable Time After $\overline{OE}$ High	t_{GOFF}	0	20	0	25	0	30	ns	1
Write Cycle Time	t_{WC}	160	-	190	-	220	-	ns	
Write Pulse Duration	t_{WP}	15	-	20	-	25	-	ns	
Write Hold Time After $\overline{RAS}$ Low	t_{WCR}	70	-	85	-	110	-	ns	6 & 7
$\overline{MemWr}$ Low Setup Time Before $\overline{CAS}$ High	t_{CWL}	25	-	25	-	30	-	ns	
$\overline{MemWr}$ Low Setup Time Before $\overline{CAS}$ Low	t_{WCS}	0	-	0	-	0	-	ns	6
Write Hold Time After $\overline{CAS}$ Low	t_{WCH}	15	-	20	-	25	-	ns	
$\overline{MemWr}$ Low Setup Time Before RAS High	t_{RWL}	25	-	25	-	30	-	ns	
Data Setup Time Before $\overline{CAS}$ Low	t_{DSC}	0	-	0	-	0	-	ns	5
Data Hold Time After $\overline{CAS}$ Low	t_{DHC}	15	-	20	-	25	-	ns	5
Data Hold Time After $\overline{RAS}$ Low	t_{DHR}	75	-	90	-	120	-	ns	7
Data Setup Time Before $\overline{MemWr}$ Low	t_{DSW}	0	-	0	-	0	-	ns	5
Data Hold Time After $\overline{MemWr}$ Low	t_{DHW}	15	-	20	-	25	-	ns	5
Delay Time, $\overline{OE}$ High Before Data valid	t_{GDD}	25	-	25	-	30	-	ns	
Delay Time $\overline{RAS}$ high to $\overline{CAS}$ low	t_{RPC}	10	-	10	-	10	-	ns	3
Delay Time $\overline{CAS}$ low to $\overline{RAS}$ low	t_{CSR}	10	-	10	-	10	-	ns	3
Delay Time RAS low to CAS high	t_{CHR}	20	-	20	-	25	-	ns	3
Delay Time Address valid to ALE low	t_{LAL}	10	-	10	-	10	-	ns	
Delay Time $\overline{ALE}$ low to Address not valid	t_{LHL}	13	-	13	-	13	-	ns	
Delay Time ALE high to Address valid	t_{LHH}	13	-	13	-	13	-	ns	
$\overline{ALE}$ Pulse Duration, High	t_{LP}	4	-	4	-	4	-	ns	
Address Latch Setup Time	t_{LRS}	13	-	13	-	13	-	ns	

Notes :

1. t_{OFF} and t_{GOFF} are specified when the output is no longer driven.
2. All cycle times assume t_T=5ns.
3. $\overline{CAS}$ before $\overline{RAS}$ refresh only.
5. Later of $\overline{CAS}$ or $\overline{MemWr}$ in write operation.
6. Early write operation only.
7. The minimum value is measured when t_{RAD} is set to t_{RAD} min as a reference.
8. Read cycle only.
9. Write cycle only.
10. Maximum value specified only to guarantee access time.

DESCRIPTION

The MD321000FKX is a high speed 33,554,432 bit Dynamic Random Access Memory organised as 1,048,576 words of 32 bits each. Although designed primarily for use with Transputers, it can be used with any system which supports Dynamic Memory and a 32 bit Multiplexed Address / Data Bus. Information on interfacing this part with both Transputers and other systems is given below.

TRANSPUTER OPERATION

Four different Memory Configuration options are provided via the MemConfig pin. This pin is connected, at the manufacturing stage, to one of the Address / Data pins AD4, AD5, AD6, AD7, the particular option specified by the customer when ordering. This allows for a wide range of memory speed and Transputer speed configurations to be used, depending on the application, as shown in the table below.

MEMORY SPEED (ns)	TRANSPUTER SPEED MHz											
	20				25				30			
	AD LINK				AD LINK				AD LINK			
	4	5	6	7	4	5	6	7	4	5	6	7
80	●	●	●	●	●	●	●	●				●
100	●	●	●	●				●				●
120				●				●				●

● Indicates allowable combination.

Connections to the Transputer are as follows :

Transputer Pin	*MD321000 Pin*
MemnotWrD0	AD0
MemnotRfD1	AD1
MemAD2-MemAD31	AD2-AD31
notMemS0	$\overline{ALE}$
notMemS1	$\overline{RAS}$
notMemS2	$\overline{AMUX}$
notMemS3	$\overline{CAS}$
MemConfig	MemConfig
notMemRd	$\overline{OE}$
notMemWrB0-3	$\overline{MemWrB0\text{-}3}$

GENERAL OPERATION

The MD321000 is a 1M x 32 bit Dynamic Memory with a multiplexed Address / Data bus. This device has on board address latches and address multiplexing, which reduces the complexity of external circuitry. This data sheet descibes the use of this memory in normal READ and WRITE modes and EARLY WRITE mode, as well as two types of REFRESH.

Address AD2 - AD21

20 Address bits are required to decode 1 of 1M locations. This 20 bit address is converted by the on board circuitry to two 10 bit addresses for use by the 1M x 4 DRAMS used, and strobed into the DRAMS by using the $\overline{RAS}$ and $\overline{CAS}$ control inputs.

$\overline{MemWrB0}$ - $\overline{MemWrB3}$

The READ or WRITE mode is selected by these inputs, a separate input provided for each byte, the least significant byte controlled by $\overline{MemWrB0}$. A logic high on these inputs selects the READ mode and a logic low selects the WRITE mode. The data input is disabled when READ mode is selected. When $\overline{MemWrB0\text{-}3}$ go low prior to $\overline{CAS}$ (early write), data out will remain in the high impedance state for the entire cycle, permitting a WRITE operation with $\overline{OE}$ grounded.

Data IN AD0 - AD31

Data is written during a WRITE or EARLY WRITE cycle. In an EARLY WRITE cycle, $\overline{MemWrB0\text{-}3}$ are brought low before $\overline{CAS}$ and the data is strobed by $\overline{CAS}$. In a WRITE cycle, $\overline{CAS}$ is already low so the data is strobed in by MemWrB0-3; note that $\overline{OE}$ must be high to put the output buffers into a high impedance state before placing data onto AD0 - AD31.

See diagrams showing WRITE and EARLY WRITE-waveforms for detailed timing.

Data OUT AD0 - AD31

The three state output buffer is in the high impedance state until both $\overline{CAS}$ and $\overline{RAS}$ are brought low. In a READ cycle the output becomes valid after the access time interval t_{CAC}, and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ going high returns it to the high impedance state.

See diagram showing READ waveform for detailed timing.

Output Enable $\overline{OE}$

When $\overline{OE}$ is high the output buffers are in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will place the output buffers in the low impedance state, as long as $\overline{RAS}$ and $\overline{CAS}$ are low as well. If either $\overline{OE}$ or $\overline{CAS}$ are brought high the buffers will return to the high impedance state.

Address Latch Enable $\overline{ALE}$

On the high to low transition of $\overline{ALE}$ the address on the lines AD2 - AD21 is latched, and remains latched until $\overline{ALE}$ goes high. With $\overline{ALE}$ high these latches operate transparently i.e. the data on the outputs follows the inputs.

Address Latch Multiplex $\overline{AMUX}$

When $\overline{AMUX}$ is high the address on AD2 - AD11 (row address) is presented to the DRAMS and is latched onto them when $\overline{RAS}$ goes low. When $\overline{AMUX}$ is low the address on AD12 - AD21 is used, and latched onto the DRAMS when $\overline{CAS}$ goes low.

Refresh $\overline{RAS}$ Only

A refresh operation must be performed once every 16ms to retain stored data, achieved by strobing one of the 1024 rows. A normal READ or WRITE cycle will refresh all of the bits in each row that is selected. For $\overline{RAS}$ only refresh, $\overline{CAS}$ is held high and an externally generated row address must be supplied on AD2 - AD11.

See diagram showing $\overline{RAS}$ only refresh for detailed timing.

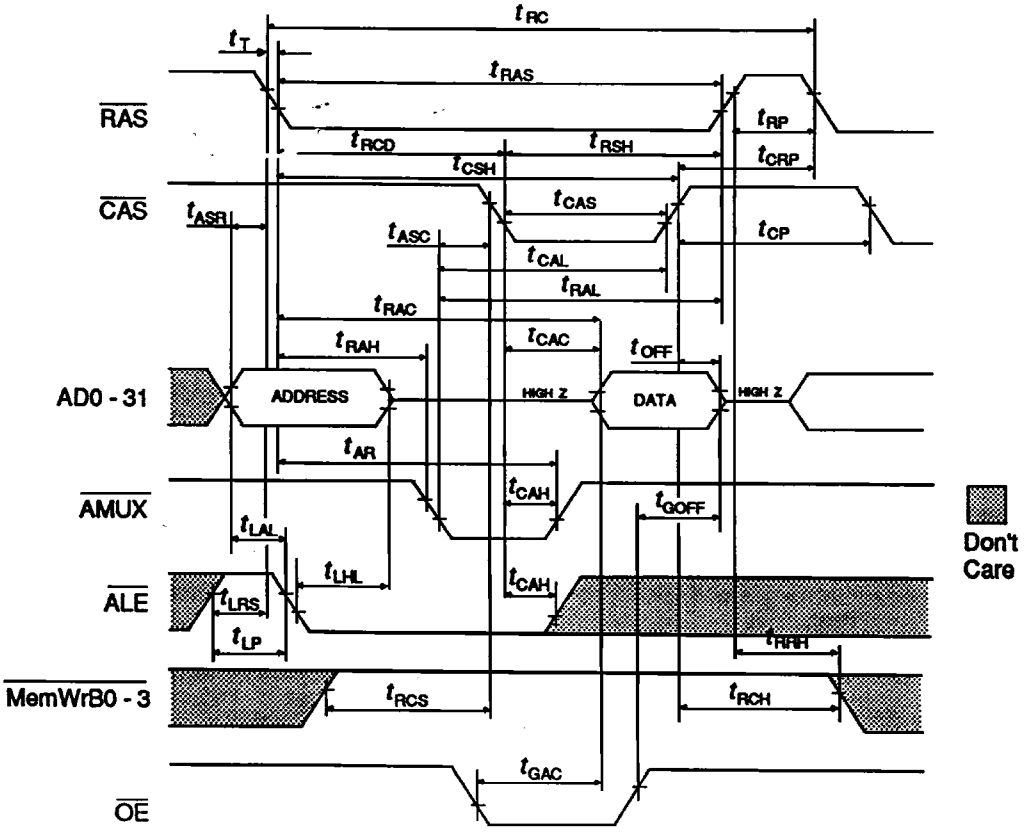
Refresh $\overline{CAS}$ Before $\overline{RAS}$

The refresh address can be generated automatically by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ and holding it low while cycling $\overline{RAS}$. In this mode the external address is ignored.

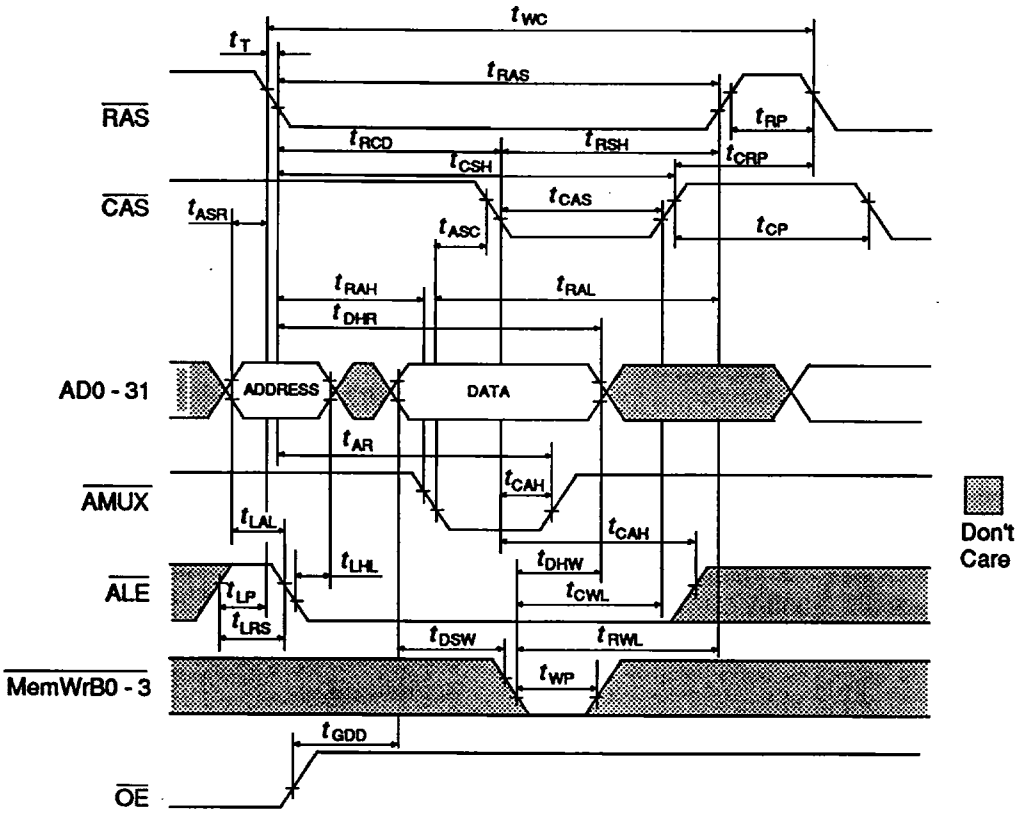
Power Up

To achieve correct device operation, after V_{CC} has reached its full level a delay of 200µs is required followed by eight initialisation cycles (READ, WRITE or REFRESH).

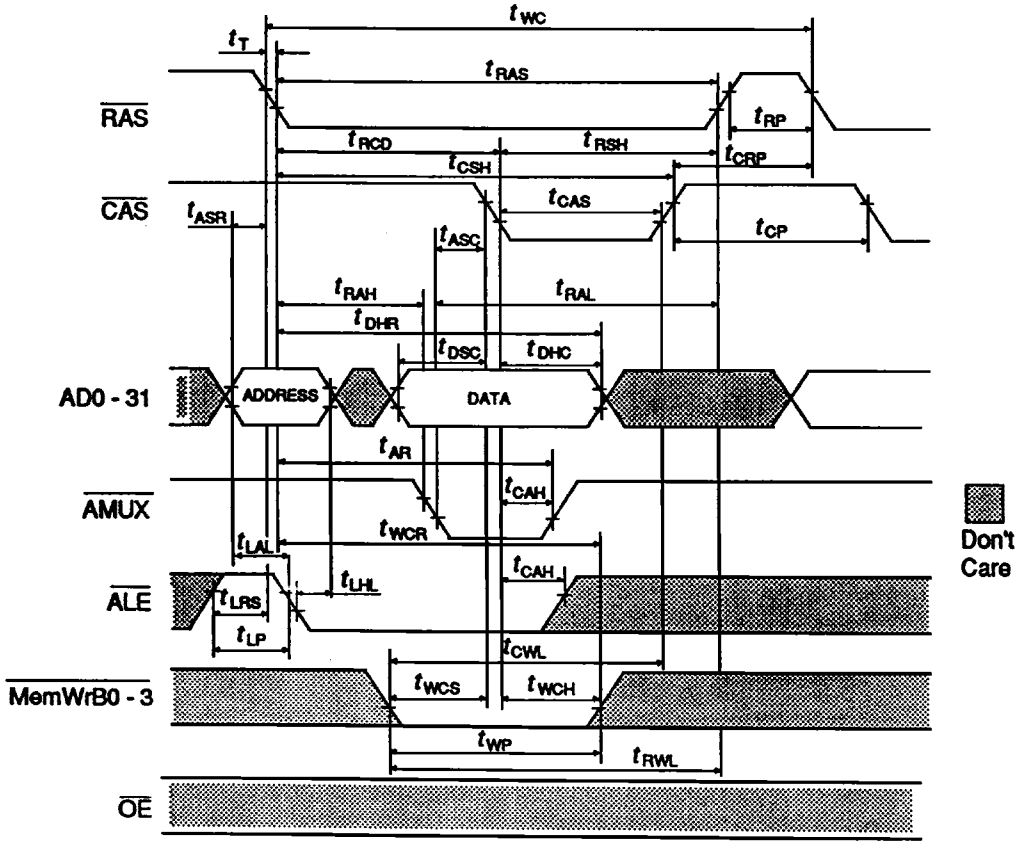
Read Cycle Timing Waveform



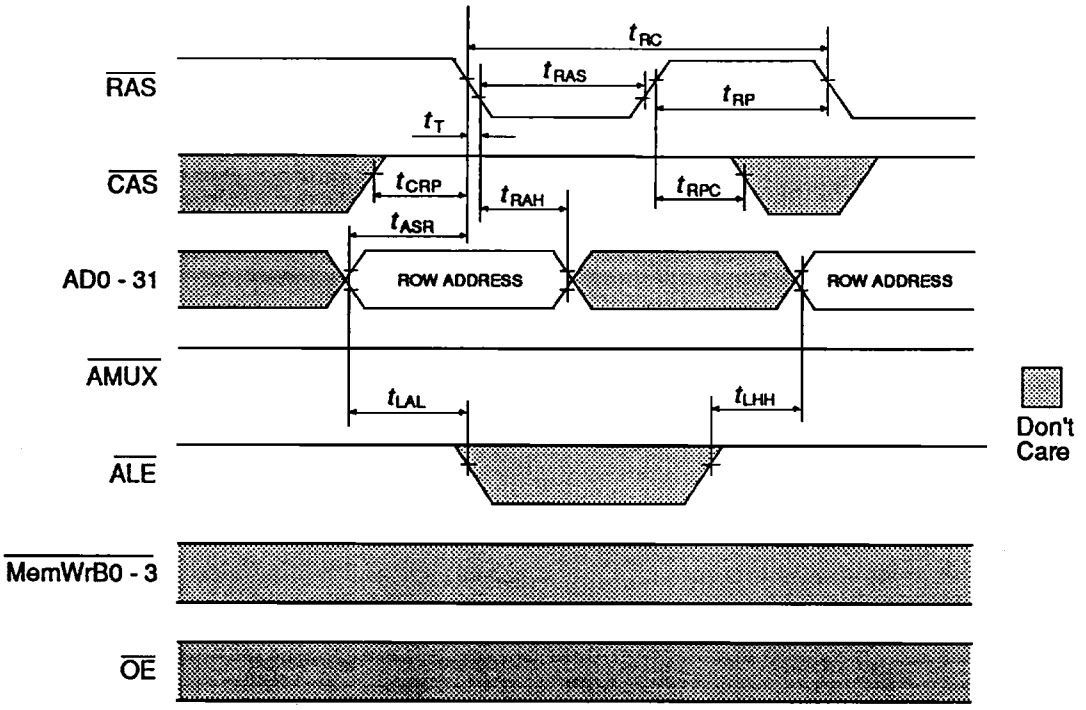
Write Cycle Timing Waveform



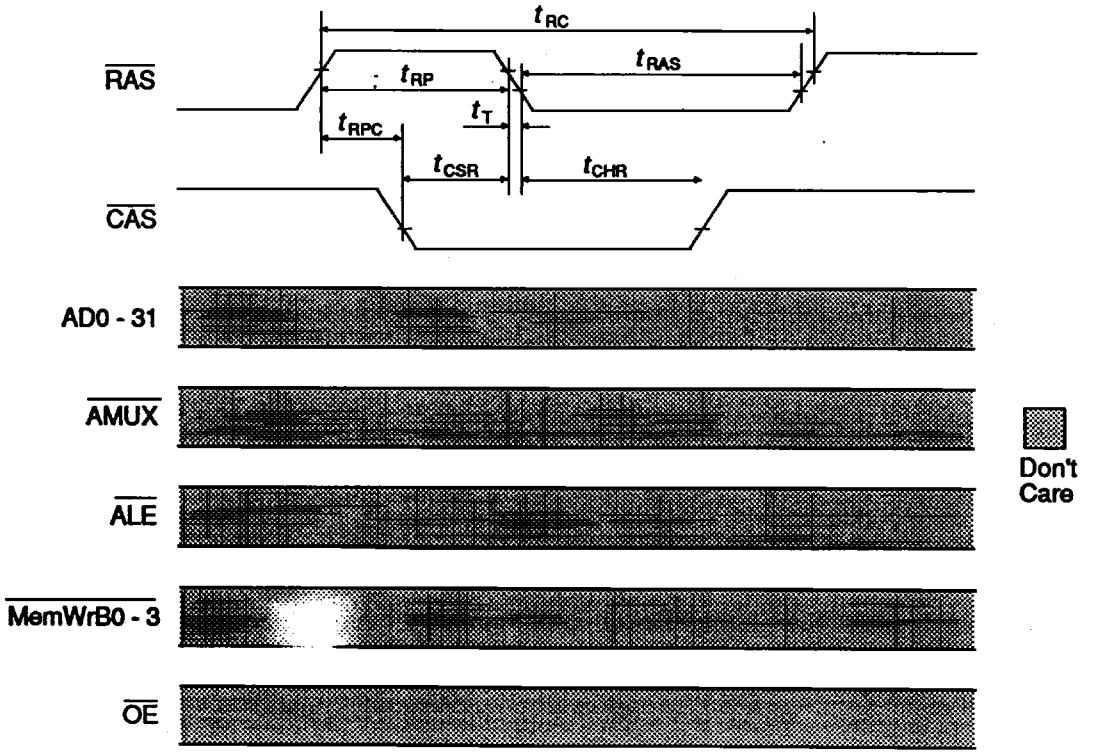
Early Write Cycle Timing Waveform



Refresh $\overline{RAS}$ Only

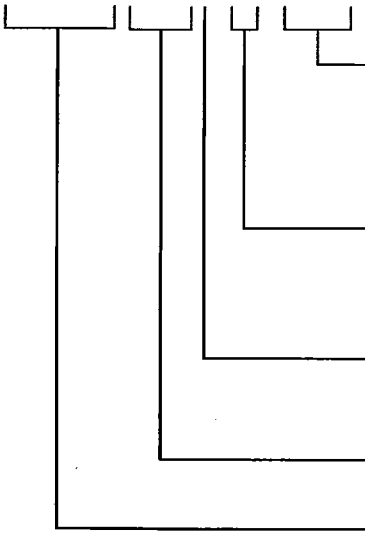


Refresh $\overline{CAS}$ Before $\overline{RAS}$



Ordering Information

MD321000FKXI-12 /AD4



Transputer Option	AD4	= Link to MemAD4
	AD5	= Link to MemAD5
	AD6	= Link to MemAD6
	AD7	= Link to MemAD7
Module Speed	80	= 80 ns
	10	= 100 ns
	12	= 120 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
Package	FKX	= Plastic DIL
Memory Arrangement	321000	= 1M x 32 bit

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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