

MAX20082

Dual, Redundant, H-Bridge Motor Driver with ASIL Diagnostics

General Description

The MAX20082 is a dual, full-bridge controller specifically designed for fault-tolerant automotive applications with high-power inductive loads such as brushed DC motors. The device has two fully independent motor-control channels designed for use with external n-channel power MOSFETs. Each channel operates from a 4.75V to 5.25V input supply voltage range, and is capable of working with motor supply voltages up to 35V.

A charge-pump regulator provides 9.8V gate drive with a 5V input supply voltage. A bootstrap capacitor is used to provide the voltage above the input battery voltage necessary to drive the high-side n-channel MOSFETs in the H-bridge. An internal top-off charge pump for the high-side drive allows DC (100% duty cycle) operation.

The device also includes programmable dead time, gate-drive slew rate, and MOSFET short-circuit threshold. The H-bridge can be driven in forward mode (clockwise), reverse mode (counterclockwise), braking mode, and coast mode. In braking mode, both the low-side MOSFETs are turned on (synchronous slow decay). In coast mode, all the MOSFETs in the H-bridge are off (asynchronous fast decay). The power MOSFETs are protected from shoot-through by a resistor-adjustable dead-time circuit.

Each channel also integrates a low-side current-sense amplifier. Used for sensing motor (H-bridge) current, the current-sense amplifier includes an overcurrent-protection circuit to limit the current in the event of motor faults.

Integrated diagnostics provide indication of undervoltage, overtemperature, H-bridge, and pin faults and can be configured to protect the power MOSFETs under most short-circuit conditions. In addition, the device supports implementation in ASIL systems by having two completely redundant H-bridge drivers in one package. The two channels are completely independent and fully redundant, with no shared pins or functions.

The MAX20082 is specified for operation over the full -40°C to $+125^{\circ}\text{C}$ ambient temperature range. The maximum junction temperature is 150°C , with thermal shutdown at 170°C (typ). The device is available in a 56-pin, 14mm x 6.1mm, TSSOP package.

[Ordering Information](#) appears at end of data sheet.

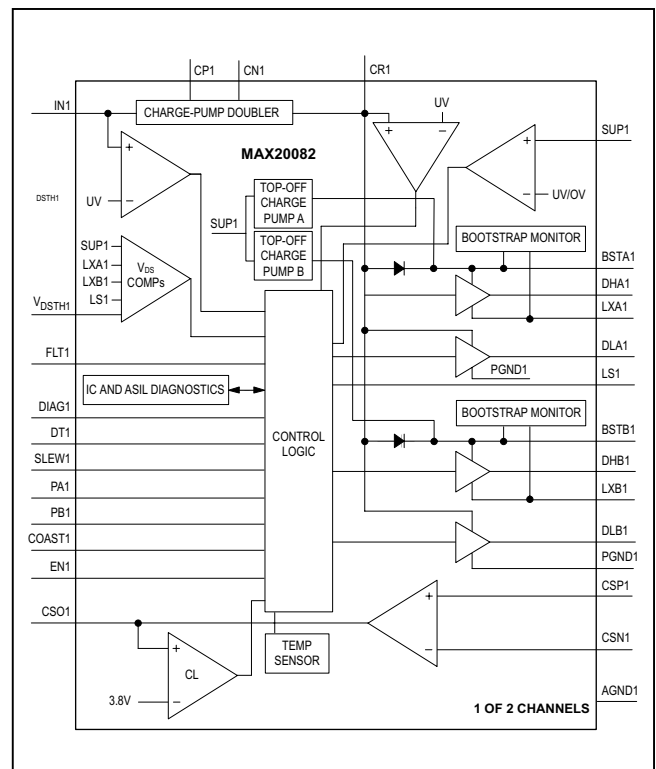
Benefits and Features

- Comprehensive IC Diagnostics Detect Both IC and H-Bridge Faults, Enhancing System Safety
- Both Channels are Fully Independent Without Any Shared Pins or Circuitry, Providing Complete Redundancy
- Resistor-Programmable Functionality Simplifies Software Development
- All nFET Operation, Including 100% Duty Cycle, Saves System Cost

Applications

- Automotive Motor Drivers
- Industrial Motor Drivers

Block Diagram



Absolute Maximum Ratings

| | | |
|---------------------|-------------------------------------|--|
| SUP_ to AGND_ | -0.3V to +40V | COAST_, PA_, PB_, EN_, DIAG_, V _{DSTH} , |
| LXA_, LXB_ to AGND_ | -4V to +40V | SLEW_, DT_, CSO_ to AGND_ |
| BSTA_ to LXA_ | -0.3V to +12V |-0.3V to + (V _{IN} + 0.3V) |
| BSTB_ to LXB_ | -0.3V to +12V | FLT_, LS_, CSP_, CSN_ to AGND_ |
| DHA_ to LXA_ | -0.3V to V _{BST} + 0.3V |-0.3V to + 6V |
| DHB_ to LXB_ | -0.3V to V _{BST} + 0.3V | PGND_ to AGND_ |
| CR_ to AGND_ | -0.3V to +12V |-0.3V to 0.3V |
| CN_ to AGND_ | -0.3V to (V _{IN} + 0.3V) | Continuous Power Dissipation (T _A = +70°C) TSSOP on |
| CP_ to CN_ | -0.3V to + 6V | Multilayer Board (derate 10.8mW/°C above +70°C) ...860mW |
| DLA_, DLB_ to AGND_ | -0.3V to + (V _{CR} + 0.3V) | Operating Ambient Temperature Range..... -40°C to +125°C |
| IN_ to AGND_ | -0.3V to +6V | Storage Temperature Range..... -55°C to +150°C |
| | | Maximum Junction Temperature..... +150°C |
| | | Lead Temperature (soldering, 10s)..... +300°C |
| | | Soldering Temperature (reflow)..... +260°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

| | | |
|---|-------------|---|
| TSSOP | | |
| Junction-to-Ambient Thermal Resistance (θ _{JA}) |93°C/W | Junction-to-Case Thermal Resistance (θ _{JC}).....21°C/W |

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(Electrical characteristics valid at T_A = T_J = -40°C to 125°C, V_{IN} = 5V, V_{SUP} = 14V, V_{EN} = V_{DIAG} = 3.3V, DH_ and DL_ open, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------------|-----------------------|---|------|------|------|-------|
| Input Supply Voltage Range | V _{IN} | | 4.75 | | 5.25 | V |
| Input Supply Undervoltage Lockout | V _{INPUV} | Rising | 4 | 4.2 | 4.5 | V |
| | V _{INUVHYS} | Hysteresis | | 200 | | mV |
| Start-Up Timer | t _{START_UP} | From EN_ going high to V _{CR} > CR _{UV_ON} , DIAG_ = low | | 13.5 | 20 | ms |
| | | From EN_ going high to V _{CR} > CR _{UV_ON} , DIAG_ = high | | 1.7 | 2 | |
| Single-Channel Supply Current | I _{IN_Q} | FLT_ and CSO_ pin unconnected | | 1.7 | 3 | mA |
| | | V _{EN} = V _{PA} = V _{PB} = V _{DIAG} = V _{COAST} = 0V | | | 10 | µA |
| CR_ OUTPUT | | | | | | |
| CR_ Output Voltage | V _{CR} | I _{CR} = 3mA, C _{CP} = 330nF, CR_ = 3.3µF | 9.4 | 9.7 | | V |
| | | I _{CR} = 3mA, V _{IN} = 4.75V | 8.9 | 9.2 | | |
| CR_ Undervoltage Lockout | CR _{UV_ON} | Rising | 6.65 | 7 | 7.35 | V |
| | CR _{UV_OFF} | Hysteresis | | 500 | | mV |
| CR_ Charge Timeout | CR _{TO} | V _{CR} from 0V to CR _{UV_ON} | 1.4 | 1.6 | 1.8 | ms |

Electrical Characteristics (continued)

(Electrical characteristics valid at $T_A = T_J = -40^\circ\text{C}$ to 125°C , $V_{IN_} = 5\text{V}$, $V_{SUP_} = 14\text{V}$, $V_{EN_} = V_{DIAG_} = 3.3\text{V}$, $DH_$ and $DL_$ open, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------|--|------------------|------|-----|-------|
| BOOTSTRAP CIRCUIT | | | | | | |
| Bootstrap Voltage Drop | $V_{BST_}$ | $V_{LX_} = 0\text{V}$, $I_{SOURCE} = 10\text{mA}$ | $V_{CR_} - 0.2$ | | | V |
| Bootstrap Input Current | $I_{BST_}$ | $V_{BST_} = 24\text{V}$, $V_{LX_} = 14\text{V}$ | | 0.3 | 0.6 | mA |
| BST_Charge Timeout | BST_{TO} | $V_{BST_}$ from 0V to $V_{BOOSTUV}$, \overline{COAST} rising | 0.7 | 0.8 | 0.9 | ms |
| Bootstrap Undervoltage Threshold | $V_{BOOSTUV}$ | Rising ($V_{BSTA_}$ to $V_{LXA_}$ or V_{BST_B} to $V_{LXB_}$) | 6.7 | 7.2 | 7.6 | V |
| | $V_{BOOSTUVHYS}$ | Hysteresis ($V_{BSTA_}$ to $V_{LXA_}$ or V_{BST_B} to $V_{LXB_}$) | | 1 | | V |
| Top-Off Charge-Pump Enable Delay | $T_{TO_EN_DLY}$ | $PA_$, $PB_$ rising | 0.5 | 0.6 | 0.7 | ms |
| GATE DRIVE | | | | | | |
| Output-Voltage High $DH_$ to $LX_$ | V_{DH_HIGH} | $V_{BST_} = 9.5\text{V}$, $I_{SOURCE} = 10\text{mA}$, $R_{SLEW_} = 10\text{k}\Omega$ | 9.1 | 9.3 | | V |
| | | $V_{BST_} = \text{unconnected}$, $V_{CR_} = 9.8\text{V}$, $I_{SOURCE} = 25\mu\text{A}$ | 6.6 | 7.7 | | |
| Output-Voltage Low $DH_$ to $LX_$ | V_{DH_LOW} | $I_{SINK} = 10\text{mA}$ | | 0.2 | 0.5 | V |
| Output-Voltage High $DL_$ to $PGND_$ | V_{DL_HIGH} | $I_{SOURCE} = 10\text{mA}$, $R_{SLEW_} = 10\text{k}\Omega$, $V_{CR_} = 9.5\text{V}$ | 9.1 | 9.3 | | V |
| Output-Voltage Low $DL_$ to $PGND_$ | V_{DL_LOW} | $I_{SINK} = 10\text{mA}$ | | 0.2 | 0.5 | V |
| Turn-Off Propagation Delay | t_{OFF} | See Figure 4 for timing characteristics | 60 | 100 | 150 | ns |
| Turn-On Propagation Delay | t_{ON} | See Figure 4 for timing characteristics | 60 | 100 | 150 | ns |
| Propagation Delay Matching | | | | 10 | | ns |
| Dead Time | t_{DEAD} | $R_{DT_} = 10\text{k}\Omega$ (see Figure 4 for timing characteristics) | | 370 | | ns |
| | | $R_{DT_} = 40\text{k}\Omega$ (see Figure 4 for timing characteristics) | | 1100 | | |
| | | $R_{DT_} = 100\text{k}\Omega$ (see Figure 4 for timing characteristics) | | 2500 | | |
| | | $R_{DT_} = 200\text{k}\Omega$ (see Figure 4 for timing characteristics) | | 5000 | | |
| Slew Current | I_{SLEW} | $R_{SLEW_} = 10\text{k}\Omega$ | | 40 | | mA |
| | | $R_{SLEW_} = 50\text{k}\Omega$, $V_{DL_} = V_{DH_} = 5\text{V}$, $V_{LX_} = 0\text{V}$ | | 8 | | mA |
| | | $R_{SLEW_} = 200\text{k}\Omega$ | | 2 | | mA |

Electrical Characteristics (continued)

(Electrical characteristics valid at $T_A = T_J = -40^\circ\text{C}$ to 125°C , $V_{IN_} = 5\text{V}$, $V_{SUP_} = 14\text{V}$, $V_{EN_} = V_{DIAG_} = 3.3\text{V}$, $DH_$ and $DL_$ open, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|-------------------|--|------|------|------|------------------|
| CURRENT-SENSE AMPLIFIER | | | | | | |
| Input Common-Mode Voltage Range | CMVR | | 0 | | 3 | V |
| Input Offset Voltage | V_{OFF} | | -1.5 | | +1.5 | mV |
| Input Bias Current | I_{BIAS} | | | 200 | -600 | nA |
| Input Offset Current | I_{OFF} | | | 20 | | nA |
| Differential DC Voltage Gain | | $R_{CSO_} = 2\text{k}\Omega$ | 90 | 105 | | dB |
| Input Capacitance | C_{CS_IN} | | | 5 | | pF |
| Output Voltage Range | $V_{CSO_}$ | $I_{CSO_} = \pm 3\text{mA}$ | 0.5 | | 4.5 | V |
| Output Sink Current | I_{CSO_sink} | $V_{CSO_} = 0\text{V}$ | 10 | | 50 | mA |
| Output Source Current | I_{CSO_SOURCE} | $V_{CSO_} = 5\text{V}$ | 14 | | 54 | mA |
| Output Slew Rate | SR | Gain > 10, $C_{LOAD} = 100\text{pF}$ | | 10 | | V/ μs |
| DC Common-Mode Rejection | CMR | | 81 | 100 | | dB |
| Gain-Bandwidth Product | GBW | $C_{LOAD} = 100\text{pF}$ | | 30 | | MHz |
| Phase Margin | SR | $C_{LOAD} = 100\text{pF}$, gain = 10 | | 66 | | ° |
| OVERCURRENT PROTECTION | | | | | | |
| Overcurrent Threshold | V_{OC} | $V_{CSO_}$ rising | 3.5 | 3.75 | 4 | V |
| Overcurrent Threshold Hysteresis | V_{OC_HYS} | | | 0.2 | | V |
| V_{DS} PROTECTION | | | | | | |
| $V_{DSTH_}$ Input Voltage Range | V_{DS_RNG} | | 0.2 | | 2 | V |
| $V_{DSTH_}$ Accuracy | V_{DS_ACC} | $V_{DSTH_} = 0.5\text{V}$ | -50 | | -60 | mV |
| $V_{DSTH_}$ Input Current | $V_{DSTH_}$ | | | 0.1 | 1 | μA |
| $V_{DSTH_}$ Disable Voltage | V_{DS_DIS} | | 2.6 | | | V |
| $V_{DSTH_}$ Fault Blanking Time | t_{VDS_BLANK} | From dead time elapsed | 12 | 15 | 18 | μs |
| $V_{DSTH_}$ Comp Propagation Delay | t_{VDS_DEL} | From fault time elapsed, 100mV overdrive | | 1 | | μs |
| LX_ Input Current | I_{LX} | $V_{EN_} = 0\text{V}$, $V_{LX_} = 0$ to 16V, no switching | | | 250 | μA |
| SUP_ Input Current | $I_{SUP_}$ | | | 50 | 100 | μA |
| LS_ Input Current | $I_{LS_}$ | | | | 30 | μA |

Electrical Characteristics (continued)

(Electrical characteristics valid at $T_A = T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN_} = 5\text{V}$, $V_{SUP_} = 14\text{V}$, $V_{EN_} = V_{DIAG_} = 3.3\text{V}$, $DH_$ and $DL_$ open, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------|---|-----|------|-----|---------------|
| SUP_ INPUT PROTECTION | | | | | | |
| Overvoltage Blanking Time | t_{BLANK_OV} | | 350 | 400 | 450 | ms |
| SUP_ Undervoltage Lockout | SUP_UV | Rising | 4.2 | 4.6 | 5 | V |
| | SUP_UV_HYS | Hysteresis | | 300 | | mV |
| SUP_ Overvoltage Lockout | SUP_OV | Rising, more than t_{BLANK_OV} | 35 | 36.5 | 38 | V |
| | SUP_OV_HYS | Hysteresis | | 1.2 | | V |
| THERMAL PROTECTION | | | | | | |
| Overtemperature Fault Threshold | T_JFT_R | Rising | | 170 | | °C |
| | T_JFT_F | Falling | | 145 | | |
| FAULT FLAG | | | | | | |
| Fault Output, Low State | V_{FLT_LOW} | $I_{SINK} = 1\text{mA}$ | | | 0.3 | V |
| Fault Output Leakage, High State | I_{FLT_HIGH} | $V_{FLT_} = 5\text{V}$ | -1 | | +1 | μA |
| Fault Class 1 | %FLT_1 | | | 12.5 | | % |
| | | DIAG_ low during pin-to-pin check routine | | 62.5 | | |
| Fault Class 2 | %FLT_2 | | | 25 | | % |
| Fault Class 3 | %FLT_3 | | | 50 | | % |
| Fault Class 4 | %FLT_4 | | | 75 | | % |
| Fault Class 5 | %FLT_5 | | | 87.5 | | % |
| Fault Frequency | $f_{FLT_}$ | | 550 | 625 | 700 | kHz |
| EN_, COAST_, PA_, PB_, and DIAG_ LOGIC INPUTS | | | | | | |
| Input High Voltage | IN_{VIH} | | 2 | | | V |
| Input Low Voltage | IN_{VIL} | | | | 0.7 | V |
| Input Leakage Current | IN_{LKG} | Input voltage from 0 to 5.5V | -1 | | +1 | μA |
| EN_ Deglitch Time | t_{RES} | Note 3 | 7 | 10 | 13 | μs |
| EN_ Pulldown Resistor | EN_RES | | | 50 | | k Ω |
| EN_ Low Time to Enter Shutdown Mode | t_{SHDW} | Note 4 | 0.8 | 1 | 1.2 | ms |

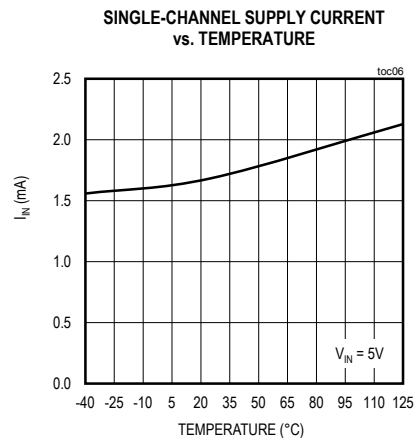
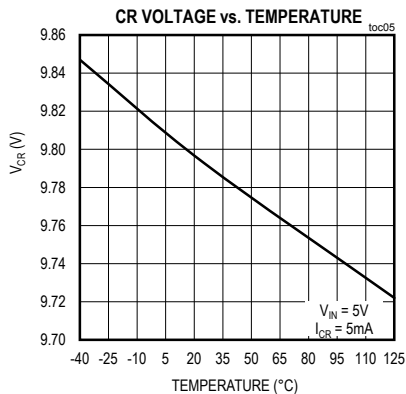
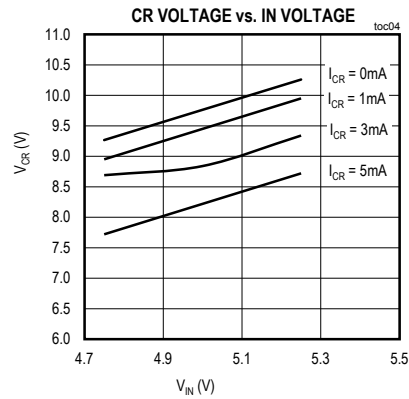
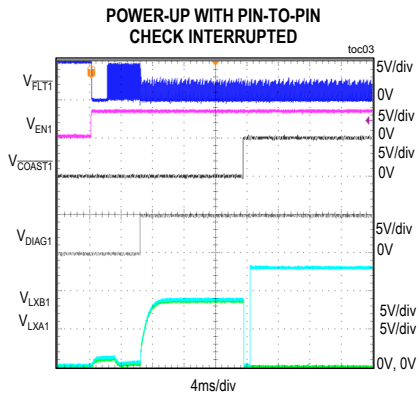
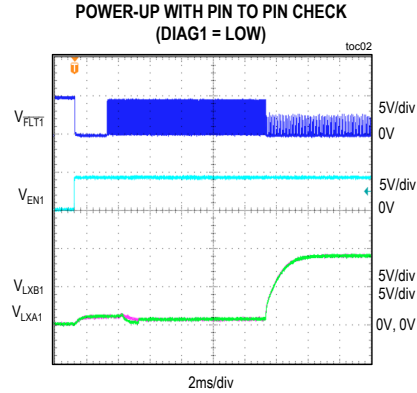
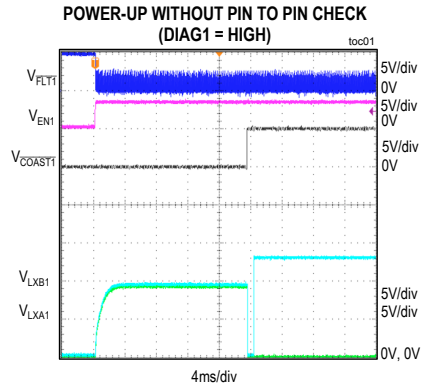
Note 2: Limits are 100% tested at $T_A = +25^{\circ}\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 3: Minimum time EN_ has to be low in order to enter reset state.

Note 4: Minimum time EN_ has to stay low after a power-up in order to enter shutdown mode.

Typical Operating Characteristics

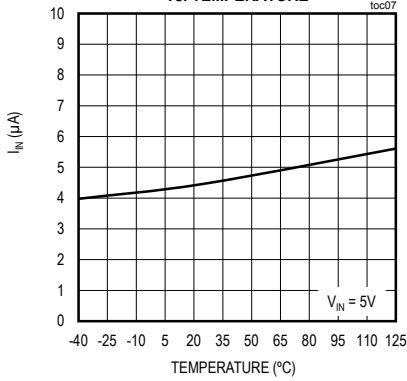
($V_{IN_}$ = 5V, $V_{SUP_}$ = 14V, $V_{EN_}$ = $V_{DIAG_}$ = 3.3V, unless otherwise noted.)



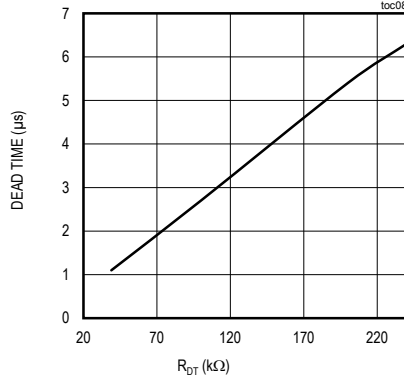
Typical Operating Characteristics (continued)

($V_{IN_}$ = 5V, $V_{SUP_}$ = 14V, $V_{EN_}$ = $V_{DIAG_}$ = 3.3V, unless otherwise noted.)

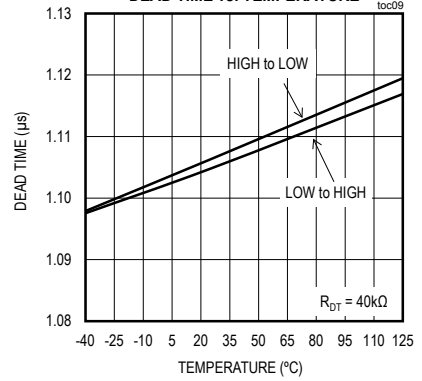
SINGLE-CHANNEL SHUTDOWN CURRENT vs. TEMPERATURE



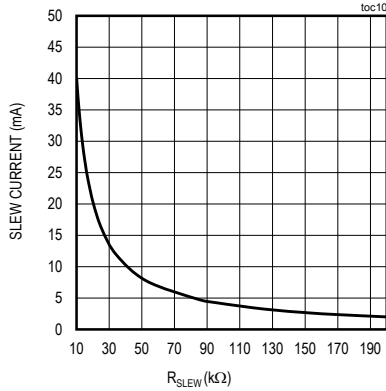
DEAD TIME vs. R_DT



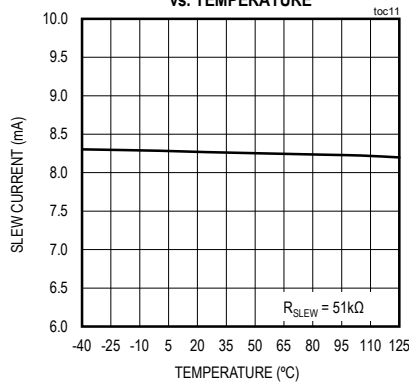
DEAD TIME vs. TEMPERATURE



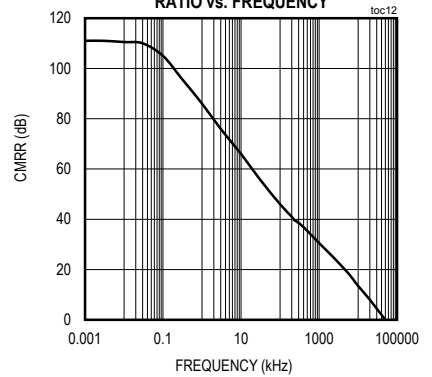
SLEW CURRENT vs. R_SLEW



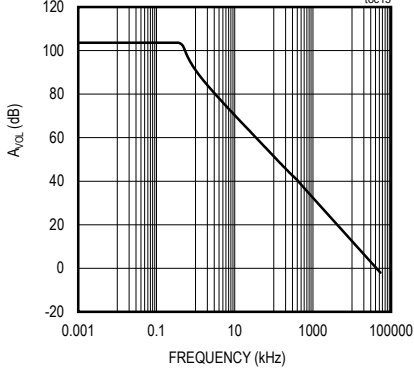
DRIVER SLEW CURRENT (SINKING OR SOURCING) vs. TEMPERATURE



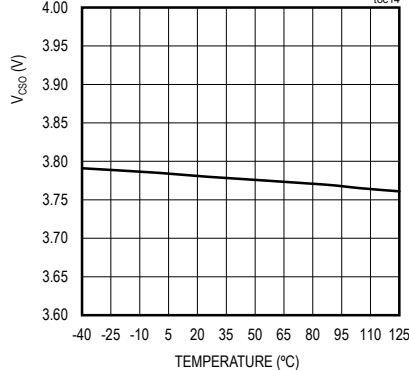
CSA COMMON-MODE REJECTION RATIO vs. FREQUENCY



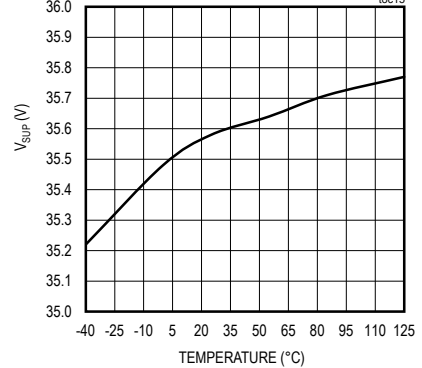
CSA OPEN-LOOP GAIN vs. FREQUENCY



OVERCURRENT THRESHOLD vs. TEMPERATURE



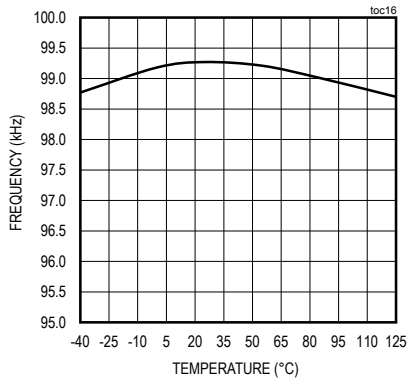
SUP_ OVERVOLTAGE THRESHOLD vs. TEMPERATURE



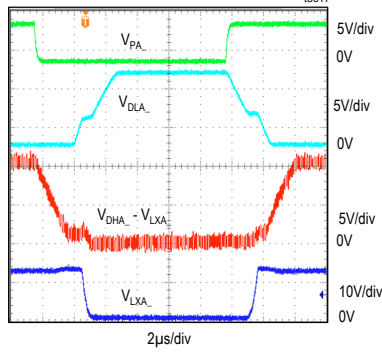
Typical Operating Characteristics (continued)

($V_{IN_}$ = 5V, $V_{SUP_}$ = 14V, $V_{EN_}$ = $V_{DIAG_}$ = 3.3V, unless otherwise noted.)

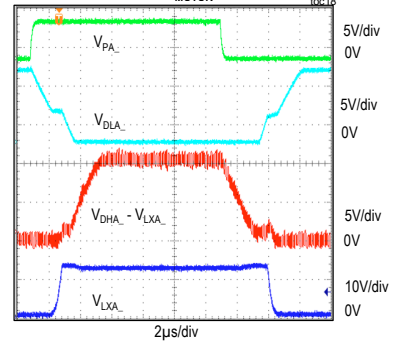
CHARGE-PUMP FREQUENCY vs. TEMPERATURE



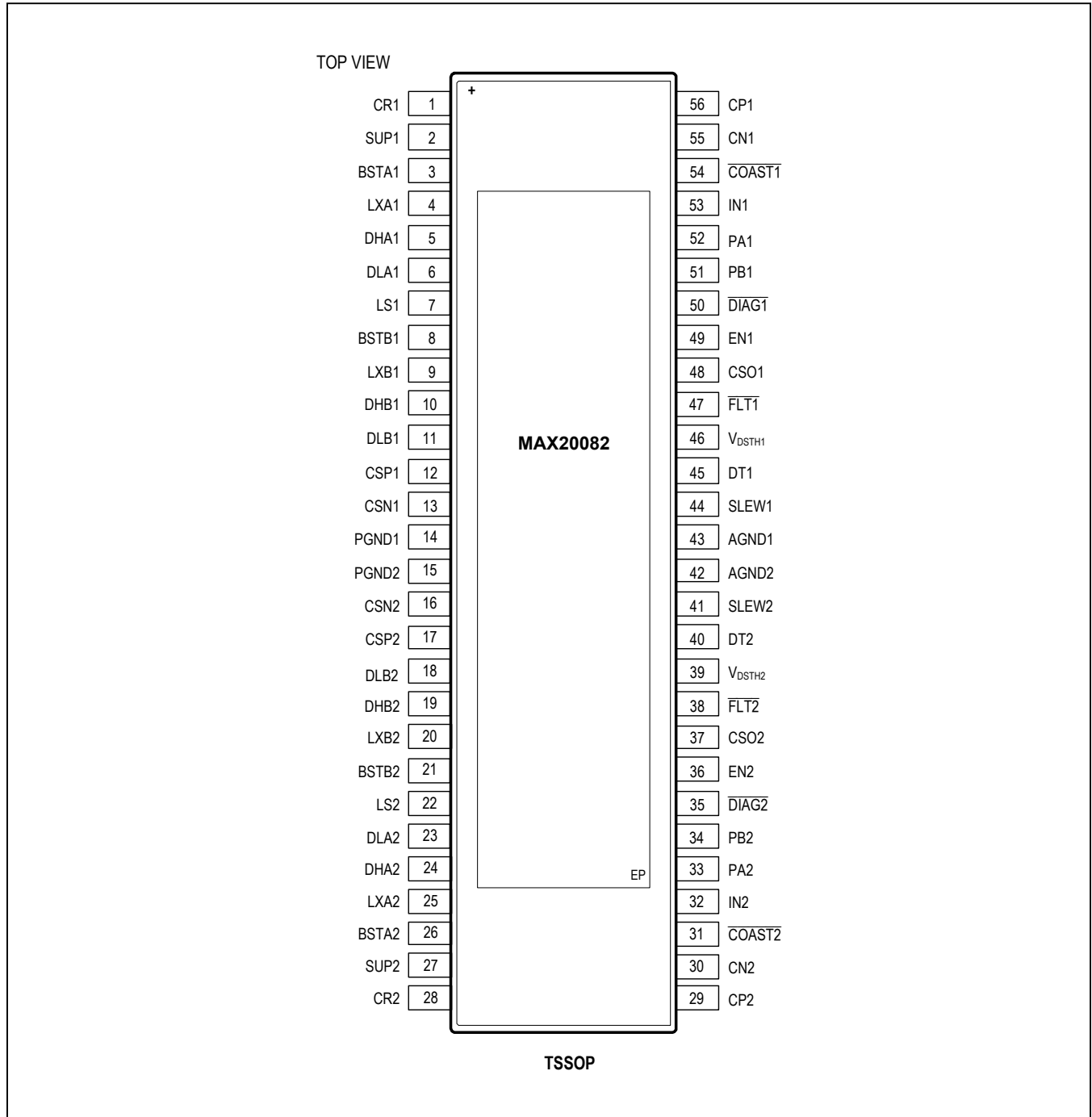
DRIVER TRANSIENT RESPONSE TO PA_TOGGLING (I_{MOTOR} = 3.5A SOURCE)



DRIVER TRANSIENT RESPONSE TO PA_TOGGLING (I_{MOTOR} = 3.5A SINK)



Pin Configuration



Pin Description

| PIN | NAME | FUNCTION |
|-----|--------|--|
| 1 | CR1 | Nominal 10V Supply Voltage for the Gate Drivers |
| 2 | SUP1 | High-Side Common Drain Connection and Sense |
| 3 | BSTA1 | Bootstrap Capacitor Connection for High-Side Drive A |
| 4 | LXA1 | Motor Connection A |
| 5 | DHA1 | High-Side Gate Drive A |
| 6 | DLA1 | Low-Side Gate Drive A |
| 7 | LS1 | Low-Side Common Source Connection |
| 8 | BSTB1 | Bootstrap Capacitor Connection for High-Side Drive B |
| 9 | LXB1 | Motor Connection B |
| 10 | DHB1 | High-Side Gate Drive B |
| 11 | DLB1 | Low-side Gate Drive B |
| 12 | CSP1 | Positive Input Current Sense |
| 13 | CSN1 | Negative Input Current Sense |
| 14 | PGND1 | Power Ground |
| 15 | PGND2 | Power Ground |
| 16 | CSN2 | Negative Input Current Sense |
| 17 | CSP2 | Positive Input Current Sense |
| 18 | DLB2 | Low-Side Gate Drive B |
| 19 | DHB2 | High-Side Gate Drive B |
| 20 | LXB2 | Motor Connection B |
| 21 | BSTB2 | Bootstrap Capacitor Connection for High-Side Drive B |
| 22 | LS2 | Low-Side Common Source Connection |
| 23 | DLA2 | Low-Side Gate Drive A |
| 24 | DHA2 | High-Side Gate Drive A |
| 25 | LXA2 | Motor Connection A |
| 26 | BSTA2 | Bootstrap Capacitor Connection for High-Side Drive A |
| 27 | SUP2 | High-Side Common Drain Connection and Sense |
| 28 | CR2 | Nominal 10V Supply Voltage for the Gate Drivers |
| 29 | CP2 | Charge-Pump Doubler Capacitor Connection P |
| 30 | CN2 | Charge-Pump Doubler Capacitor Connection N |
| 31 | COAST2 | Active-Low H-Bridge Disable Input |
| 32 | IN2 | 5V Input Supply |
| 33 | PA2 | Logic Control Input A |
| 34 | PB2 | Logic Control Input B |
| 35 | DIAG2 | Diagnostic Input |

Pin Description (continued)

| PIN | NAME | FUNCTION |
|-----|----------------------------|---|
| 36 | EN2 | Enable Input |
| 37 | CSO2 | Input Current-Sense Amplifier Output |
| 38 | $\overline{\text{FLT}}2$ | Fault Flag Open-Drain Output |
| 39 | V _{DSTH2} | Drain-to-Source Fault-Threshold Level Input |
| 40 | DT2 | Dead-Time Resistor Connection |
| 41 | SLEW2 | Slew-Time Resistor Connection |
| 42 | AGND2 | Analog Ground |
| 43 | AGND1 | Analog Ground |
| 44 | SLEW1 | Slew-Time Resistor Connection |
| 45 | DT1 | Dead-Time Resistor Connection |
| 46 | V _{DSTH1} | Drain-to-Source Fault-Threshold Level Input |
| 47 | $\overline{\text{FLT}}1$ | Fault Flag Open-Drain Output |
| 48 | CSO1 | Input Current-Sense Amplifier Output |
| 49 | EN1 | Enable Input |
| 50 | $\overline{\text{DIAG}}1$ | Diagnostic Input |
| 51 | PB1 | Logic Control Input B |
| 52 | PA1 | Logic Control Input A |
| 53 | IN1 | 5V Input Supply |
| 54 | $\overline{\text{COAST}}1$ | Active-Low H-Bridge Disable Input |
| 55 | CN1 | Charge-Pump Capacitor Connection N |
| 56 | CP1 | Charge-Pump Capacitor Connection P |

Detailed Description

The MAX20082 is a dual, full-bridge controller specifically designed for use in fault-tolerant automotive applications, with high-power inductive loads such as brushed DC motors. The device has two fully independent motor-control channels designed for use with external n-channel power MOSFETs. Each channel operates from a 4.75V to 5.25V input supply voltage range, and is capable of working with motor supply voltages up to 35V.

A charge-pump regulator provides 9.8V gate drive with a 5V input supply voltage. A bootstrap capacitor is used to provide the voltage above the input battery voltage necessary to drive the high-side n-channel MOSFETs in the H-bridge. An internal top-off charge pump for the high-side drive allows DC (100% duty cycle) operation.

The device also includes programmable dead time, gate-drive slew rate, and MOSFET short-circuit threshold. The H-bridge can be driven in forward mode (clockwise), reverse mode (counterclockwise), braking mode, and coast mode. In braking mode, both the low-side MOSFETs are turned on (synchronous slow decay). In coast mode, all the MOSFETs in the H-bridge are off (asynchronous fast decay). The power MOSFETs are protected from shoot-through by a resistor-adjustable dead time.

Each channel also integrates a low-side current-sense amplifier. Used for sensing-motor (H-bridge) current, the current-sense amplifier includes an overcurrent-protection circuit to limit the current in the event of motor faults.

Integrated diagnostics provide indication of undervoltage, overtemperature, H-bridge, and pin faults and can be configured to protect the power MOSFETs under most short-circuit conditions. In addition, the device supports implementation in ASIL systems by having two completely redundant H-bridge drivers in one package. The two channels are completely independent and fully redundant, with no shared pins or functions.

The device is specified for operation over the full -40°C to $+125^{\circ}\text{C}$ ambient temperature range. The maximum junction temperature is $+150^{\circ}\text{C}$, with thermal shutdown at $+170^{\circ}\text{C}$ (typ). The device is available in a 56-pin 14mm x 6.1mm TSSOP package.

Input Supply

Individual 5V power-supply connections, isolated with fuses, should be provided to the device in order to guarantee fault isolation. Decouple each supply with a 2.2 μF ceramic capacitor connected close to the IN_ pins and ground pins. An RC filter, consisting of a 1 Ω resistor in series with a 2.2 μF connected to AGND, is needed to prevent supply line transients from triggering undesired UVLO faults. The device operates within specified parameters with an input supply from 4.75 to 5.25 V.

Input Supply Undervoltage

The device includes undervoltage-lockout circuitry (UVLO) on the IN_ pins. Input supply voltages of less than 4.25V inhibit operation of the device by turning off the driver outputs (motor in coast) and CR_ charge pump.

Charge Pump

A charge-pump doubler provides the voltage required to drive the switching MOSFETs in the H-bridge. The charge-pump boost converter doubles the input supply voltage (IN_) through a pump capacitor connected between the CP_ and CN_ pins. This capacitor should typically be a 330nF ceramic type. The switching frequency of the charge pump is set at 100kHz.

The regulated voltage is available on the CR_ pin. Connect a 3.3 μF ceramic capacitor between CR_ and AGND_ to provide the transient charging current to the low-side drivers and the bootstrap capacitors. The charge pump features undervoltage-lockout circuitry that turns off the driver outputs (motor in coast) and CR charge pump when the CR_ voltage is lower than 7V (typ). See [Figure 1](#).

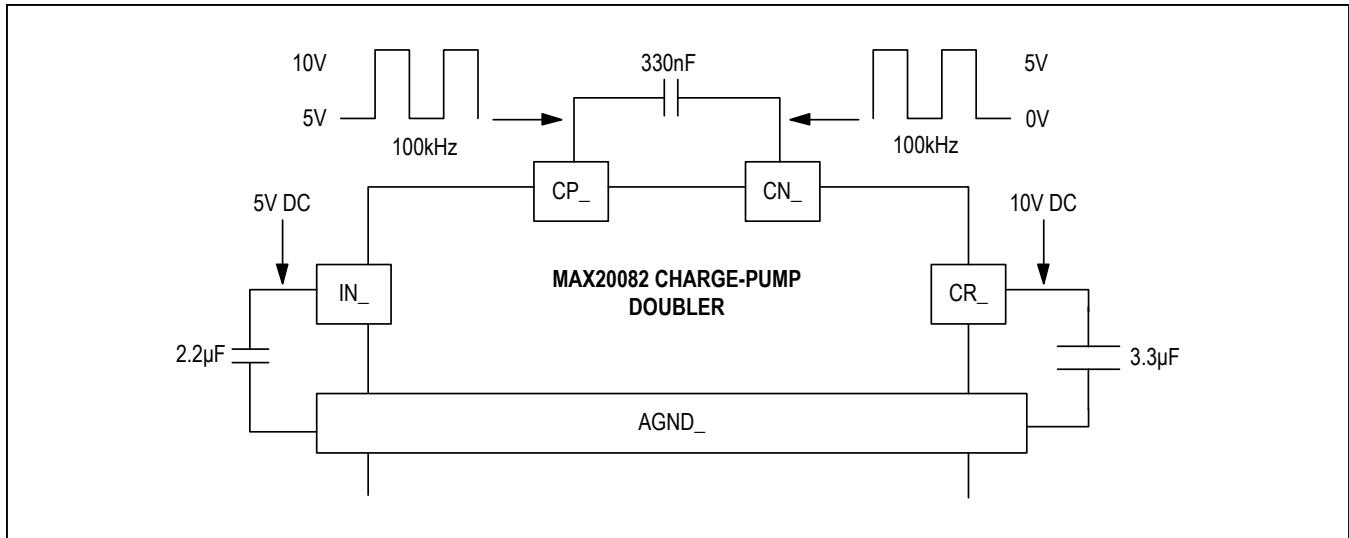


Figure 1. Charge-Pump Doubler

Top-Off Charge Pump

A top-off charge pump maintains the gate voltage on the external FETs during 100% duty-cycle operation. It is a low-current trickle pump and operates only when the corresponding high-side FET has been on for at least 0.6ms (typ). Without the top-off charge pump, this current would be drawn from the bootstrap capacitor causing it to discharge. The charge pump provides sufficient current to ensure that the bootstrap voltage is maintained close to twice the IN_ voltage. The dynamic charge required to turn on the external FETs is provided by the bootstrap capacitor. The top-off charge pump only provides the charge required to compensate for any leakage current that occurs on the high-side once the FET is on.

Low-Side Gate Drivers

The gate drivers are controlled by the logic inputs (PA_ and PB_). The low-side drivers are powered by the charge-pump output voltage on CR_. DLA_ controls the low-side FET whose drain is connected to LXA_ and

DLB_ controls the low-side FET whose drain is connected to LXB_. DLA_ goes low to turn off the low-side FET whose drain is connected to LXA_ and DLB_ goes low to turn off the low-side FET whose drain is connected to LXB_.

The rise and fall times can be controlled by a resistor on the SLEW_ pin and are designed to be symmetrical. Additional increase in the slew times can be achieved by adding external resistors in series with the connection to the external FET gate. The dead time is controlled by a resistor on the DT_ pin and is also symmetrical.

Low-Side MOSFET Drain Connection

The LXA_ and LXB_ pins are directly connected to the motor. These pins should be connected to the negative side of the bootstrap capacitors and are the negative rail connection for the high-side drivers. The discharge current from the high-side gate capacitance flows through these connections so a low-impedance connection is needed to the MOSFET bridge.

High-Side Gate Drivers

The high-side gate drive outputs (DHA_ and DHB_) are used to drive the high-side FETs in the H-bridge. Connect the external FET gates as close as possible to the DHA_ and DHB_ pins.

Both the rise/fall times can be controlled by the resistor on the SLEW_ pin. Additional gate-drive resistors can be added to increase the slew times beyond what is programmed on the SLEW_ pin. The dead time is controlled by the resistor on the DT_ pin and is symmetrical.

Bootstrap Capacitor Connections

These are the high-side connections for the bootstrap capacitors and are the positive supply for the high-side gate drives. The bootstrap capacitors are charged to approximately the CR_ voltage when the associated output LXA_ or LXB_ terminal is low.

When the LXA_ or LXB_ output swings high, the charge on the bootstrap capacitor causes the voltage at the corresponding BSTA_ or BSTB_ terminal to rise with the output to provide the boosted gate voltage needed to drive the high-side MOSFETs.

Undervoltage circuitry monitors the voltage on the bootstrap capacitors and turns on the H-bridge low-side FETs (see the faults description) if this voltage is lower than 60% of the CR_ voltage. A typical bootstrap capacitor value of 330nF is advised.

Dead-Time Programming

Dead time is defined as the time between the high/low side starting to turn off and the complementary side starting to turn on. Dead time is required to prevent shoot-through in the MOSFET bridge when the high- or low-side FET is turned off and the complementary low- or high-side FET is turned on. Set the dead time for all the phases in one channel by a single resistor on the DT_ pin.

The voltage on the DT_ pin is regulated to 1V \pm 3% when a resistor greater than 10k Ω is connected from this pin to AGND_. The dead time is programmed by the current

through the DT_ resistor, within a range between 370ns to 5 μ s. The current flowing into the resistor on the DT_ pin is given by:

$$I_{DT_} = 1/R_{DT_}$$

where R_{DT_} is the resistor on the DT_ pin. For R_{DT_} values between 10k Ω and 200k Ω at 25°C, the nominal value of the dead time (t_{DEAD}) is given by:

$$t_{DEAD}(R_{DT_}) = 25 \times R_{DT_} (k) + 100ns$$

Slew-Time Programming

The gate pullup or pulldown current for all the FETs is programmed by a resistor on the SLEW_ pin. This results in controlled LX_ rise and fall times, which are symmetrical and equivalent for all the FETs in the H-bridge. The voltage on the slew pin is regulated to 1V \pm 3% when a resistor greater than 10k Ω is connected from this pin to AGND_.

The slew current is programmed within the 40mA and 2mA range. The current flowing into the resistor on the SLEW_ pin is given by:

$$I_{SLEW_} = 1/R_{SLEW_}$$

where R_{SLEW_} is the resistor on the SLEW_ pin. For R_{SLEW_} values between 10k Ω and 200k Ω at 25°C, the nominal value of the slew current (I_{SLEW_}) is given by:

$$I_{SLEW_}(R_{SLEW_}) = 400/R_{SLEW_} (k) \text{ mA}$$

Slew time can be determined with the following formula, where Q_{GD} is the gate drain charge of the external nMOS:

$$t_{SLEW_} = Q_{GD} (nF) / I_{SLEW_} (mA)$$

Enable

When EN_ is low, the device is in shutdown mode and the maximum current drawn by each half of the device is less than 10 μ A. To enter shutdown, hold EN_ low for at least 1.2ms.

Phase Control

The $\overline{\text{COAST}}$, PA_, and PB_ logic inputs allow motor control through a single-bit PWM digital signal. Depending on the logic configuration of the PA_ and PB_ inputs, the μC can select the direction of the motor and the current-decay mode during the off time (see [Figure 2](#), [Figure 3](#), and [Table 1](#)).

PA_ (PB_) 0 \rightarrow 1 and $\overline{\text{COAST}}$ = 1:

- 1) Q2 (Q4) is turned off and dead-time delay starts.
- 2) When dead-time delay elapses, Q1 (Q3) is turned on.

PA_ (PB_) 1 \rightarrow 0 and $\overline{\text{COAST}}$ = 1:

- 1) Q1 (Q3) is turned off and dead-time delay starts.
- 2) When dead-time delay elapses, Q2 (Q4) is turned on.

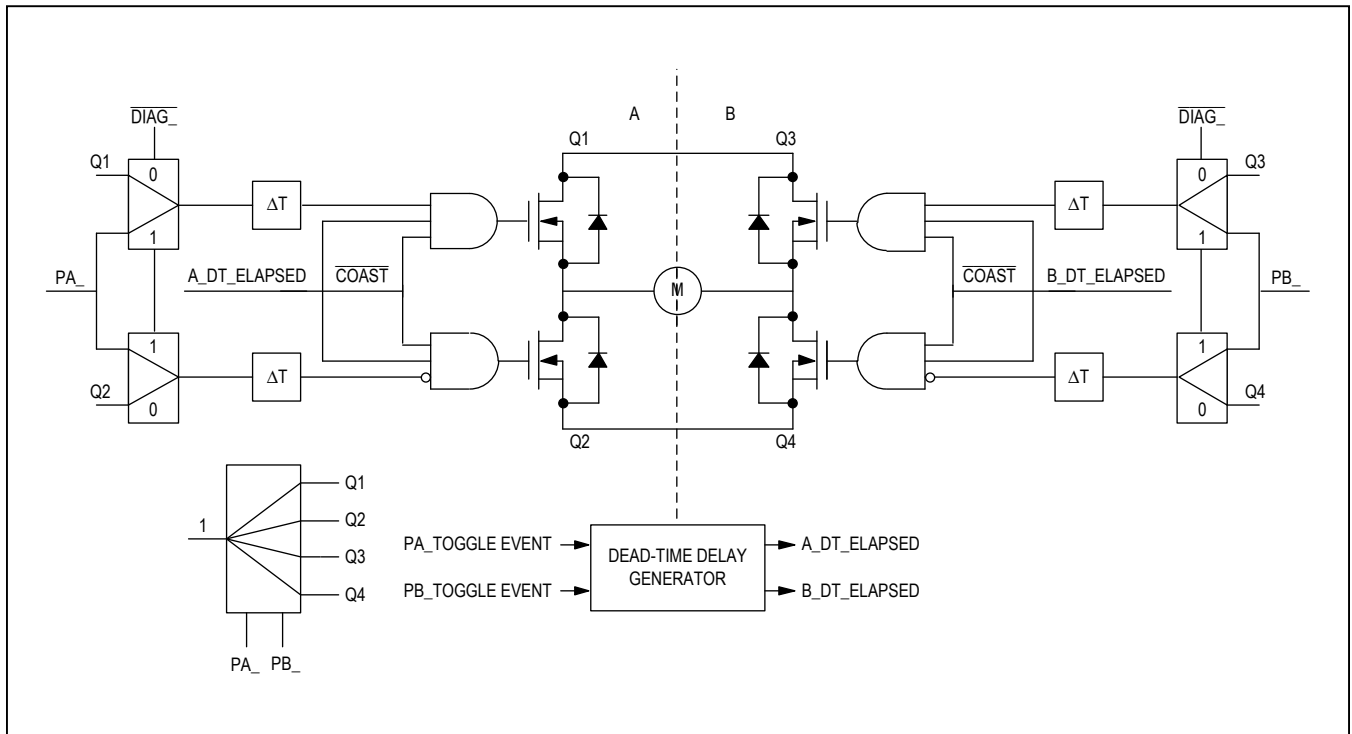


Figure 2. H-Bridge Logic (Normal/Diagnostic Mode)

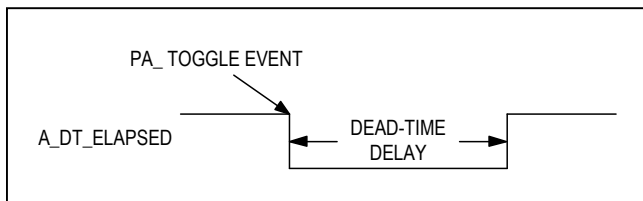


Figure 3. A_DT_Elapsed Signal Used in Dead-Time Generation

Table 1. Phase Control

| PA_ (PB_) | $\overline{\text{COAST}}$ | Q1 (Q3) | Q2 (Q4) |
|-----------|---------------------------|---------|---------|
| 1 | 1 | On | Off |
| 0 | 1 | Off | On |
| X | 0 | Off | Off |

Table 2. H-Bridge Application

| PA_ | PB_ | COAST_ | ON TIME | OFF TIME |
|-------------------------|-------------------------|--------|------------------------|-------------------------|
| PWM | 0 | 1 | Forward (Q1 and Q4 on) | LS brake (Q2 and Q4 on) |
| 1 | $\overline{\text{PWM}}$ | 1 | Forward (Q1 and Q4 on) | HS brake (Q1 and Q3 on) |
| PWM | $\overline{\text{PWM}}$ | 1 | Forward (Q1 and Q4 on) | Reverse (Q2 and Q3 on) |
| 0 | PWM | 1 | Reverse (Q2 and Q3 on) | LS brake (Q2 and Q4 on) |
| $\overline{\text{PWM}}$ | 1 | 1 | Reverse (Q2 and Q3 on) | HS brake (Q1 and Q3 on) |
| $\overline{\text{PWM}}$ | PWM | 1 | Reverse (Q2 and Q3 on) | Forward (Q1 and Q4 on) |

Table 3. Truth Table for External MOSFET Control

| PA_ | PB_ | COAST_ | DIAG_ | Q1 | Q2 | Q3 | Q4 | H-BRIDGE STATE |
|-----|-----|--------|-------|-----|-----|-----|-----|--------------------------|
| 0 | 0 | 1 | 1 | Off | On | Off | On | Low sides on (LS brake) |
| 0 | 1 | 1 | 1 | Off | On | On | Off | Reverse |
| 1 | 0 | 1 | 1 | On | Off | Off | On | Forward |
| 1 | 1 | 1 | 1 | On | Off | On | Off | High sides on (HS brake) |
| X | X | 0 | X | Off | Off | Off | Off | Coast |
| 0 | 0 | 1 | 0 | On | Off | Off | Off | FETs diagnostic (Q1 on) |
| 0 | 1 | 1 | 0 | Off | Off | Off | On | FETs diagnostic (Q4 on) |
| 1 | 1 | 1 | 0 | Off | On | Off | Off | FETs diagnostic (Q2 on) |
| 1 | 0 | 1 | 0 | Off | Off | On | Off | FETs diagnostic (Q3 on) |

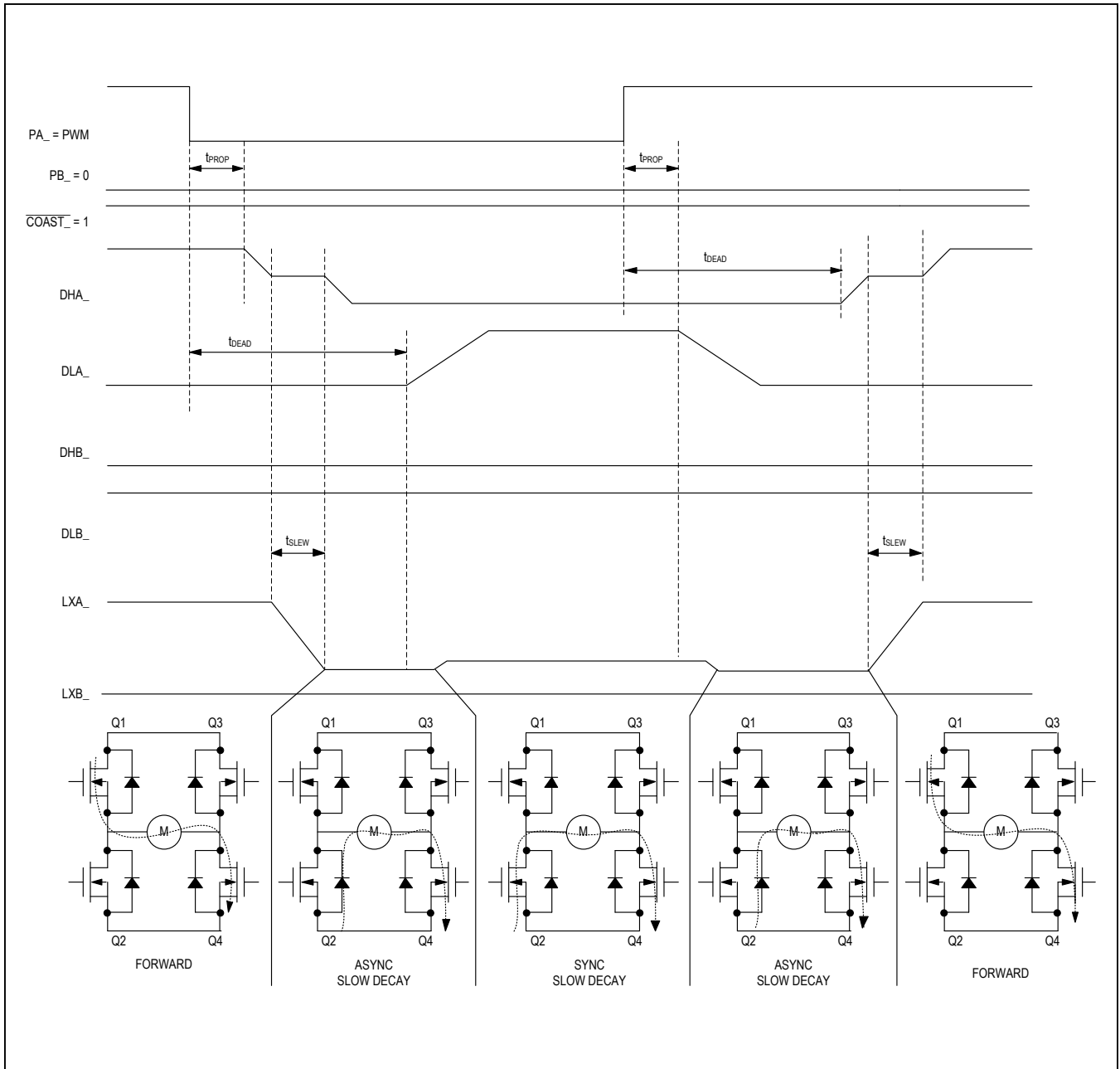


Figure 4. On Time/Forward; Off Time/Brake (Sync Slow Decay)

Current-Sense Amplifier and Overcurrent Detection

The H-bridge current is sensed by the low-side current-sense amplifier. The open-loop gain of the current-sense amplifier is 110dB and the closed-loop gain of this amplifier is set with external resistors (CSA_G) according to:

$$CSA_G = R2/R1 + 1 \text{ with } R3/R4 = R2$$

With additional external resistors, it is possible to add a bias voltage to the CSO_ output to enable negative current monitoring during fast decay:

$$BIAS = V_{REF} \times [R3 / (R3 + R4)]$$

The values of R1–R4 must be chosen in accordance with [Table 4](#) in order to pass the power-up diagnostic test.

An overcurrent fault is triggered when the output of the current-sense amplifier (CSO_) reaches 3.8V. The motor overcurrent value can be estimated with the following formula:

$$I_{MOTOR_OC} = (3.8V - BIAS) / (R_{SENSE} \times CSA_G)$$

The application circuit for a slow-decay case (I_MOTOR always positive) is shown in [Figure 7](#).

$$CSA_G = 38, BIAS = 0V, \text{ CSA Closed-Loop Bandwidth} = 790kHz$$

The application circuit for a fast-decay case (I_MOTOR is positive and negative) is shown in [Figure 8](#).

$$CSA_G = 19, BIAS = 1.9V, \text{ CSA Closed-Loop Bandwidth} = 1.6MHz$$

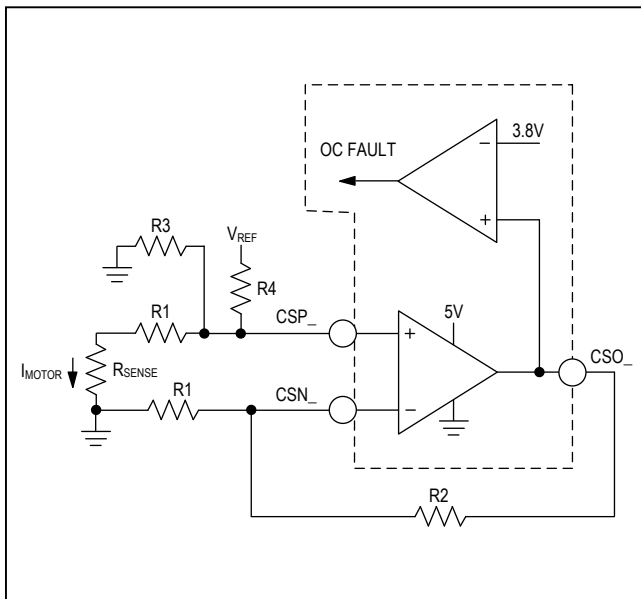


Figure 5. Current-Sense Amplifier (Typical Configuration)

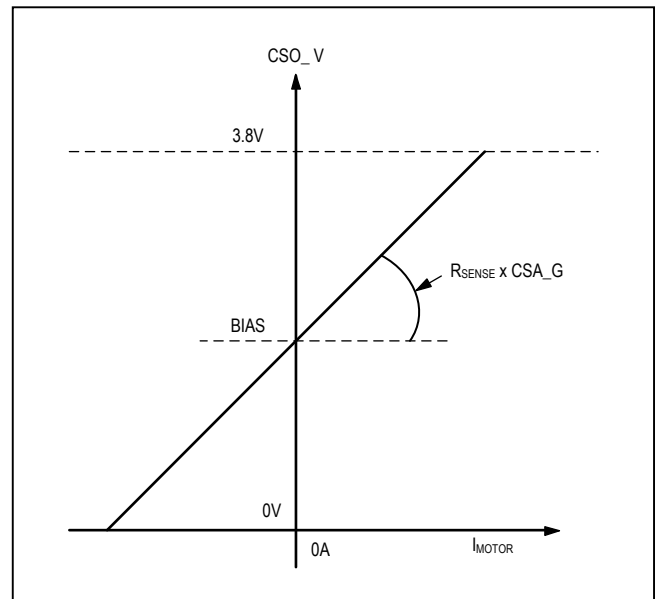


Figure 6. Current-Sense Amplifier Output Characteristics

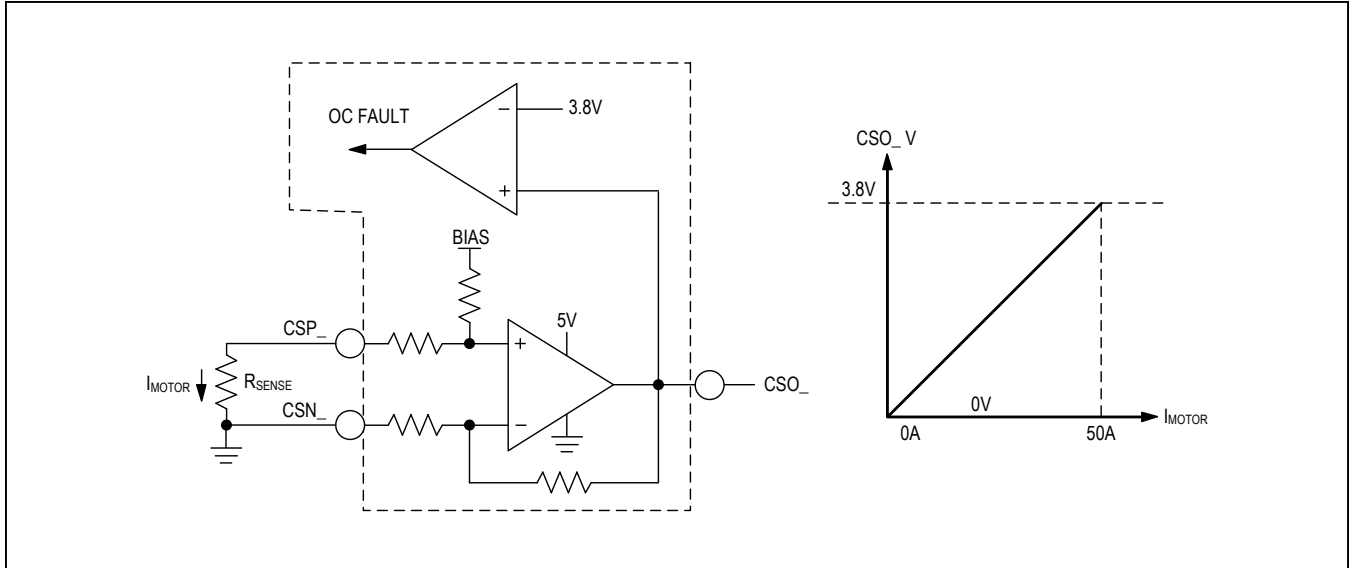


Figure 7. Current-Sense Amplifier Configuration (Positive Current Only)

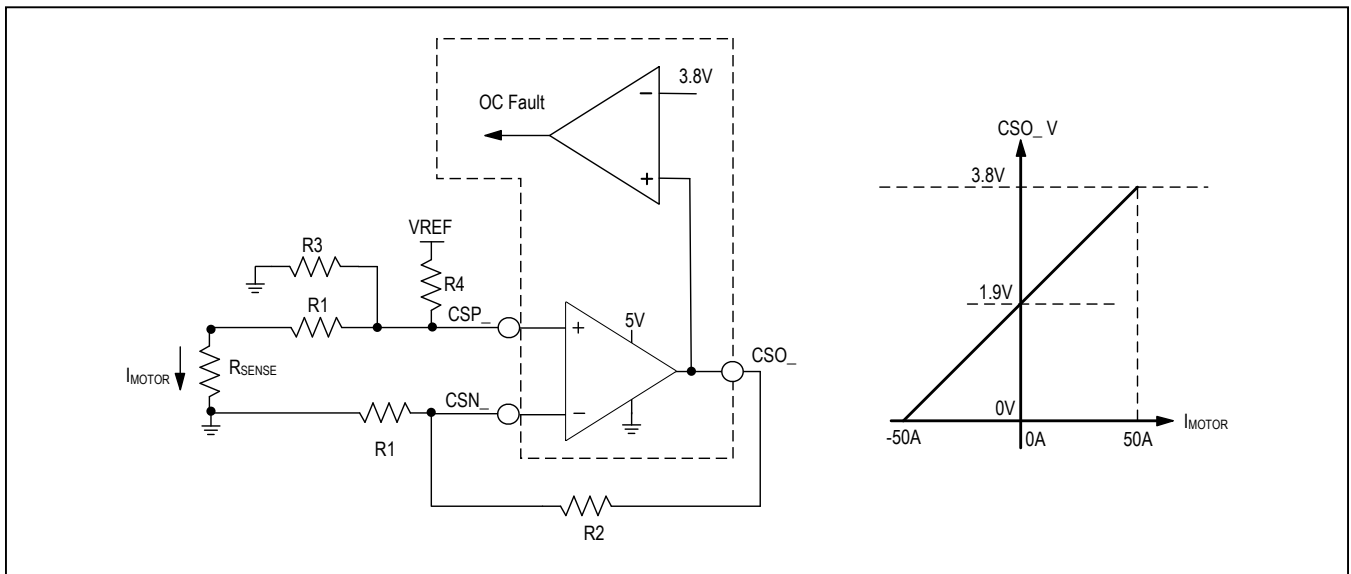


Figure 8. Current-Sense Amplifier Configuration (Bidirectional Current Flow)

Power-Up Diagnostic Mode

After power-up, every time EN₊ goes high with $\overline{\text{DIAG}}$ low, the diagnostic power-up routine starts. The device performs the following checks for each pin:

- Is the pin shorted to ground?
- Is the pin open?
- Is the pin shorted to an adjacent pin?

The diagnostic strategy is based on a sequential routine that starts from the $\overline{\text{VDSTH}}$ pin and proceeds counter-clockwise to end at the $\overline{\text{COAST}}$ pin. In the event of a diagnostic error during the sequential check, the diagnostic sequence is terminated and an ASIL fault is declared at the $\overline{\text{FLT}}$ pin by forcing the duty of the output signal to 25%.

Pins LX₊, DH₊, DL₊, BST₊, SUP₊, and LS₊ are not checked during this power-up diagnostic routine. Their functionality can be verified during the FET diagnostic mode, as described in the *FET Diagnostic Mode* section.

FET Diagnostic Mode

During normal operation (after power-up is completed, EN₊ pin high), FET diagnostic mode can be entered by forcing $\overline{\text{DIAG}} = 0$. The LX_{A+} and LX_{B+} pins are then connected through an internal 1k Ω (typ) pulldown/pullup to PGND₊/SUP₊, based on the selected FET under diagnosis.

V_{DS} fault and overcurrent event can be used to check the motor and H-bridge status in FET diagnostic mode.

Table 4. Power-Up Diagnostic Pin Setting

| PIN | CONDITION TO PASS POWER-UP TEST |
|---------------------------|--|
| CR ₊ | 3.3 μF $\pm 10\%$ ceramic capacitor connected to ground. |
| CSP ₊ | Place an equivalent resistance with a value between 500 Ω and 2k Ω . |
| CSN ₊ | Place an equivalent resistance with a value between 500 Ω and 2k Ω . |
| CSO ₊ | Place a feedback resistance with a value between 5k Ω and 100k Ω . |
| PGND ₊ | Connect to the ground plane of the system board. |
| SLEW ₊ | Place a resistance with a value between 10k Ω and 200k Ω . |
| DT ₊ | Place a resistance with a value between 10k Ω and 200k Ω . |
| $\overline{\text{VDSTH}}$ | Place an equivalent resistance with a value between 500 Ω and 10k Ω . |
| $\overline{\text{FLT}}$ | Connect a resistance with a value between 1k Ω and 3.3k Ω to IN ₊ . |
| EN ₊ | Connect to IN ₊ through external driving circuitry. |
| $\overline{\text{DIAG}}$ | Connect to AGND ₊ /PGND ₊ or IN ₊ through external driving circuitry. |
| PA ₊ | Connect to AGND ₊ /PGND ₊ through external driving circuitry. |
| PB ₊ | Connect to IN ₊ through external driving circuitry. |
| $\overline{\text{COAST}}$ | Connect to AGND ₊ /PGND ₊ through external driving circuitry. |

Table 5. FET Control

| $\overline{\text{COAST}}$ | PA ₊ | PB ₊ | FET ON | LXA ₊ STATUS | LXB ₊ STATUS |
|---------------------------|-----------------|-----------------|--------|----------------------------|----------------------------|
| 1 | 0 | 0 | Q1 | Pulldown to ground | Hi-Z |
| 1 | 1 | 1 | Q2 | Pullup to SUP ₊ | Hi-Z |
| 1 | 1 | 0 | Q3 | Hi-Z | Pulldown to ground |
| 1 | 0 | 1 | Q4 | Hi-Z | Pullup to SUP ₊ |

Table 6. Interpreting Fault Information in Diagnostic Mode

| TURNED ON nMOS | V _{DS} FAULT | V _{DS} AND OVERCURRENT EVENT |
|----------------|---|---------------------------------------|
| Q1 | Q1 open or motor terminal A shorted to ground | Q2 shorted |
| Q2 | Q2 open or motor terminal A shorted to SUP_ | Q1 shorted |
| Q3 | Q3 open or motor terminal B shorted to ground | Q4 shorted |
| Q4 | Q4 open or motor terminal B shorted to SUP_ | Q3 shorted |

Power-Up Scenarios

See [Figure 9](#), [Figure 10](#), and [Figure 11](#) for power-up scenarios.

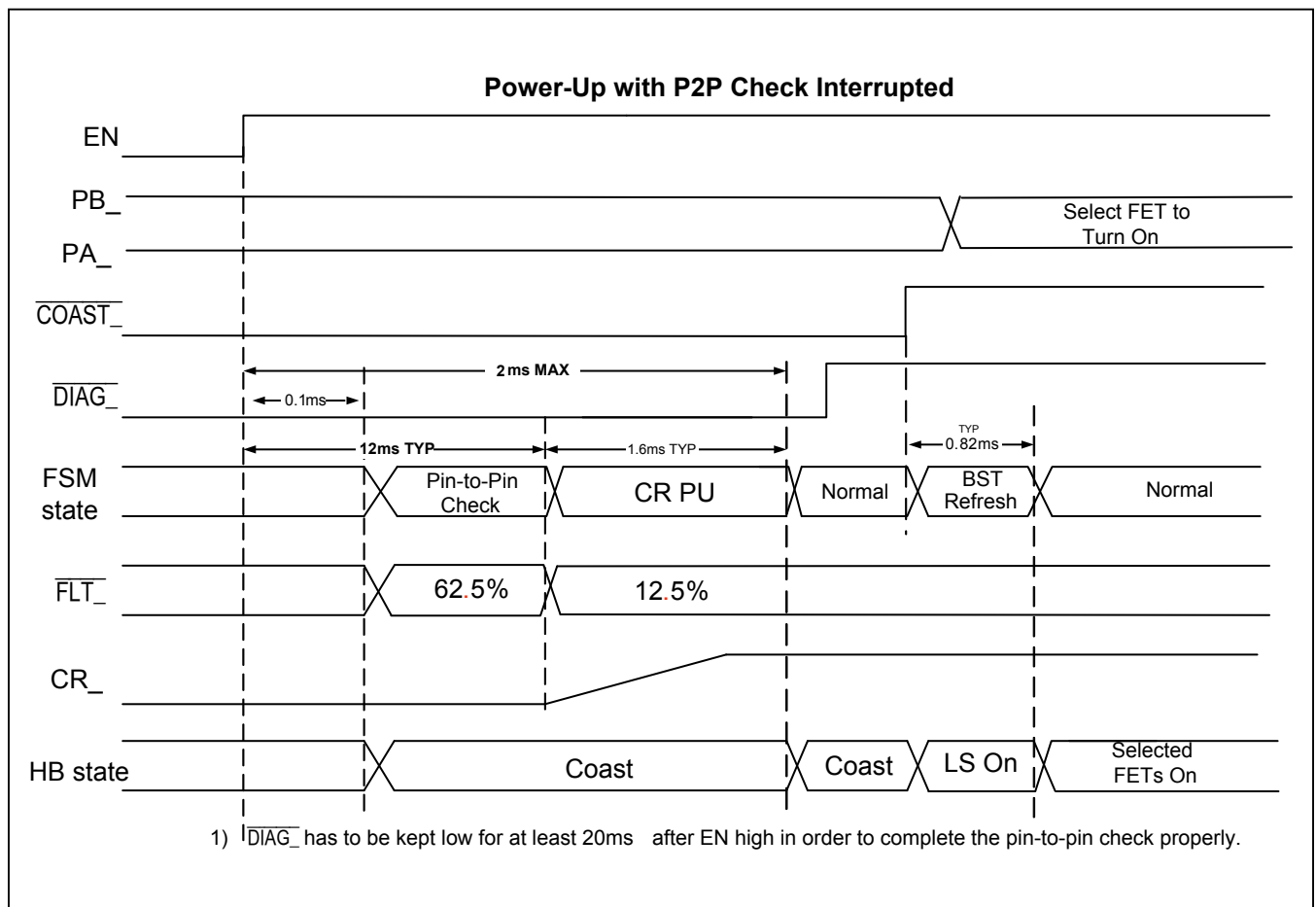


Figure 9. Power-Up Sequencing with Pin-to-Pin Check Enabled

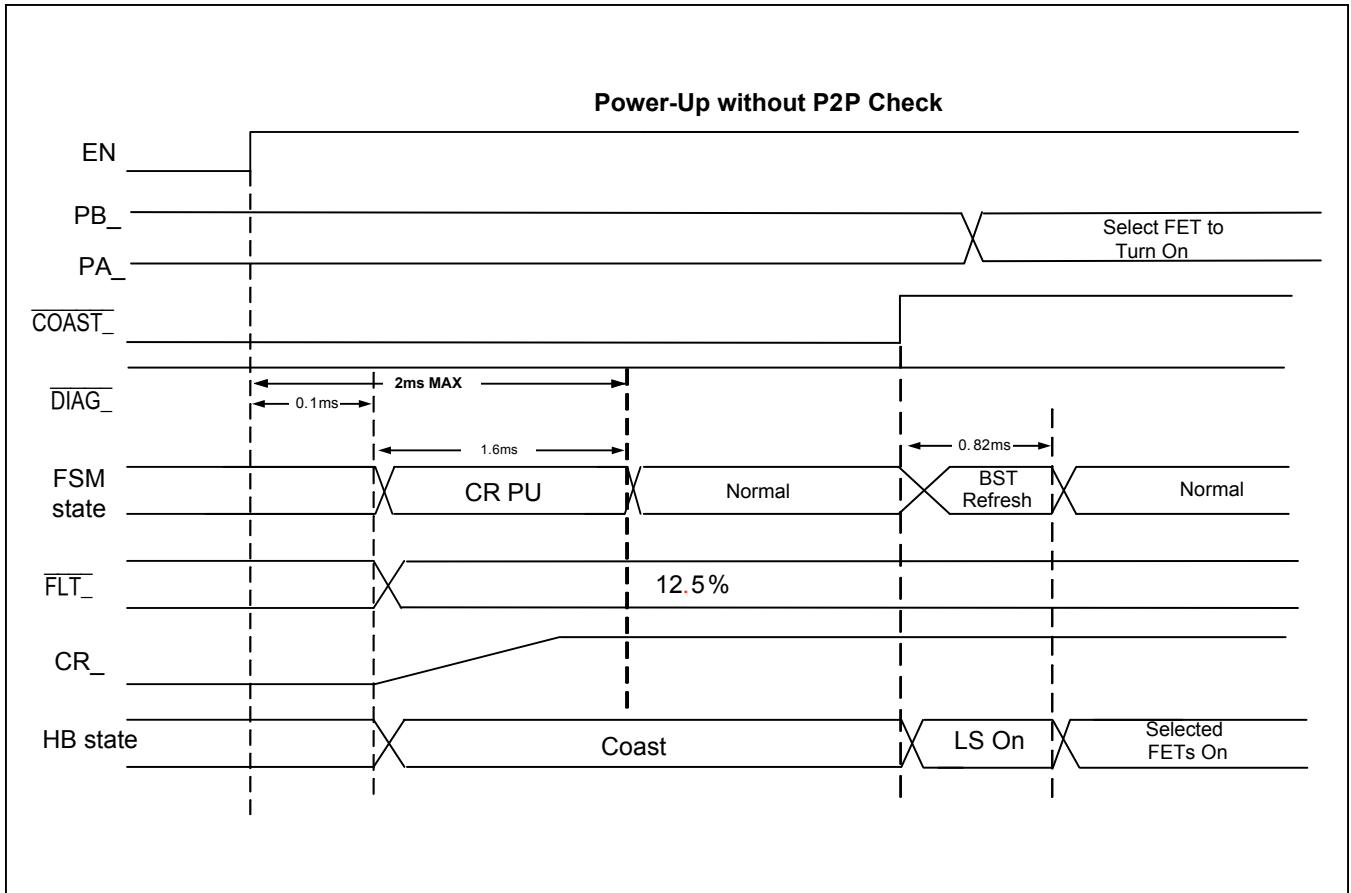


Figure 10. Power-Up Sequencing with Pin-to-Pin Check Disabled

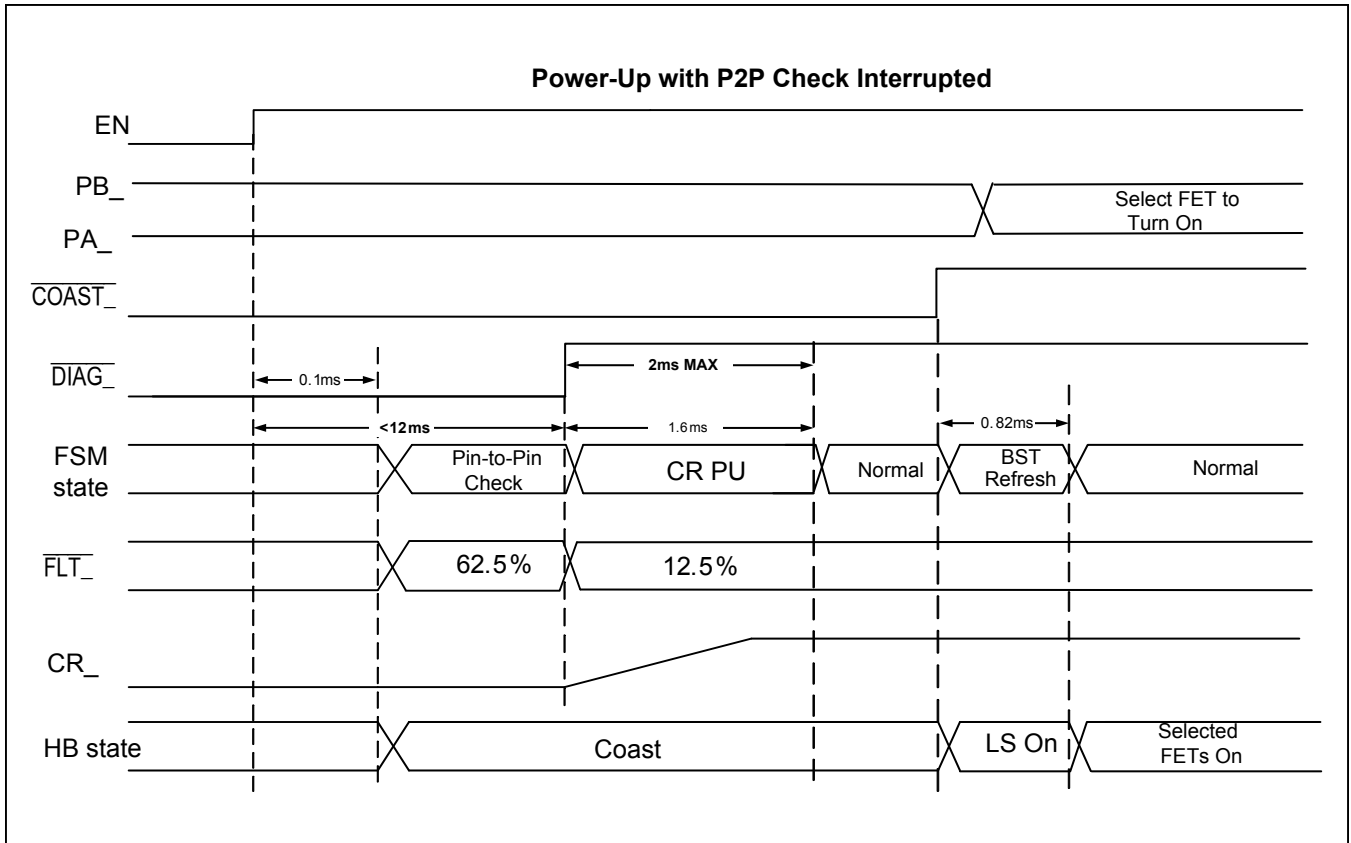


Figure 11. Power-Up Sequencing with Pin-to-Pin Check Interrupted

State Diagram

See Figure 12 for the FSM state diagram.

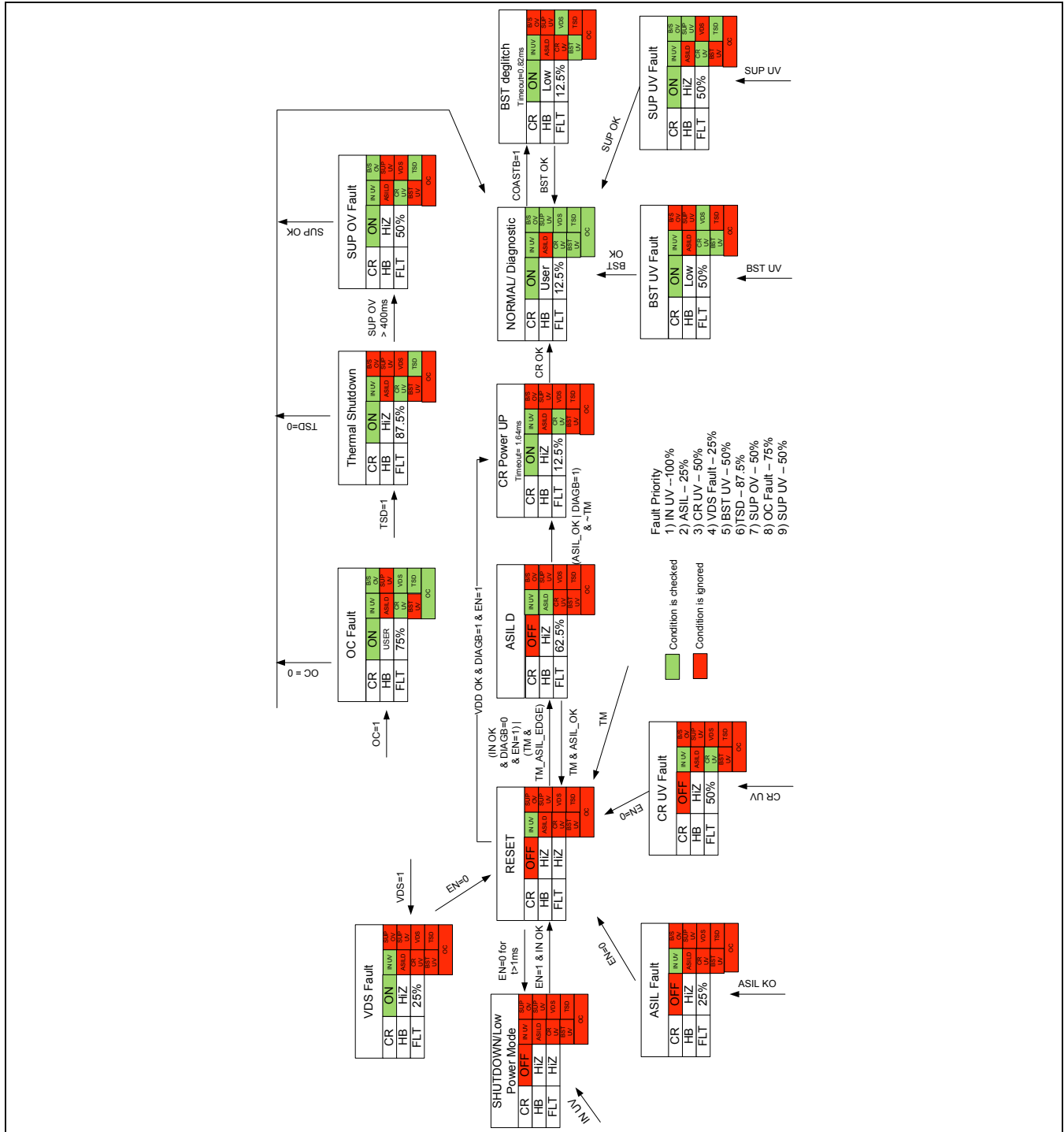


Figure 12. FSM State Diagram

BST Fault

A BST fault is detected (except in coast mode, when it is masked) when the voltage on any of the BST_ capacitors falls below 7V (typ). When this happens, normal operation of the H-bridge is impossible until the BST_ capacitor is recharged. To avoid faults due to undervoltage on the boost (BST_) capacitors, a BST fault deglitch timer is incorporated in the device. At each low-to-high transition of the $\overline{\text{COAST}}$ _ pin, the deglitch timer is activated. During the deglitch time, the internal logic of the device takes control and the DLA and DLB outputs are forced high in order to turn on the external low-side MOSFETs and refresh the charge on the boost capacitors. When this timer elapses, the bootstrap capacitors are fully charged and ready to operate the motor.

When a BST fault occurs (in the absence of faults), it is normally sufficient to perform a boost-capacitor refresh by taking $\overline{\text{COAST}}$ _ low and then high again and waiting at least 0.9ms until the BST fault deglitch timer elapses.

V_{DS} Fault

Every time an FET of the H-bridge is turned on, a dedicated drain-source comparator checks if its drain-source voltage is lower or higher than the V_{DS} voltage threshold set through the V_{DSTH}_ pin. If the FET drain-source voltage is higher than the voltage on the V_{DSTH}_ pin, a fault is detected. To avoid false error detection, the V_{DS} comparators are inhibited after MOSFET power-on for a blanking time (t_{BLANK}). Connect V_{DSTH}_ to IN_ to disable the V_{DS} fault-detection circuitry.

SUP_ Undervoltage and Overvoltage Protections

The device includes undervoltage and overvoltage detection circuitry on the SUP_ pins. If the voltage is less than 4.5V, a SUP_ undervoltage fault is signaled through the $\overline{\text{FLT}}$ _ pin and all the MOSFET drivers are turned off. If the SUP_ voltage exceeds 35V for more than 400ms, a SUP_ overvoltage fault is detected and all the drivers are turned off (H-bridge).

Fault Behavior

The $\overline{\text{FLT}}$ _ pin indicates detected faults by means of a 625kHz signal, with varying duty cycle according to [Table 7](#).

Table 7. Fault Classes and the $\overline{\text{FLT}}$ _ Output

| FAULT CLASS | FAULT DESCRIPTION | DUTY CYCLE OF $\overline{\text{FLT}}$ _ (%) |
|-------------|--|---|
| 1 | None | 12.5 |
| 2 | V _{DS} fault, ASIL fault | 25 |
| 3 | SUP_ overvoltage (SUP_, CR_ and BST_ undervoltage) | 50 |
| 1 | None (pin-to-pin check routine ongoing) | 62.5 |
| 4 | Overcurrent | 75 |
| 5 | Thermal shutdown | 87.5 |
| 6 | IN_ undervoltage | 100 |

Table 8. Fault Summary

| FAULT | FAULT DESCRIPTION | DUTY CYCLE (%) | CR_ | H-BRIDGE FETs STATE | LATCHED | FAULT RESET |
|--|--|----------------|-----|---------------------|---------|---------------|
| None | — | 12.5 | On | User control | No | — |
| Overcurrent | $V_{CSO_} > 3.8V$ | 75 | On | User control | No | — |
| V_{DS} fault ($\overline{DIAG_} = X$) | FET on-drain source voltage $> V_{DSTH_}$ | 25 | On | Off (coast*) | Yes | EN_ low pulse |
| IN_ undervoltage | $V_{IN_} < V_{INUV}$ | 100 | Off | Off (coast*) | No | — |
| CR_ undervoltage | $CR_ < V_{CRUV}$ | 50 | Off | Off (coast*) | Yes | EN_ low pulse |
| BSTA_/BSTB_ undervoltage | $BST_ - LX_ < V_{BSTUV}$ | 50 | On | DLA_, DLB_ high | No | — |
| SUP_ undervoltage | $SUP_ < V_{SUPUV}$ | 50 | On | Off (coast*) | No | — |
| SUP_ overvoltage | $SUP_ > 36V$ for $t > 400ms$ | 50 | On | Off (coast*) | No | — |
| Thermal shutdown | $T_J > T_{JTSD}$ | 87.5 | On | Off (coast*) | No | — |

*Coast = Motor in Hi-Z.

Applications Information

Power Dissipation

To evaluate the device's power consumption, it is necessary to calculate the total supply current from the supply input pin (IN_) for a single channel:

$$I_{IN_} = I_{IN_Q} + 4 \times Q_G \times f_{PWM}$$

where I_{IN_Q} is the quiescent current, Q_G is the total gate charge of the external nMOS, and f_{PWM} is the PWM switching frequency.

The device's total power dissipation is then (for both channels):

$$PD = 2 \times [V_{IN_} \times I_{IN_}]$$

Layout Guidelines

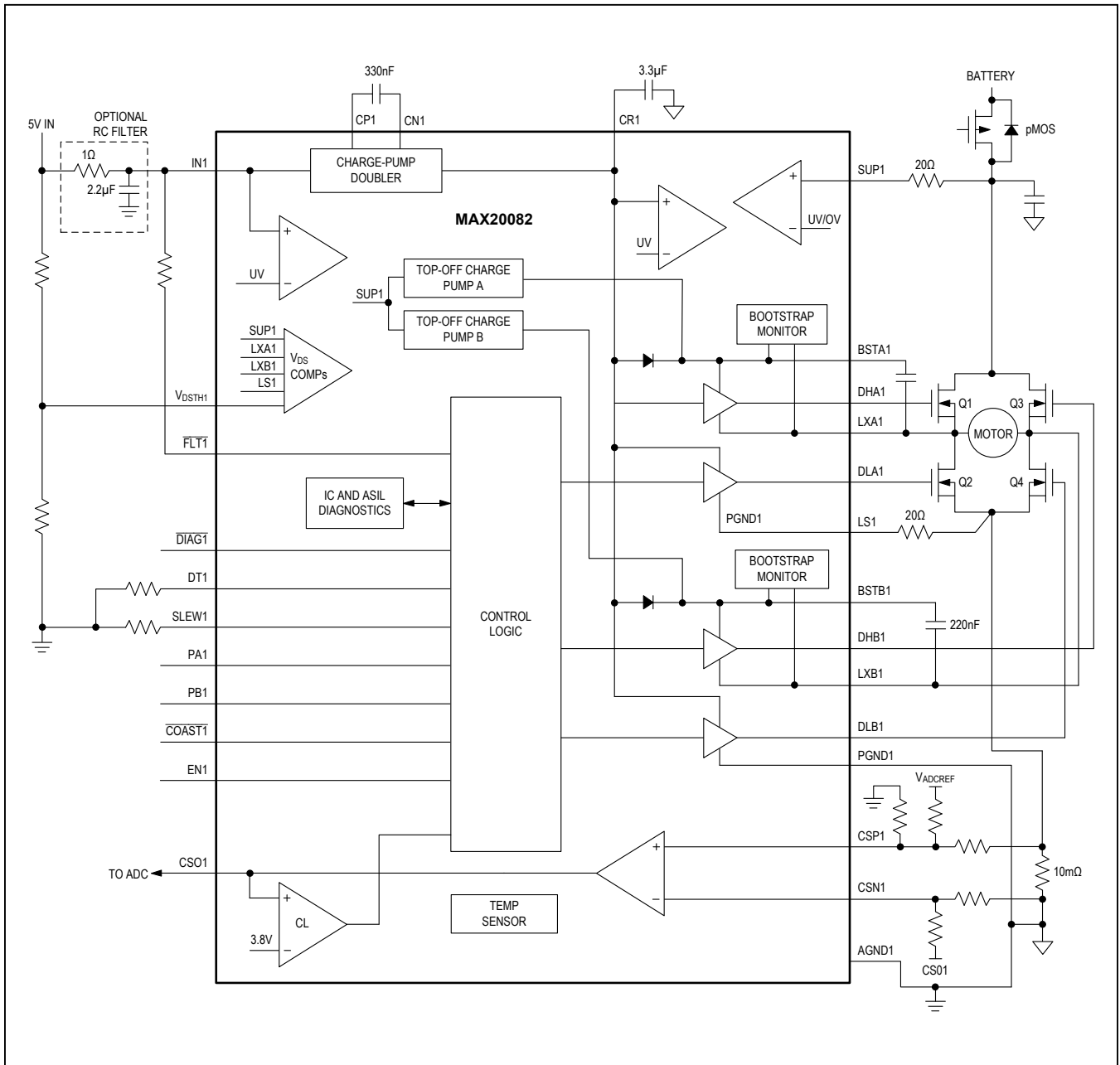
For best performance, it is advisable to use the following guidelines when designing the PCB for the MAX20082:

- Use separate analog ground (AGND) and power ground (PGND) planes and connect them at a single point. Implement connections between the same grounds on different layers with multiple vias.

- Maintain the input and output power sections (connections to SUP_, LXA_, LXB_, and LS_) as compact as possible.
- Use wide traces to connect the components related to the high-current paths.
- Use multiples vias to connect high-current paths that must pass from one layer to another.
- Make the MOSFET gate-drive traces (DHA_, DHB_, DLA_, and DLB_) as short as possible and use large track widths.
- Place the boost capacitors (between CP_ and CN_), charge-pump output capacitors (on CR_), and the input capacitors (on IN_) close to the IC and connect them without using vias.
- The current-sense connections should be Kelvin connected.

Contact your Maxim Integrated representative for further details on choosing and placing external components.

Typical Application Circuit (1 Channel Shown)



Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|-----------------|-----------------|-------------|
| MAX20082AUN/V+T | -40°C to +125°C | 56 TSSOP |

V denotes an automotive qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 56 TSSOP | U56N+2C | 21-0481 | 90-0338 |

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|-----------------|---------------|
| 0 | 8/14 | Initial release | — |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.