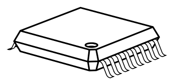
GaAs MMIC

Data Sheet

CGY 96

- Power amplifier for GSM class 4 phones
- 3.2 W (35 dBm) output power at 3.5 V
- Overall power added efficiency 50%
- Fully integrated 3 stage amplifier
- Power ramp control
- Input matched to 50 Ω, simple output match



MW-16

ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precautions!

Type	**Marking**	**Ordering Code** (taped)	**Package**
CGY 96	CGY 96	Q62702-G63	MW-16

Maximum Ratings

Parameter	**Symbol**	**Value**	**Unit**
Positive supply voltage	V_D	9	V
Supply current	I_D	4	A
Channel temperature	T_{Ch}	150	°C
Storage temperature	T_{stg}	– 55 … + 150	°C
Pulse peak power dissipation	P_{Pulse}	17	W
Total power dissipation ($T_C \leq 83$ °C) T_C: Temperature on case	P_{tot}	9.5	W

Thermal Resistance

Parameter	**Symbol**	**Value**	**Unit**
Junction-Case	R_{thJCh}	7.0	K/W

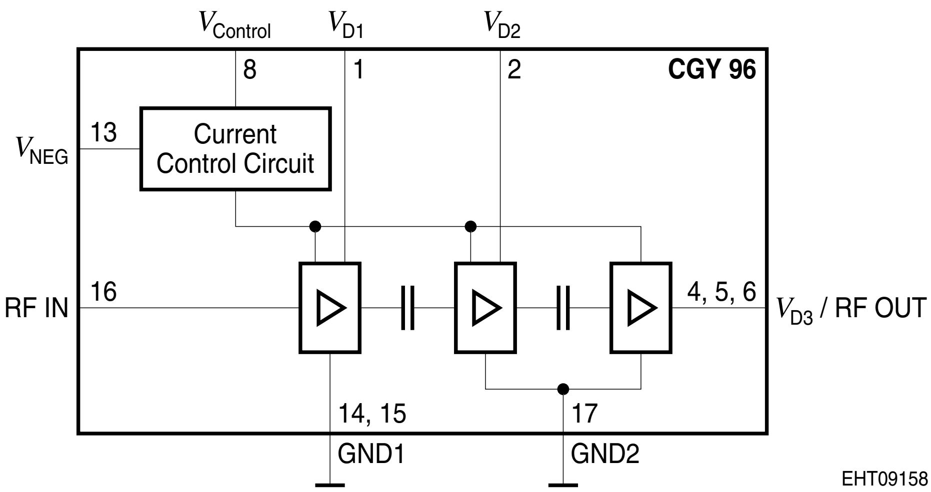


Figure 1 Functional Block Diagram

Pin Configuration

Pin No.	Name	Configuration
1	V_{D1}	Drain voltage 1st stage
2	V_{D2}	Drain voltage 2nd stage
3	N.C.	–
4, 5, 6	V_{D3}/RF OUT	Drain 3rd stage and RF-output
7	N.C.	–
8	$V_{Control}$	Control voltage for power ramping
9, 10, 11, 12	N.C.	–
13	V_{NEG}	Negative voltage for current control circuit
14, 15	GND1	Ground pin 1st stage
16	RF IN	RF Input
(17)	GND2	Ground (backside of MW-16 package)

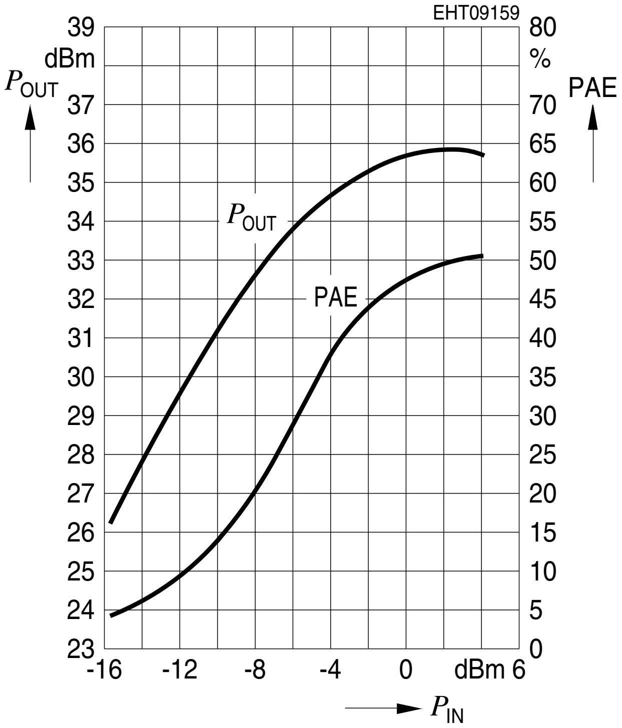
Electrical Characteristics

T_A = 25 °C, V_D = 3.5 V, V_{NEG} = – 5 V, $V_{Control}$ = 2.2 V; duty cycle 12.5%, t_{ON} = 577 µs

Parameters	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Frequency range	f	880	–	915	MHz	–
Supply current	I_D	–	1.8	2.2	A	P_{IN} = 2 dBm
Gain (small signal)	G	35	38	–	dB	–
Power gain	G_P	32.5	33	–	dB	P_{IN} = 2 dBm
Output Power	P_{OUT}	34.5	35	–	dBm	P_{IN} = 2 dBm, $V_{Control}$ = 2.0 … 2.5 V
Overall Power added Efficiency	η	44	50	–	%	P_{IN} = 2 dBm
Dynamic range output power	–	75	80	–	dB	$V_{Control}$ = 0.2 … 2.2 V
Harmonics	$H(2f_0)$ $H(3f_0)$ $H(4f_0)$	35 35 35	– 40 – 43 – 44	– – –	dBc	P_{IN} = 2 dBm
Noise Power in RX (935 - 960 MHz)	N_{RX}	–	– 81	– 70	dBm	P_{IN} = 2 dBm, P_{OUT} = 35 dBm, 100 kHz RBW
Stability	–	–	10:1	–	–	all spurious outputs < – 60 dBc, VSWR load, all phase angles
Input VSWR	–	3:1	1.7:1	–	–	–

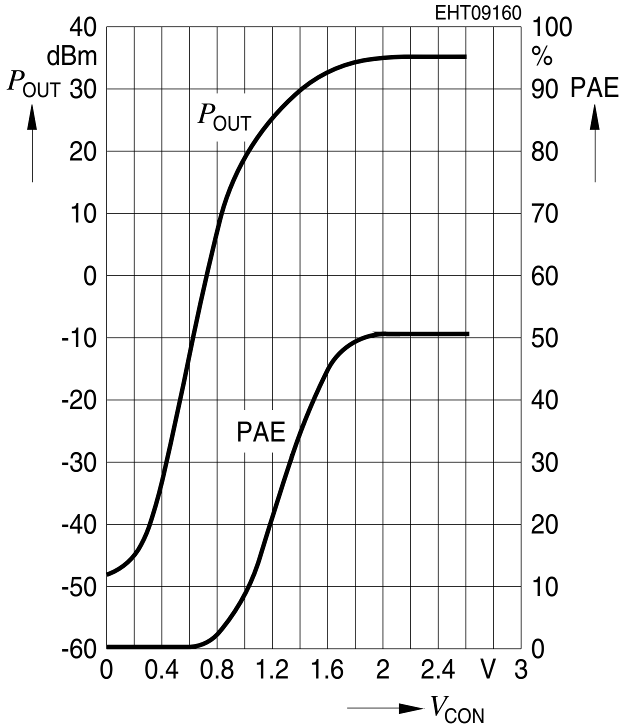
Output Power and PAE vs. Input Power

V_D = 3.5 V, $V_{Control}$ = 2.2 V, f = 900 MHz, duty cycle 12.5%, t_{ON} = 577 µs



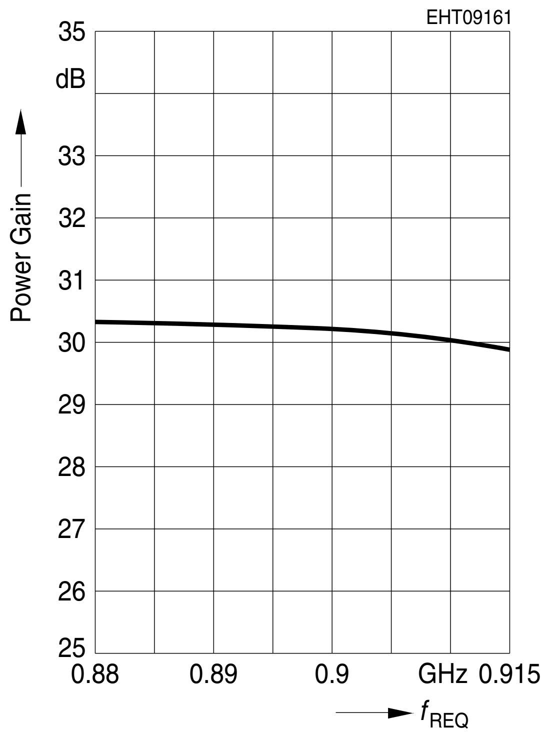
Output Power and PAE vs. Control Voltage

V_D = 3.5 V, P_{IN} = 0 dBm, f = 900 MHz, duty cycle 12.5%, t_{ON} = 577 µs



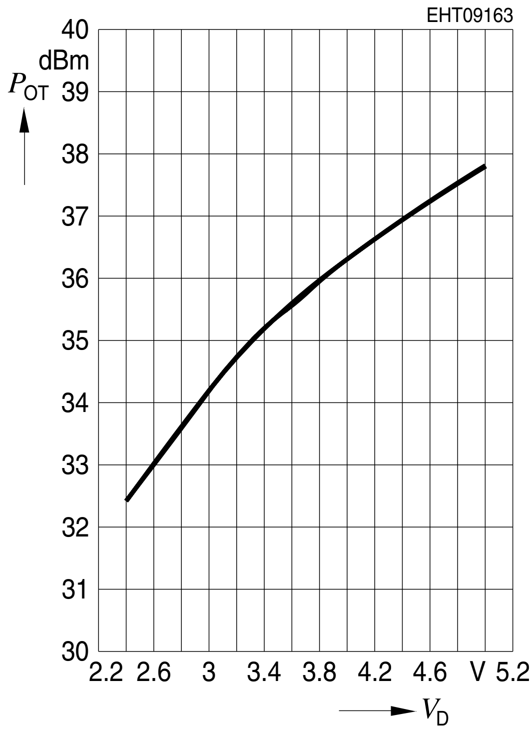
Power Gain and Input Return Loss vs. Frequency

V_D = 3.5 V, $V_{Control}$ = 2.2 V, P_{IN} = 5 dBm, duty cycle 12.5%, t_{ON} = 577 µs



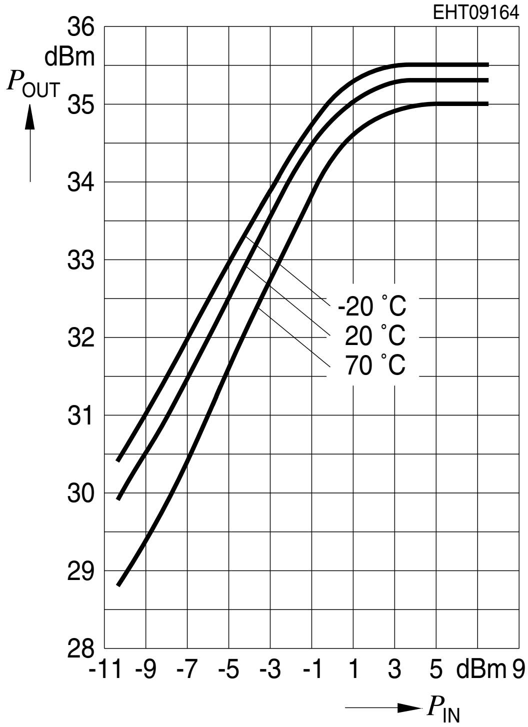
Output Power vs. Drain Voltage

matched for V_D = 3.5 V, $V_{Control}$ = 2.2 V, P_{IN} = 0 dBm, duty cycle 12.5%, t_{ON} = 577 µs



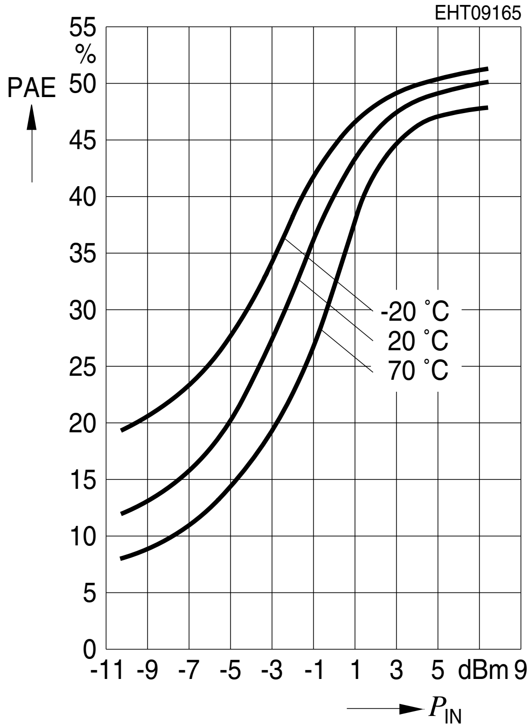
Output Power at Different Temperatures

V_D = 3.5 V, $V_{Control}$ = 2.2 V, f = 900 MHz, duty cycle 12.5%, t_{ON} = 577 µs



PAE at Different Temperatures

V_D = 3.5 V, $V_{Control}$ = 2.2 V, f = 900 MHz, duty cycle 12.5%, t_{ON} = 577 µs



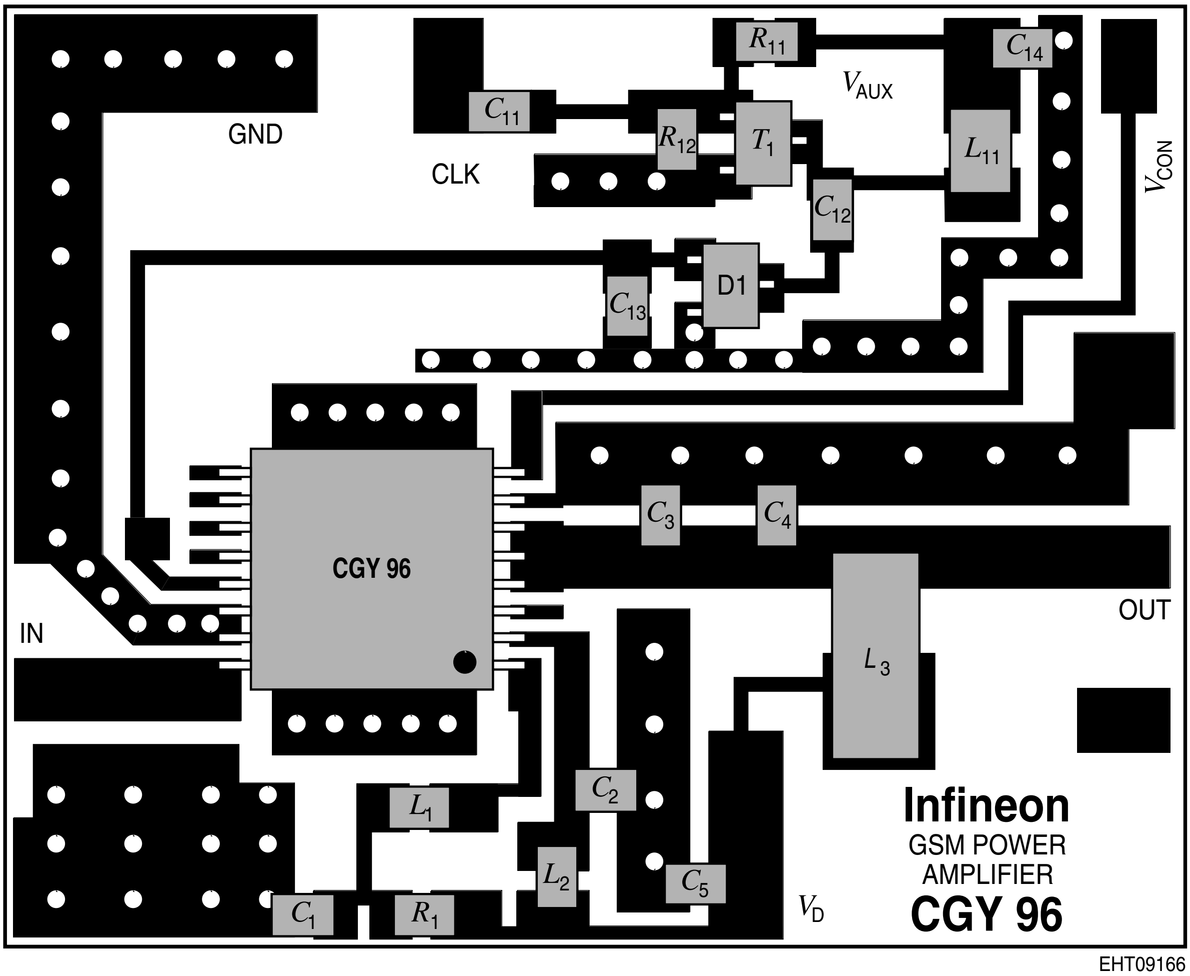


Figure 2 CGY 96 Evaluation Board

Layout size is 34 mm × 27 mm.

Connections

- V_D 2.7 to 6 VDC, pulsed (GSM: 12.5% duty cycle, t_{ON}= 0.577 ms)
- V_{AUX} 2.7 to 6 VDC
- $V_{Control}$ 0.2 to 2.2 VDC (0.2 V: min. P_{OUT}, 2.2 V: max. P_{OUT})
- CLK 5 MHz to 15 MHz (with a 10 µH inductor) or
  150 kHz to 250 kHz (with a 100 µH inductor instead of the 10 µH)
  (rectangular signal, 50% duty, 0 V to V_D voltage level)

Power on Sequence

1. continuous clock (CLK) on
2. turn on V_{AUX} ==> check negative voltage at pin#13 (– 5 … – 10 V)
3. turn on $V_{Control}$ (may be at the same time as 2)
   turn on Drain voltage V_D
   turn on Input Power

Operation without using the Negative Voltage Generator

Operation without using the on-board negative voltage generator is possible. In that case apply – 5 … – 8 V directly at pin#13 (V_{NEG}-pin). The devices in front of pin 13 are not necessary in that case.

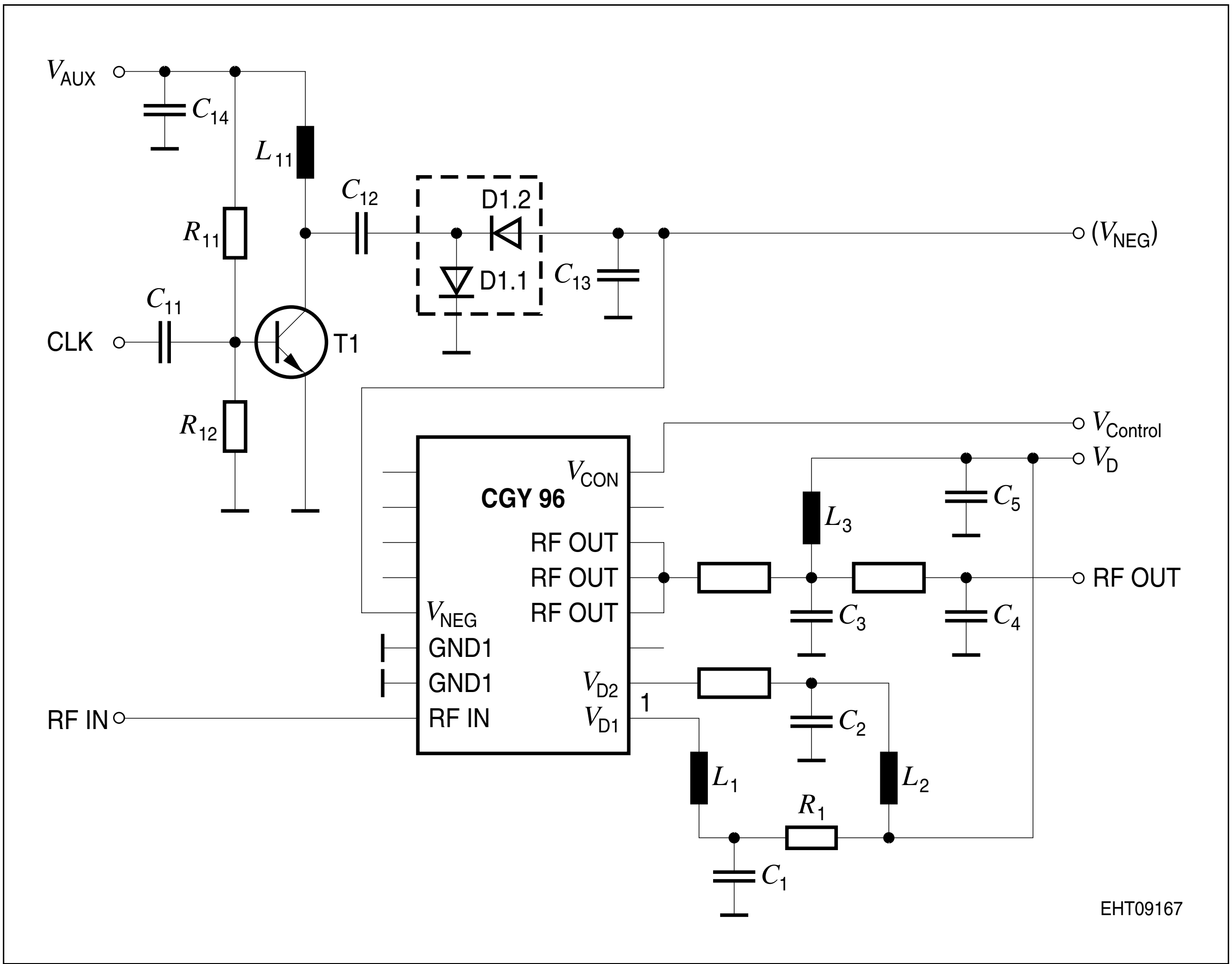


Figure 3 Application Circuit

Part List

CGY 96		Negative Voltage Generator	
L_1	33 nH	D_1	BAS 40-04W
L_2	33 nH	T_1	BC 848B
L_3	33 nH[1)]	L_{11}	10 µH
C_1	1 nF	C_{11}	1 nF
C_2	12 pF	C_{12}	1 nF
C_3	10 pF[2)]	C_{13}	47 nF
C_4	2.2 pF[2)]	C_{14}	1 nF
C_5	1 nF	R_{11}	3.8 kΩ
R_1	3.3 Ω	R_{12}	680 Ω

1) 33 nH SMD-Inductor for drain3: Part number BV1250 distributed by Horst David GmbH, 85375 Neufarn, Germany, Phone-No. +49-8165/9548-0, Fax-No. +49-8165/9548-28

2) for maximum efficiency use high quality capacitors for the output matching: Part-number ACCU-P0603 distributed by AVX GmbH, 85757 Karlsfeld, Germany, Phone-No. +49-8131/9004-0

Determination of Permissible Total Power Dissipation for Continuous and Pulse Operation

The purpose of the following procedure is to prevent the junction temperature T_j from exceeding the maximum allowed data sheet value. T_j is determined by the dissipated power and the thermal properties of the device and board. The dissipated power is the power which remains in the chip and heats the device and junction. It does not contain RF signals which are coupled out consistently.

This is a two step approach: For a pulsed condition both steps are needed. For CW and DC step one is sufficient.

Step 1: Continuous Wave / DC Operation

For the determination of the permissible total power dissipation $P_{tot\text{-}DC}$ from the diagram below it is necessary to obtain the temperature of the case T_C first. Because the MW-16 heat sink is not easily accessible to a temperature measurement the thermal resistance is defined as R_{thJC} using the case temperature T_C. There are two cases:

- When R_{thCA} (case to ambient) is not known: Measure T_C in operation of device and board at the upper side of the case where the temperature is highest. Small thermoelements (< 1 mm, thin wires, thermopaste) or thermopapers with low heat dissipation are well suited.

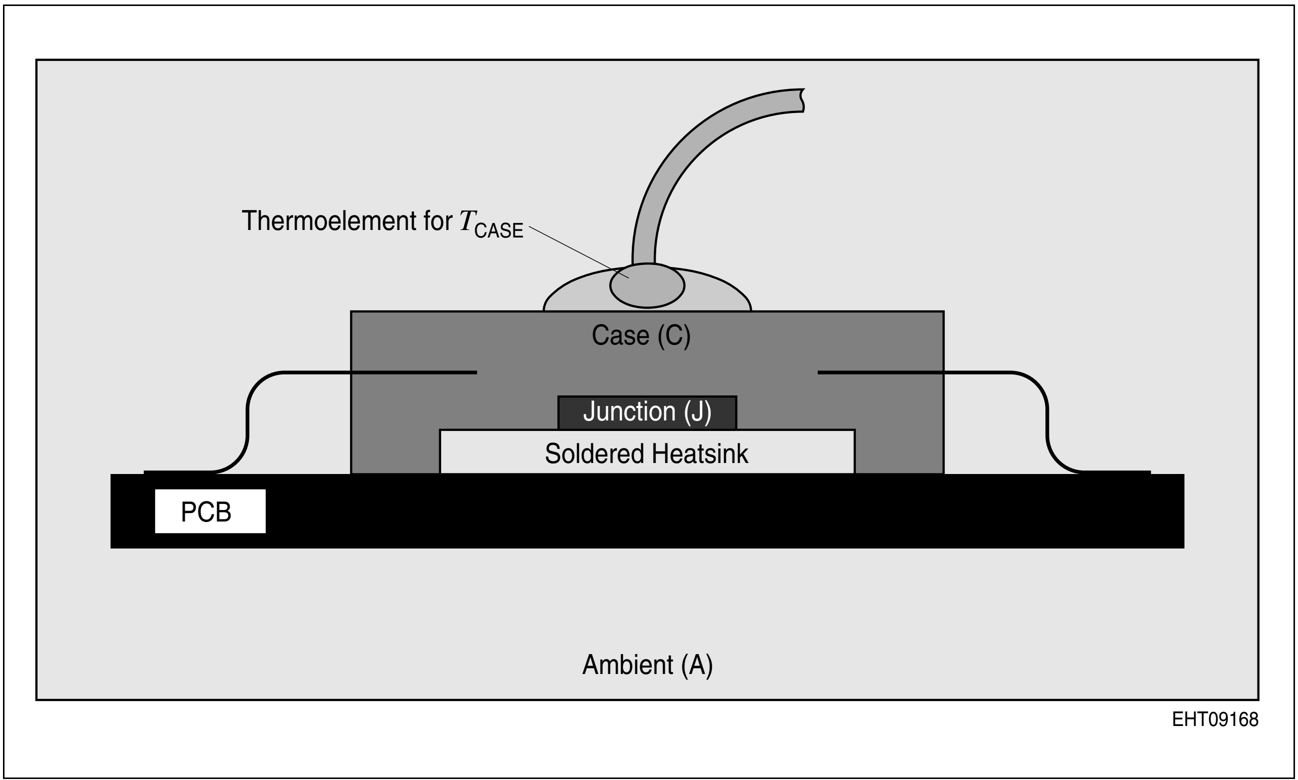
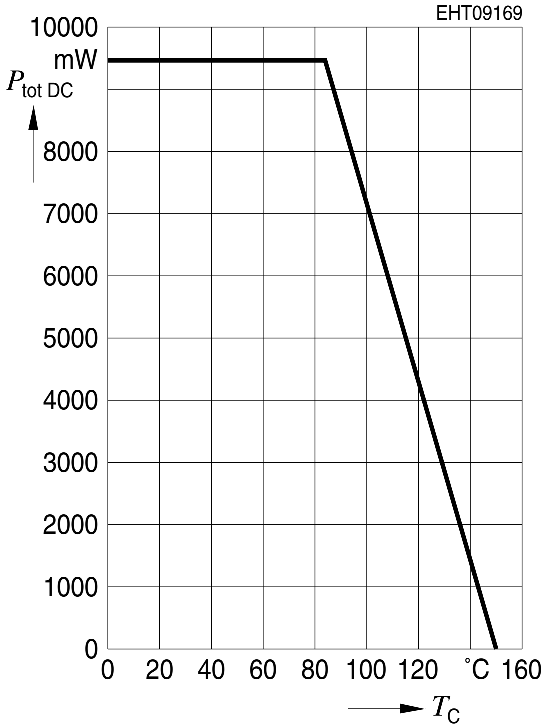


Figure 4 Measurement of Case Temperature T_C

- When R_{thCA} is already known.

  Calculate the case temperature as $T_C = P_{Diss} \times R_{thCA} + T_A$

Graph for $P_{tot\text{-}DC}$ [mW]



Step 2: Pulsed Operation

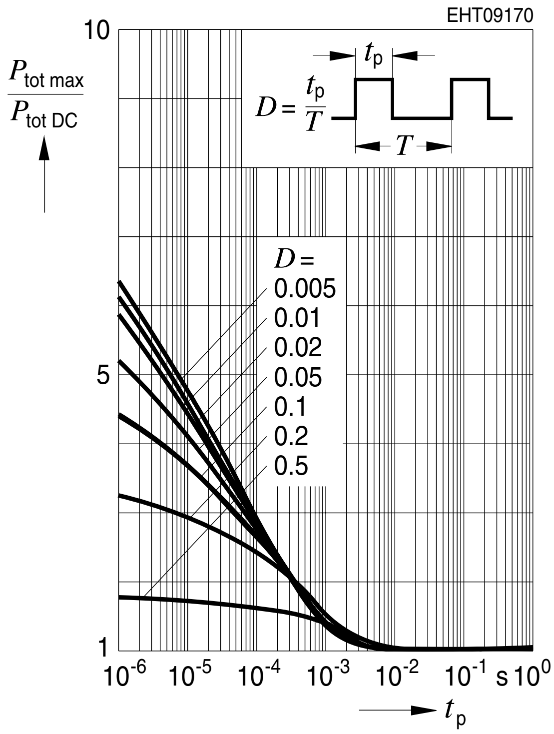
For the calculation of the permissible pulse load $P_{tot\text{-}max}$ the following formula is applicable:

$P_{tot\text{-}max} = P_{tot\text{-}DC} \times \text{Pulse Factor} = P_{tot\text{-}DC} \times (P_{tot\text{-}max}/P_{tot\text{-}DC})$

Use the values for $P_{tot\text{-}DC}$ as derived from the above diagram and for the Pulse Factor = $P_{tot\text{-}max}/P_{tot\text{-}DC}$ from the following diagram to get a specific value.

Pulse Factor

$P_{tot\text{-}max}/P_{tot\text{-}DC} = f(t_P)$



$P_{tot\text{-}max}$ should not exceed the absolute maximum rating for the dissipated power

P_{Pulse} = “Pulse peak power”

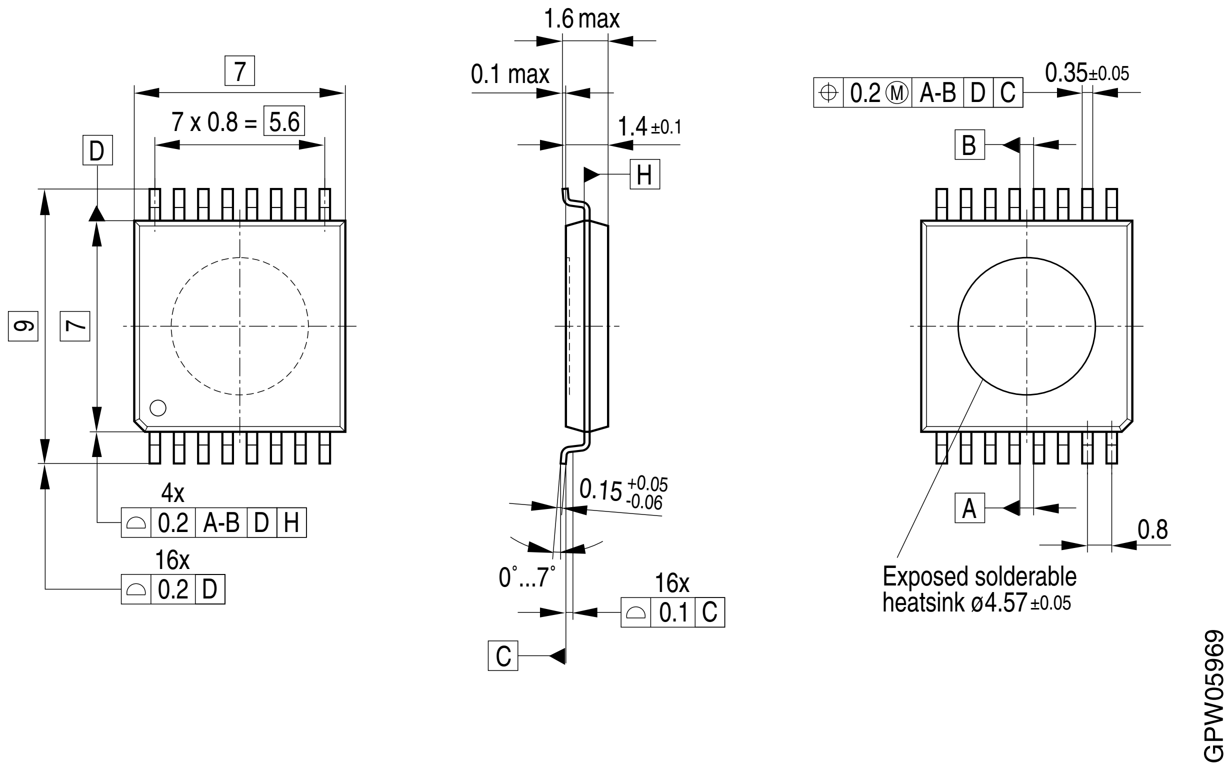
Reliability Considerations

The above procedure yields the upper limit for the power dissipation for continuous wave (cw) and pulse applications which correspond to the maximum allowed junction temperature. For best reliability keep the junction temperature low. The following formula allows to track the individual contributions which determine the junction temperature.

T_j =	($P_{tot\text{-}Diss}$/Pulse Factor ×	R_{thJC}) +	T_C
Junction temperature (= channel temperature)	Power dissipated in the chip, divided by the applicable pulse factor (= 1 for DC and CW). It does not contain decoupled RF- power	R_{th} of device from junction to case	Temperature of the case, measured or calculated, device and board operating

Package Outlines

MW-16
(Special Package)



Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm