Table 10. 3.3V DC Specifications

T_{CASE} = 0 to 95°C; $V_{CC}2$ = 2.9V (3.1V for 150 MHz) ±165mV; $V_{CC}3$ = 3.3V ±165mV

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL}3$	Input Low Voltage	–0.3	0.8	V	TTL Level (3)
$V_{IH}3$	Input High Voltage	2.0	$V_{CC}3$+0.3	V	TTL Level (3)
$V_{OL}3$	Output Low Voltage		0.4	V	TTL Level (1) (3)
$V_{OH}3$	Output High Voltage	2.4		V	TTL Level (2) (3)
$I_{CC}2$	Power Supply Current from 2.9V (3.1V for 150 MHz) core supply		1565 2085 2500 2775 3350	mA mA mA mA mA	@75 MHz (4) @100 MHz (4) (5) @120 MHz (4) @133 MHz (4) @150 MHz (4)
$I_{CC}3$	Power Supply Current from 3.3V I/O buffer supply		270 355 320 355 320	mA mA mA mA mA	@75 MHz (4) @100 MHz (4) (5) @120 MHz (4) @133 MHz (4) @150 MHz (4)

NOTES:

1. Parameter measured at 4 mA.
2. Parameter measured at 3 mA.
3. 3.3V TTL levels apply to all signals except CLK.
4. This value should be used for power supply design. It was determined using a worst-case instruction mix and V_{CC}+165mV. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes. For more information, refer to section 4.3.2.
5. Refer to document 242973 for previous process specification.

Table 11. 3.3V (5V Safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL}5$	Input Low Voltage	–0.3	0.8	V	TTL Level (1)
$V_{IH}5$	Input High Voltage	2.0	5.55	V	TTL Level (1)

NOTE:

1. Applies to CLK only.

Table 12. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	(4)
C_O	Output Capacitance		20	pF	(4)
$C_{I/O}$	I/O Capacitance		25	pF	(4)
C_{CLK}	CLK Input Capacitance		15	pF	(4)
C_{TIN}	Test Input Capacitance		15	pF	(4)
C_{TOUT}	Test Output Capacitance		20	pF	(4)
C_{TCK}	Test Clock Capacitance		15	pF	(4)
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{CC}3$ (1)
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{CC}3$ (1)
I_{IH}	Input Leakage Current		200	µA	V_{IN} = 2.4V (3)
I_{IL}	Input Leakage Current		-400	µA	V_{IN} = 0.4V (2)

NOTES:
1. This parameter is for input without pull up or pull down.
2. This parameter is for input with pull up.
3. This parameter is for input with pull down.
4. Guaranteed by design.

Table 13. Power Dissipation Requirements for Thermal Design

Parameter	Typical(1)	Max(2)	Unit	Notes
Thermal Design Power (7)		4.4 5.9 7.1 7.9 10.0	Watts Watts Watts Watts Watts	@75 MHz (6) @100 MHz (6) @120 MHz (5) @133 MHz @150 MHz
Active Power (8)	1.7--2.3 2.0--3.0 2.5--3.5 3.0--4.0 3.8--5.0	N/A	Watts Watts Watts Watts Watts	@75 MHz (6) @100 MHz (6) @120 MHz (5) @133 MHz @150 MHz
Stop Grant / Auto Halt Power		0.8 1.2 1.2 1.3 1.4	Watts Watts Watts Watts Watts	@75 MHz (3) @100 MHz (3) @120 MHz (3) @133 MHz (3) @150 MHz (3)
Stop Clock Power	.02	0.05	Watts	(4)

NOTES:

1. This is the typical power dissipation in a system. This value was the average value measured in a system using a typical device at $V_{CC}2$ = 2.9V (3.1V for 150 MHz) and $V_{CCC}3$ = 3.3V running typical applications. This value is highly dependent upon the specific system configuration. Typical power specifications are not tested.
2. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using a worst-case instruction mix with $V_{CC}2$ = 2.9V (3.1V for 150 MHz) and $V_{CC}3$ = 3.3V. The use of nominal V_{CC} in this measurement takes into account the thermal time constant of the package.
3. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.
5. The lower power number is due to a process improvement.
6. Refer to document 242973 for previous process specification.
7. Thermal Design Power is the maximum power dissipation under normal operating conditions at nominal $V_{CC}2$ worst case temperature, while executing the worst case power instruction mix.
8. Active Power is the average power measured in a system using a typical device running typical applications under normal operating conditions at nominal V_{CC} and room temperature.

4.3. AC Specifications

The AC specifications of the TCP Pentium processor with voltage reduction technology consist of setup times, hold times, and valid delays at 0 pF. All TCP Pentium processor with voltage reduction technology AC specifications are valid for $V_{CC}2$ = 2.9V (3.1V for 150 MHz) ±165mV, $V_{CC}3$ = 3.3V ±165mV and Tcase = 0 to 95°C.

4.3.1. POWER AND GROUND

For clean on-chip power distribution, the TCP Pentium processor with voltage reduction technology has 37 $V_{CC}2$ (2.9V power), 42 $V_{CC}3$ (3.3V power) and 72 V_{SS} (ground) inputs. Power and ground connections must be made to all external $V_{CC}2$, $V_{CC}3$ and V_{SS} pins of the Pentium processor with voltage reduction technology. On the circuit board all $V_{CC}2$ pins must be connected to a 2.9V V_{CC2} plane (or island) and all $V_{CC}3$ pins must be connected to a 3.3V $V_{CC}3$ plane. All V_{SS} pins must be connected to a V_{SS} plane. Please refer to Table 2 for the list of $V_{CC}2$, $V_{CC}3$ and V_{SS} pins.

4.3.2. DECOUPLING RECOMMENDATIONS

Transient power surges can occur as the processor is executing instruction sequences or driving large loads. To mitigate these high frequency transients, liberal high frequency decoupling capacitors should be placed near the processor.

Low inductance capacitors and interconnects are recommended for best high frequency electrical

performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible.

These capacitors should be evenly distributed around each component on the 3.3V plane and the 2.9V (3.1V for 150 MHz) plane (or island). Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

Power transients also occur as the processor rapidly transitions from a low level of power consumption to a much higher level (or high to low power). A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the processor to enter the Auto HALT Powerdown state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the processor. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µf range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor (on the 3.3V plane and the 2.9V (3.1V for 150 MHz) plane (or island)) to ensure that these supply voltages stay within specified limits during changes in the supply current during operation.

For more detailed information, please contact Intel or refer to the Pentium® Processor with Voltage Reduction Technology: Power Supply Design Considerations for Mobile Systems application note (Order Number 242558).

4.3.3. CONNECTION SPECIFICATIONS

All NC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to $V_{CC}3$. Unused active high inputs should be connected to ground.

4.3.4. AC TIMINGS FOR A 50-MHz BUS

The AC specifications given in Table 14 consist of output delays, input setup requirements and input hold requirements for a 50-MHz external bus. All AC specifications (with the exception of those for the TAP signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

Table 14. TCP Pentium® Processor with Voltage Reduction Technology AC Specifications for 50-MHz Bus Operation

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, T_{CASE} = 0°C to 95°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	25.0	50.0	MHz		
t_{1a}	CLK Period	20.0	40.0	nS	3	
t_{1b}	CLK Period Stability		±250	pS		(1), (19)
t_2	CLK High Time	4.0		nS	3	@2V, (1)
t_3	CLK Low Time	4.0		nS	3	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	3	(2.0V–0.8V), (1), (5)
t_5	CLK Rise Time	0.15	1.5	nS	3	(0.8V–2.0V), (1), (5)
t_{6a}	ADS#, PWT, PCD, BE0-7#, M/IO#, D/C#, CACHE#, SCYC, W/R# Valid Delay	1.0	7.0	nS	4	(22)
t_{6b}	AP Valid Delay	1.0	8.5	nS	4	(22)
t_{6c}	A3-A31, LOCK# Valid Delay	1.1	7.0	nS	4	(22)
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	(1), (22)
t_8	APCHK#, IERR#, FERR#, PCHK# Valid Delay	1.0	8.3	nS	4	(4), (22)
t_{9a}	BREQ, HLDA, SMIACT# Valid Delay	1.0	8.0	nS	4	(4), (22)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	4	(22)
t_{10b}	HITM# Valid Delay	1.1	6.6	nS	4	(22)
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	4	(22)
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	4	(22)
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	8.5	nS	4	(22)
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	5	(1)

Table 14. TCP Pentium® Processor with Voltage Reduction Technology
AC Specifications for 50-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, T_{CASE} = 0°C to 95°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{14}	A5-A31 Setup Time	6.5		nS	6	(20)
t_{15}	A5-A31 Hold Time	1.0		nS	6	
t_{16a}	INV, AP Setup Time	5.0		nS	6	
t_{16b}	EADS# Setup Time	6.0		nS	6	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	6	
t_{18a}	KEN# Setup Time	5.0		nS	6	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	6	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	6	
t_{20}	BRDY# Setup Time	5.0		nS	6	
t_{21}	BRDY# Hold Time	1.0		nS	6	
t_{22}	BOFF# Setup Time	5.5		nS	6	
t_{22a}	AHOLD Setup Time	6.0		nS	6	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	6	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	6	
t_{25}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	6	
t_{25a}	HOLD Hold Time	1.5		nS	6	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	6	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	6	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	6	(11), (15), (16)

Table 14. TCP Pentium® Processor with Voltage Reduction Technology AC Specifications for 50-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, T_{CASE} = 0°C to 95°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	6	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs	6	(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	6	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	6	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs	6	(14), (16)
t_{34}	D0-D63, DP0-7 Read Data Setup Time	3.8		nS	6	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		nS	6	
t_{36}	RESET Setup Time	5.0		nS	7	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	7	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	7	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	7	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	7	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	7	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	7	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	7	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	7	To RESET falling edge (21)
t_{42d}	Reset Configuration Signal BRDY# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge (1), (21)

Table 14. TCP Pentium® Processor with Voltage Reduction Technology AC Specifications for 50-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, T_{CASE} = 0°C to 95°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{43a}	BF[1:0] Setup Time	1.0		mS	7	(18) to RESET falling edge
t_{43b}	BF[1:0] Hold Time	2.0		CLKs	7	(18) to RESET falling edge
t_{43c}	BE4# Setup Time	2.0		CLKs	7	To RESET falling edge
t_{43d}	BE4# Hold Time	2.0		CLKs	7	To RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	3	
t_{46}	TCK High Time	25.0		nS	3	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	3	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	3	(2.0V–0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	3	(0.8V–2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	9	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		nS	8	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	8	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	8	(8)
t_{54}	TDO Float Delay		25.0	nS	8	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	8	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	8	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	8	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	8	(3), (7), (10)

4.3.5. AC TIMINGS FOR A 60-MHz BUS

The AC specifications given in Table 15 consists of output delays, input setup requirements and input hold requirements for the 120-MHz Pentium processor. The AC specifications given in Table 16 consists of output delays, input setup requirements and input hold requirements for the 150-MHz Pentium processor. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

Table 15. Mobile Pentium® Processor 120 MHz AC Specifications for 60-MHz Bus Operation

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	30.0	60.0	MHz		
t_{1a}	CLK Period	16.67	33.33	nS	3	
t_{1b}	CLK Period Stability		±250	pS		(1), (19)
t_2	CLK High Time	4.0		nS	3	@2V, (1)
t_3	CLK Low Time	4.0		nS	3	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	3	(2.0V–0.8V), (1), (5)
t_5	CLK Rise Time	0.15	1.5	nS	3	(0.8V–2.0V), (1), (5)
t_{6a}	ADS#, PWT, PCD, BE0-7#, M/IO#, D/C#, CACHE#, SCYC, W/R# Valid Delay	1.0	7.0	nS	4	(22)
t_{6b}	AP Valid Delay	1.0	8.5	nS	4	(22)
t_{6c}	LOCK# Valid Delay	1.1	7.0	nS	4	(22)
t_{6e}	A3-A31, Valid Delay	1.1	6.3	nS	4	(22)
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	(1), (22)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	4	(4), (22)
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	4	(4), (22)
t_{9a}	BREQ, HLDA Valid Delay	1.0	8.0	nS	4	(4), (22)
t_{9b}	SMIACT# Valid Delay	1.0	7.6	nS	4	(22)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	4	(22)

Table 15. Mobile Pentium® Processor 120 MHz AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	4	(22)
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	4	(22)
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	4	(22)
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	4	(22)
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	5	(1)
t_{14}	A5-A31 Setup Time	6.0		nS	6	(20)
t_{15}	A5-A31 Hold Time	1.0		nS	6	
t_{16a}	INV, AP Setup Time	5.0		nS	6	
t_{16b}	EADS# Setup Time	5.5		nS	6	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	6	
t_{18a}	KEN# Setup Time	5.0		nS	6	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	6	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	6	
t_{20}	BRDY# Setup Time	5.0		nS	6	
t_{21}	BRDY# Hold Time	1.0		nS	6	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	6	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	6	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	6	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	6	
t_{25b}	HOLD Hold Time	1.5		nS	6	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	6	(11), (15)

Table 15. Mobile Pentium® Processor 120 MHz AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	6	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	6	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	6	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	6	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	6	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0–D63, DP0–7 Read Data Setup Time	3.0		nS	6	
t_{35}	D0–D63, DP0–7 Read Data Hold Time	1.5		nS	6	
t_{36}	RESET Setup Time	5.0		nS	7	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	7	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	7	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	7	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	7	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	7	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	7	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	7	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	7	To RESET falling edge (21)

Table 15. Mobile Pentium® Processor 120 MHz AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{42d}	Reset Configuration Signal BRDY# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge (1), (21)
t_{43a}	BF[1:0] Setup Time	1.0		mS	7	(18) to RESET falling edge
t_{43b}	BF[1:0] Hold Time	2.0		CLKs	7	(18) to RESET falling edge
t_{43c}	BE4# Setup Time	2.0		CLKs	7	To RESET falling edge
t_{43d}	BE4# Hold Time	2.0		CLKs	7	To RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	3	
t_{46}	TCK High Time	25.0		nS	3	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	3	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	3	(2.0V–0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	3	(0.8V–2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	9	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		nS	8	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	8	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	8	(8)
t_{54}	TDO Float Delay		25.0	nS	8	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	8	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	8	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	8	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	8	(3), (7), (10)

Table 16. Mobile Pentium® Processor 150 MHz AC Specifications for 60-MHz Bus Operation

$V_{CC}2$ = 3.1V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	30.0	60.0	MHz		
t_{1a}	CLK Period	16.67	33.33	nS	3	
t_{1b}	CLK Period Stability		±250	pS		(1), (19)
t_2	CLK High Time	4.0		nS	3	@2V, (1)
t_3	CLK Low Time	4.0		nS	3	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	3	(2.0V–0.8V), (1), (5)
t_5	CLK Rise Time	0.15	1.5	nS	3	(0.8V–2.0V), (1), (5)
t_{6a}	PWT, PCD, BE0-7#, D/C#, CACHE#, SCYC, W/R# Valid Delay	0.8	7.0	nS	4	(22)
t_{6b}	AP Valid Delay	1.0	8.5	nS	4	(22)
t_{6c}	LOCK# Valid Delay	1.1	7.0	nS	4	(22)
t_{6e}	A3-A16 Valid Delay	0.7	6.3	nS	4	(22)
t_{6f}	M/IO# Valid Delay	0.85	7.0	nS	4	(22)
t_{6g}	ADS# Valid Delay	0.7	8.5	nS	4	(22)
t_{6h}	A17-A31 Valid Delay	0.8	6.3	nS	4	(22)
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	(1), (22)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	0.85	8.3	nS	4	(4), (22)
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	4	(4), (22)
t_{9a}	BREQ, HLDA Valid Delay	1.0	8.0	nS	4	(4), (22)
t_{9b}	SMIACT# Valid Delay	1.0	7.6	nS	4	(22)
t_{10a}	HIT# Valid Delay	1.0	8.0	nS	4	(22)

Table 16. Mobile Pentium® Processor 150 MHz AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 3.1V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{10b}	HITM# Valid Delay	0.9	6.0	nS	4	(22)
t_{11a}	PM0-1, BP0-3 Valid Delay	0.85	10.0	nS	4	(22)
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	4	(22)
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	4	(22)
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	5	(1)
t_{14}	A5-A31 Setup Time	6.0		nS	6	(20)
t_{15}	A5-A31 Hold Time	1.0		nS	6	
t_{16a}	INV, AP Setup Time	5.0		nS	6	
t_{16b}	EADS# Setup Time	5.5		nS	6	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	6	
t_{18a}	KEN# Setup Time	5.0		nS	6	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	6	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	6	
t_{20}	BRDY# Setup Time	5.0		nS	6	
t_{21}	BRDY# Hold Time	1.0		nS	6	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	6	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	6	
t_{24}	BUSCHK#, EWBE#, HOLD, PEN# Setup Time	5.0		nS	6	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	6	
t_{25b}	HOLD Hold Time	1.5		nS	6	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	6	(11), (15)

Table 16. Mobile Pentium® Processor 150 MHz AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 3.1V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	6	(12)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	6	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	6	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	6	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	6	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0–D63, DP0–7 Read Data Setup Time	3.0		nS	6	
t_{35}	D0–D63, DP0–7 Read Data Hold Time	1.5		nS	6	
t_{36}	RESET Setup Time	5.0		nS	7	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	7	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15		CLKs	7	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	7	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	7	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	7	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	7	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	7	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	7	To RESET falling edge (21)

Table 16. Mobile Pentium® Processor 150 MHz AC Specifications for 60-MHz Bus Operation (Contd.)

$V_{CC}2$ = 3.1V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{42d}	Reset Configuration Signal BRDY# Hold Time, RESET driven synchronously	1.0		nS		To RESET falling edge (1), (21)
t_{43a}	BF[1:0] Setup Time	1.0		mS	7	(18) to RESET falling edge
t_{43b}	BF[1:0] Hold Time	2.0		CLKs	7	(18) to RESET falling edge
t_{43c}	BE4# Setup Time	2.0		CLKs	7	To RESET falling edge
t_{43d}	BE4# Hold Time	2.0		CLKs	7	To RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	3	
t_{46}	TCK High Time	25.0		nS	3	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	3	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	3	(2.0V–0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	3	(0.8V–2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	9	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		nS	8	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	8	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	8	(8)
t_{54}	TDO Float Delay		25.0	nS	8	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	8	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	8	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	8	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	8	(3), (7), (10)

4.3.6. AC TIMINGS FOR A 66-MHz BUS

The AC specifications given in Table 17 consist of output delays, input setup requirements and input hold requirements for the 66-MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5V for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

Table 17. Mobile Pentium® Processor AC Specifications for 66-MHz Bus Operation

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	33.33	66.6	MHz		
t_{1a}	CLK Period	15.0	30.0	nS	3	
t_{1b}	CLK Period Stability		±250	pS		(1), (19)
t_2	CLK High Time	4.0		nS	3	@2V, (1)
t_3	CLK Low Time	4.0		nS	3	@0.8V, (1)
t_4	CLK Fall Time	0.15	1.5	nS	3	(2.0V–0.8V), (1)
t_5	CLK Rise Time	0.15	1.5	nS	3	(0.8V–2.0V), (1)
t_{6a}	PWT, PCD, BE0-7#, D/C#, W/R#, CACHE#, SCYC Valid Delay	1.0	7.0	nS	4	
t_{6b}	AP Valid Delay	1.0	8.5	nS	4	
t_{6c}	LOCK# Valid Delay	1.1	7.0	nS	4	
t_{6d}	ADS# Valid Delay	1.0	6.0	nS	4	
t_{6e}	A3-A31 Valid Delay	1.1	6.3	nS	4	
t_{6f}	M/IO# Valid Delay	1.0	5.9	nS	4	
t_7	ADS#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	nS	5	(1)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	nS	4	(4)
t_{8b}	PCHK# Valid Delay	1.0	7.0	nS	4	(4)
t_{9a}	BREQ Valid Delay	1.0	8.0	nS	4	(4)
t_{9b}	SMIACT# Valid Delay	1.0	7.3	nS	4	(4)

Table 17. Mobile Pentium® Processor AC Specifications for 66-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{9c}	HLDA Valid Delay	1.0	6.8	nS	4	(4)
t_{10a}	HIT# Valid Delay	1.0	6.8	nS	4	
t_{10b}	HITM# Valid Delay	1.1	6.0	nS	4	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	nS	4	
t_{11b}	PRDY Valid Delay	1.0	8.0	nS	4	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	nS	4	
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	nS	5	(1)
t_{14}	A5-A31 Setup Time	6.0		nS	6	(20)
t_{15}	A5-A31 Hold Time	1.0		nS	6	
t_{16a}	INV, AP Setup Time	5.0		nS	6	
t_{16b}	EADS# Setup Time	5.0		nS	6	
t_{17}	EADS#, INV, AP Hold Time	1.0		nS	6	
t_{18a}	KEN# Setup Time	5.0		nS	6	
t_{18b}	NA#, WB/WT# Setup Time	4.5		nS	6	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		nS	6	
t_{20}	BRDY# Setup Time	5.0		nS	6	
t_{21}	BRDY# Hold Time	1.0		nS	6	
t_{22}	AHOLD, BOFF# Setup Time	5.5		nS	6	
t_{23}	AHOLD, BOFF# Hold Time	1.0		nS	6	
t_{24a}	BUSCHK#, EWBE#, HOLD, Setup Time	5.0		nS	6	
t_{24b}	PEN# Setup Time	4.8		nS	6	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		nS	6	
t_{25b}	HOLD Hold Time	1.5		nS	6	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		nS	6	(11), (15)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		nS	6	(12)

Table 17. Mobile Pentium® Processor AC Specifications for 66-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		nS	6	(11), (15), (16)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		nS	6	(12)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		(14), (16)
t_{31}	R/S# Setup Time	5.0		nS	6	(11), (15), (16)
t_{32}	R/S# Hold Time	1.0		nS	6	(12)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		(14), (16)
t_{34}	D0–D63, DP0–7 Read Data Setup Time	2.8		nS	6	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		nS	6	
t_{36}	RESET Setup Time	5.0		nS	7	(11), (15)
t_{37}	RESET Hold Time	1.0		nS	7	(12)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	7	(16)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	7	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		nS	7	(11), (15), (16)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		nS	7	(12)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	7	To RESET falling edge (15)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	7	To RESET falling edge (21)
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	7	To RESET falling edge (21)
t_{42d}	Reset Configuration Signal BRDY# Hold Time, RESET driven synchronously	1.0		nS	7	To RESET falling edge (1), (21)

Table 17. Mobile Pentium® Processor AC Specifications for 66-MHz Bus Operation (Contd.)

$V_{CC}2$ = 2.9V ±165mV, $V_{CC}3$ = 3.3V ±165mV, TCP T_{CASE} = 0°C to 95°C, SPGA T_{CASE} = 0°C to 85°C, C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{43a}	BF[1:0] Setup Time	1.0		mS	7	(18) to RESET falling edge
t_{43b}	BF[1:0] Hold Time	2.0		CLKs	7	(18) to RESET falling edge
t_{43c}	BE4# Setup Time	2.0		CLKs	7	To RESET falling edge
t_{43d}	BE4# Hold Time	2.0		CLKs	7	To RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		nS	3	
t_{46}	TCK High Time	25.0		nS	3	@2V, (1)
t_{47}	TCK Low Time	25.0		nS	3	@0.8V, (1)
t_{48}	TCK Fall Time		5.0	nS	3	(2.0V–0.8V), (1), (8), (9)
t_{49}	TCK Rise Time		5.0	nS	3	(0.8V–2.0V), (1), (8), (9)
t_{50}	TRST# Pulse Width	40.0		nS	9	(1), Asynchronous
t_{51}	TDI, TMS Setup Time	5.0		nS	8	(7)
t_{52}	TDI, TMS Hold Time	13.0		nS	8	(7)
t_{53}	TDO Valid Delay	3.0	20.0	nS	8	(8)
t_{54}	TDO Float Delay		25.0	nS	8	(1), (8)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	nS	8	(3), (8), (10)
t_{56}	All Non-Test Outputs Float Delay		25.0	nS	8	(1), (3), (8), (10)
t_{57}	All Non-Test Inputs Setup Time	5.0		nS	8	(3), (7), (10)
t_{58}	All Non-Test Inputs Hold Time	13.0		nS	8	(3), (7), (10)

NOTES:

Notes 2, 6 and 14 are general and apply to all standard TTL signals used with the Pentium® processor family.

1. Not 100 percent tested. Guaranteed by design.
2. TTL input test waveforms are assumed to be 0 to 3V transitions with 1V/nS rise and fall times.
3. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8V/ns ≤ CLK input rise/fall time ≤ 8V/ns.
6. 0.3V/ns ≤ input rise/fall time ≤ 5V/ns.
7. Referenced to TCK rising edge.

8. Referenced to TCK falling edge.
9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings (t_{55-58}).
11. Setup time is required to guarantee recognition on a specific clock.
12. Hold time is required to guarantee recognition on a specific clock.
13. All TTL timings are referenced from 1.5V.
14. To guarantee proper asynchronous recognition, the signal must have been de-asserted (inactive) for a minimum of two clocks before being returned active and must meet the minimum pulse width.
15. This input may be driven asynchronously.
16. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be de-asserted (inactive) for a minimum of two clocks before being returned active.
17. The D/C#, M/IO#, W/R#, CACHE#, and A5-A31 signals are sampled only on the CLK that ADS# is active.
18. BF should be strapped to $V_{CC}3$ or left floating.
19. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
20. Timing (t_{14}) is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active).
21. BUSCHK# is used as a reset configuration signal to select buffer size.
22. Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

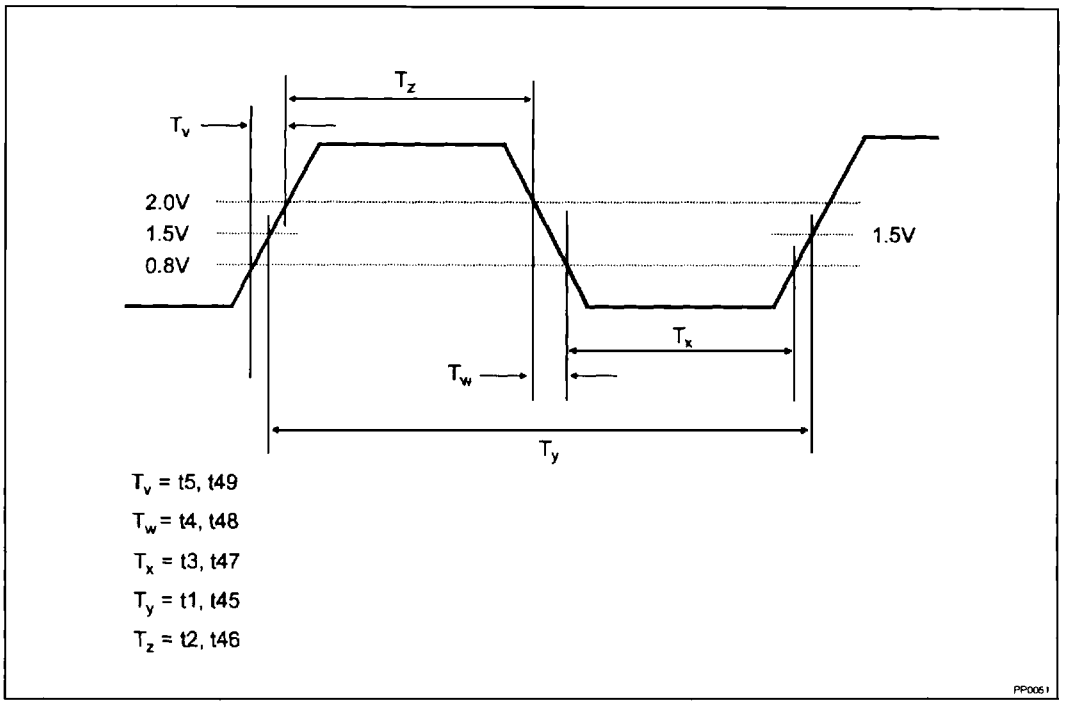


Figure 3. Clock Waveform

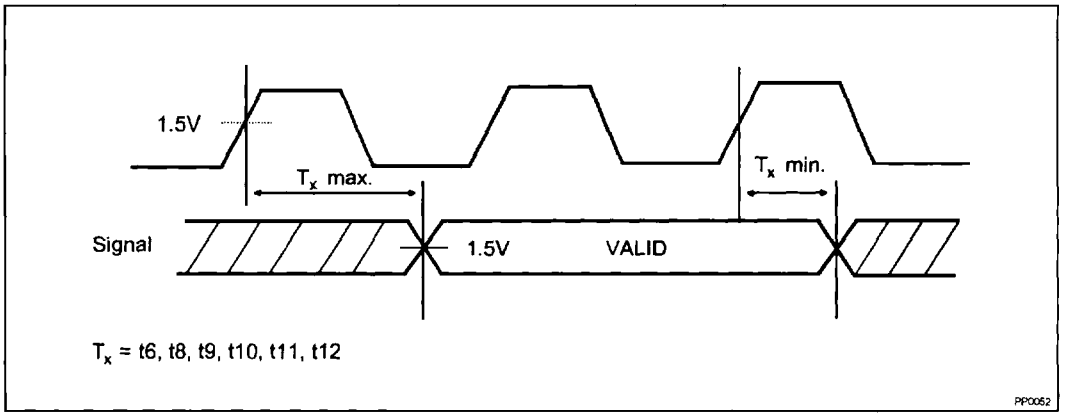


Figure 4. Valid Delay Timings

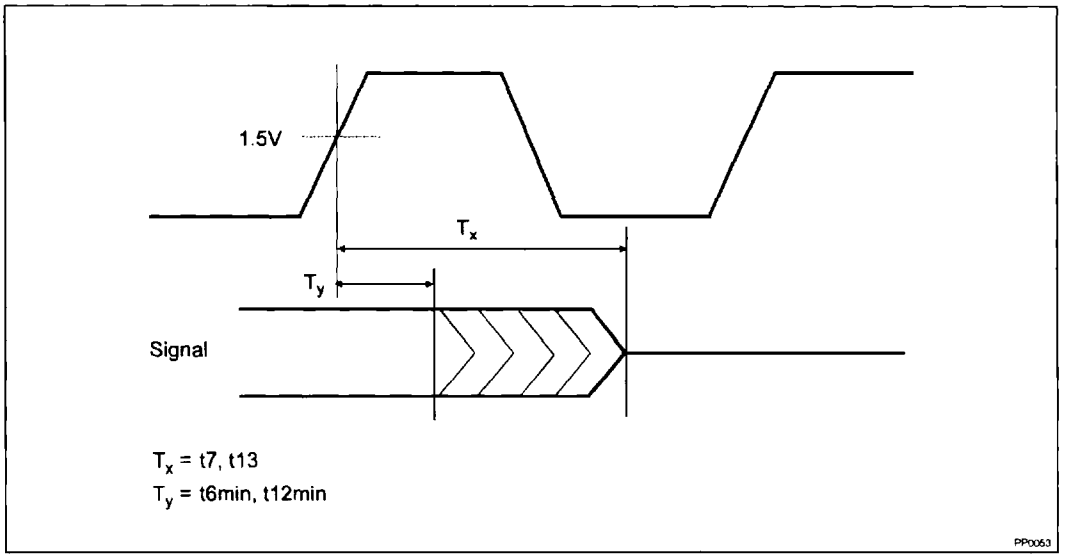


Figure 5. Float Delay Timings

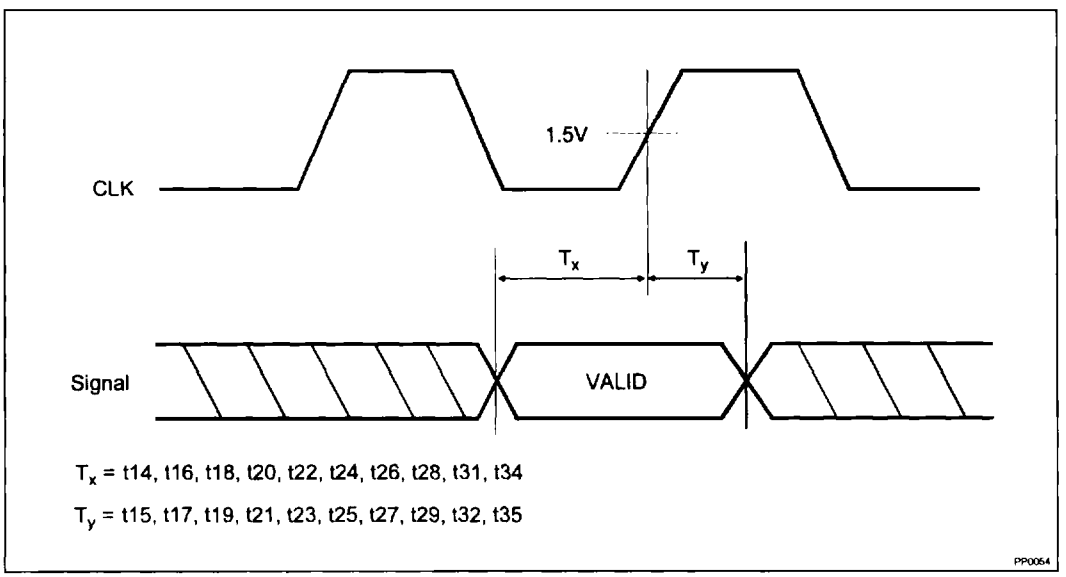
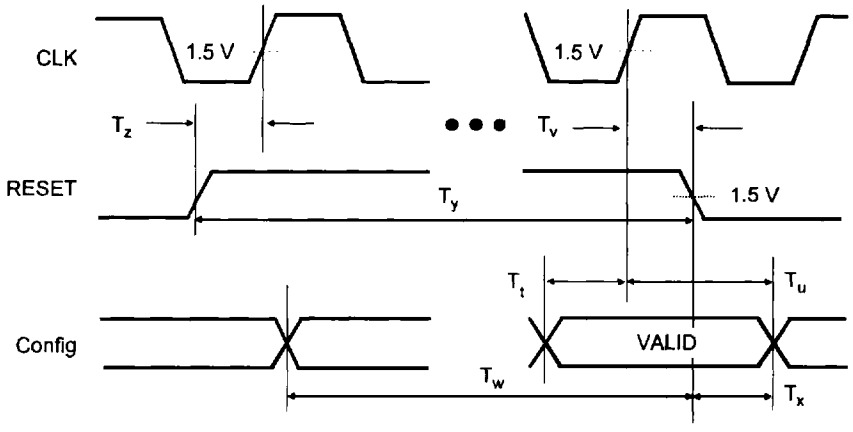


Figure 6. Setup and Hold Timings



T_t = t40

T_u = t41

T_v = t37

T_w = t42, t43a

T_x = t43b

T_y = t38, t39

T_z = t36

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Figure 7. Reset and Configuration Timings

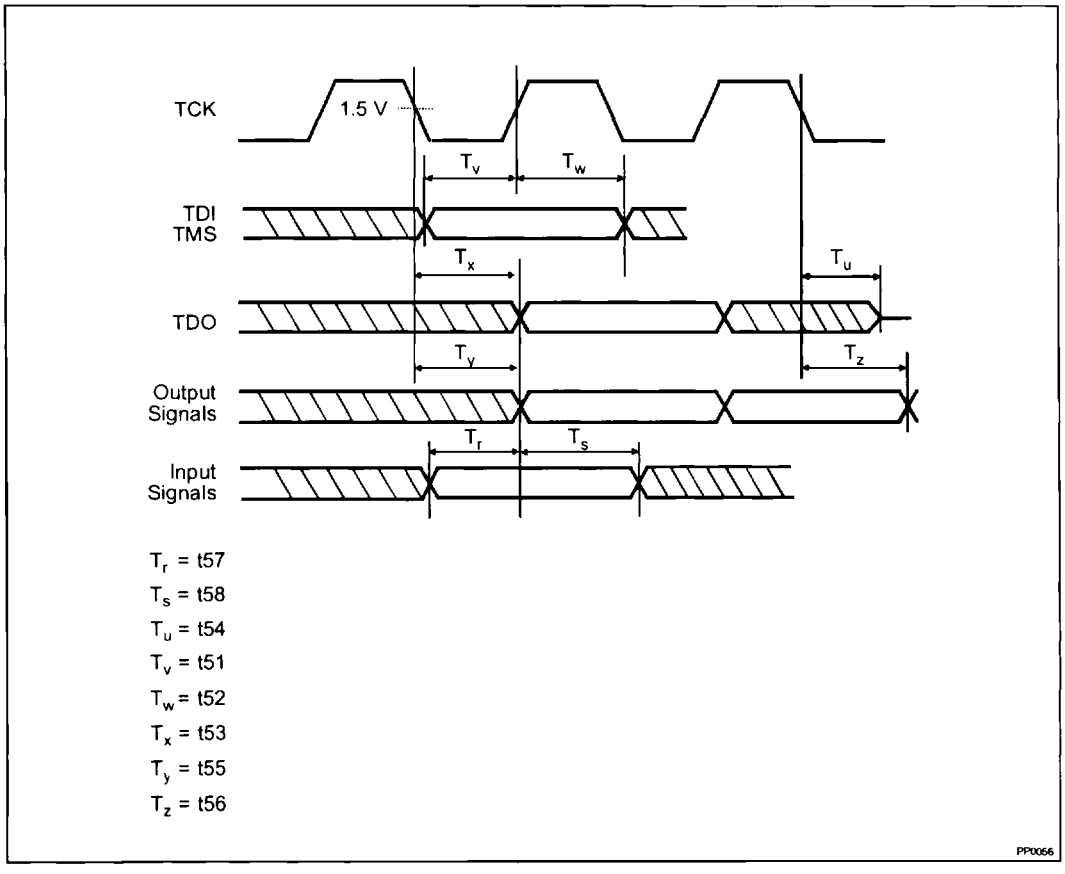


Figure 8. Test Timings

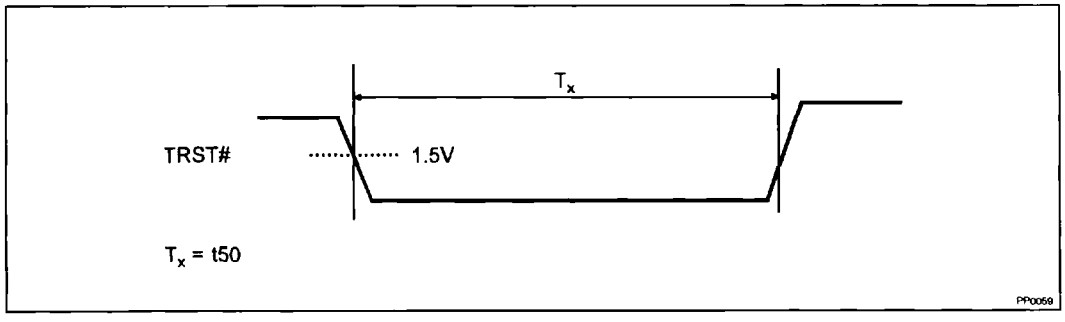


Figure 9. Test Reset Timings

4.4. I/O Buffer Models

This section describes the I/O buffer models of the Pentium processor with voltage reduction technology.

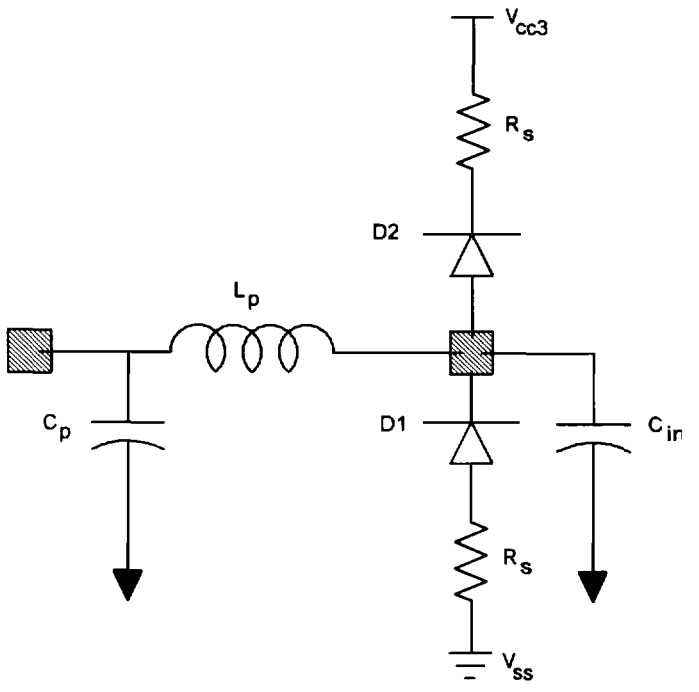
The first order I/O buffer model is a simplified representation of the complex input and output buffers used in the Pentium processor with voltage reduction technology. Figures 10 and 11 show the structure of the input buffer model and Figure 12 shows the output buffer model. Tables 18 and 19 show the parameters used to specify these models.

Although simplified, these buffer models will accurately model flight time and signal quality. For these parameters, there is very little added accuracy in a complete transistor model.

The following two models represent the input buffer models. The first model, Figure 10, represents all of the input buffers except for a special group of input buffers. The second model, Figure 11, represents these special buffers. These buffers are the inputs: AHOLD, EADS#, KEN#, WB/WT#, INV, NA#, EWBE#, BOFF# and CLK.

In addition to the input and output buffer parameters, input protection diode models are provided for added accuracy. These diodes have been optimized to provide ESD protection and provide some level of clamping. Although the diodes are not required for simulation, it may be more difficult to meet specifications without them.

Note, however, some signal quality specifications require that the diodes be removed from the input model. The series resistors (Rs) are a part of the diode model. Remove these when removing the diodes from the input model.



Note: V_{CC} in Figure 10 refers to the I/O buffer $V_{CC}3$.

PP0059

Figure 10. Input Buffer Model, Except Special Group

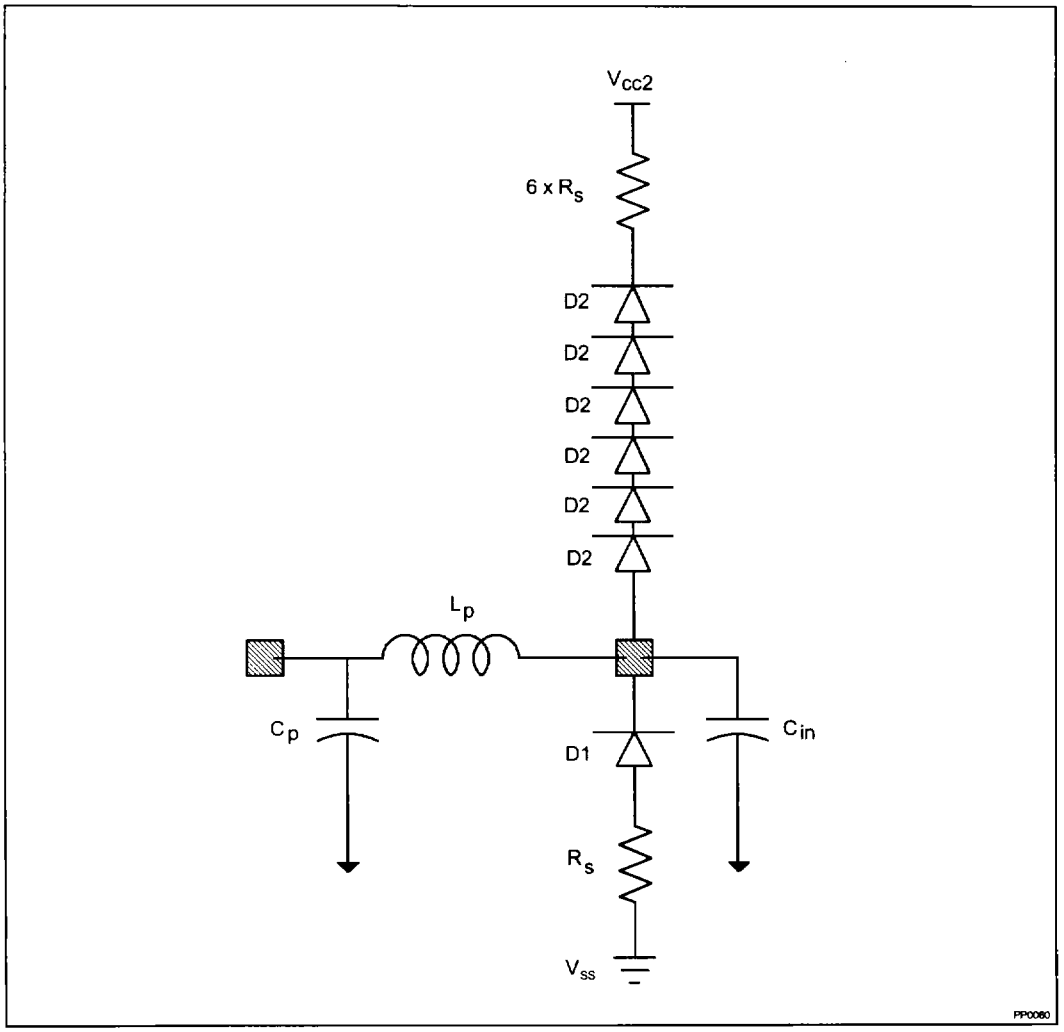


Figure 11. Input Buffer Model for Special Group

Table 18. Parameters Used in the Specification of the First Order Input Buffer Model

Parameter	Description
Cin	Minimum and Maximum value of the capacitance of the input buffer model
Lp	Minimum and Maximum value of the package inductance
Cp	Minimum and Maximum value of the package capacitance
Rs	Diode Series Resistance
D1, D2	Ideal Diodes

Figure 12 shows the structure of the output buffer model. This model is used for all of the output buffers of the Pentium processor with voltage reduction technology.

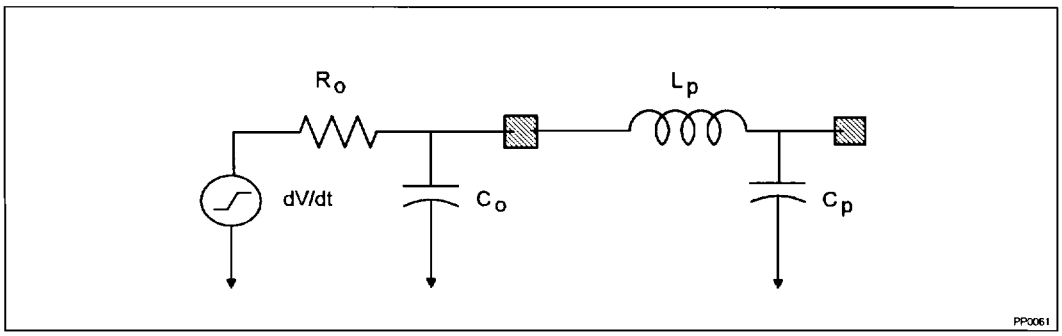


Figure 12. First Order Output Buffer Model

Table 19. Parameters Used in the Specification of the First Order Output Buffer Model

Parameter	Description
dV/dt	Minimum and maximum value of the rate of change of the open circuit voltage source used in the output buffer model
Ro	Minimum and maximum value of the output impedance of the output buffer model
Co	Minimum and Maximum value of the capacitance of the output buffer model
Lp	Minimum and Maximum value of the package inductance
Cp	Minimum and Maximum value of the package capacitance

4.4.1. BUFFER MODEL PARAMETERS

This section gives the parameters for each TCP Pentium processor with voltage reduction technology input, output and bidirectional signal, as well as the settings for the configurable buffers.

Some pins on the TCP Pentium processor with voltage reduction technology have selectable buffer sizes. These pins use the configurable output buffer EB2. Table 20 shows the drive level for BRDY# required at the falling edge of RESET to select the buffer strength. The buffer sizes selected should be the appropriate size required; otherwise AC timings might not be met, or too much overshoot and ringback may occur. There are no other selection choices; all of the configurable buffers get set to the same size at the same time.

The input, output and bidirectional buffer values of the TCP Pentium processor with voltage reduction technology are listed in Table 22. This table contains listings for all three types, do not get them confused during simulation. When a bidirectional pin is operating as an input, use the Cin, Cp and Lp values; if it is operating as a driver, use all of the data parameters.

Please refer to Table 21 for the groupings of the buffers.

Table 20. Buffer Selection Chart

Environment	BRDY#	Buffer Selection
Typical Stand Alone Component	1	EB2
Loaded Component	0	EB2A

NOTES:
For correct buffer selection, the BUSCHK# signal must be held inactive (high) at the falling edge of RESET.

Table 21. TCP Signal to Buffer Type

Signals	Type	Driver Buffer Type	Receiver Buffer Type
CLK	I		ER0
A20M#, AHOLD, BF[1:0], BOFF#, BRDY#, BUSCHK#, EADS#, EWBE#, FLUSH#, HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, PEN#, R/S#, RESET, SMI#, STPCLK#, TCK, TDI, TMS, TRST#, WB/WT#	I		ER1
APCHK#, BE[7:5]#, BP[3:2], BREQ, FERR#, HLDA, IERR#, PCD, PCHK#, PM0/BP0, PM1/BP1, PRDY, PWT, SMIACT#, TDO, U/O#	O	ED1	
A[31:21], AP, BE[4:0]#, CACHE#, D/C#, D[63:0], DP[8:0], LOCK#, M/IO#, SCYC	I/O	EB1	EB1
A[20:3], ADS#, HITM#, W/R#	I/O	EB2/EB2A	EB2/EB2A
HIT#	I/O	EB3	EB3

Table 22. TCP Pentium® Processor Input, Output and Bidirectional Buffer Model Parameters

Buffer Type	Transition	dV/dt (V/nsec)		Ro (Ohms)		Cp (pF)		Lp (nH)		Co/Cin (pF)	
		min	max	min	max	min	max	min	max	min	max
ER0	Rising					0.3	0.4	3.9	5.0	0.8	1.2
(input)	Falling					0.3	0.4	3.9	5.0	0.8	1.2
ER1	Rising					0.2	0.5	3.1	6.0	0.8	1.2
(input)	Falling					0.2	0.5	3.1	6.0	0.8	1.2
ED1	Rising	3/3.0	3.7/0.9	21.6	53.1	0.3	0.6	3.7	6.6	2.0	2.6
(output)	Falling	3/2.8	3.7/0.8	17.5	50.7	0.3	0.6	3.7	6.6	2.0	2.6
EB1	Rising	3/3.0	3.7/0.9	21.6	53.1	0.2	0.5	2.9	6.1	2.0	2.6
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	0.2	0.5	2.9	6.1	2.0	2.6
EB2	Rising	3/3.0	3.7/0.9	21.6	53.1	0.2	0.5	3.1	6.4	9.1	9.7
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	0.2	0.5	3.1	6.4	9.1	9.7
EB2A	Rising	3/2.4	3.7/0.9	10.1	22.4	0.2	0.5	3.1	6.4	9.1	9.7
(bidir)	Falling	3/2.4	3.7/0.9	9.0	21.2	0.2	0.5	3.1	6.4	9.1	9.7
EB3	Rising	3/3.0	3.7/0.9	21.6	53.1	0.2	0.4	3.2	4.1	3.3	3.9
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	0.2	0.4	3.2	4.1	3.3	3.9

Table 23. Input Buffer Model Parameters: D (Diodes)

Symbol	Parameter	D1	D2
IS	Saturation Current	1.4e-14A	2.78e-16A
N	Emission Coefficient	1.19	1.00
RS	Series Resistance	6.5 ohms	6.5 ohms
TT	Transit Time	3 ns	6 ns
VJ	PN Potential	0.983V	0.967V
CJ0	Zero Bias PN Capacitance	0.281 pF	0.365 pF
M	PN Grading Coefficient	0.385	0.376

4.4.2. SIGNAL QUALITY SPECIFICATIONS

Signals driven by the system into the Pentium processor with voltage reduction technology must meet signal quality specifications to guarantee that the components read data properly and to ensure that incoming signals do not affect the reliability of the component. There are two signal quality parameters: Ringback and Settling Time.

4.4.2.1. Ringback

Excessive ringback can contribute to long-term reliability degradation of the Pentium processor with voltage reduction technology, and can cause false signal detection. Ringback is simulated at the input pin of a component using the input buffer model. Ringback can be simulated with or without the diodes that are in the input buffer model.

Ringback is the absolute value of the maximum voltage at the receiving pin below $V_{CC}3$ (or above V_{SS}) relative to $V_{CC}3$ (or V_{SS}) level after the signal has reached its maximum voltage level. The input diodes are assumed present.

Maximum Ringback on Inputs = 0.8V (with diodes)

If simulated without the input diodes, follow the Maximum Overshoot/Undershoot specification. By meeting the overshoot/undershoot specification, the signal is guaranteed not to ringback excessively.

If simulated with the diodes present in the input model, follow the maximum ringback specification.

Overshoot (Undershoot) is the absolute value of the maximum voltage above $V_{CC}3$ (below V_{SS}). The guideline assumes the absence of diodes on the input.

- • Maximum Overshoot/Undershoot on 5V 82497 Cache Controller, and 82492 Cache SRAM Inputs (CLK and PICCLK only) = 1.6V above $V_{CC}5$ (without diodes)
- Maximum Overshoot/Undershoot on 3.3V Pentium processor with voltage reduction technology Inputs (not CLK) = 1.4V above $V_{CC}3$ (without diodes)

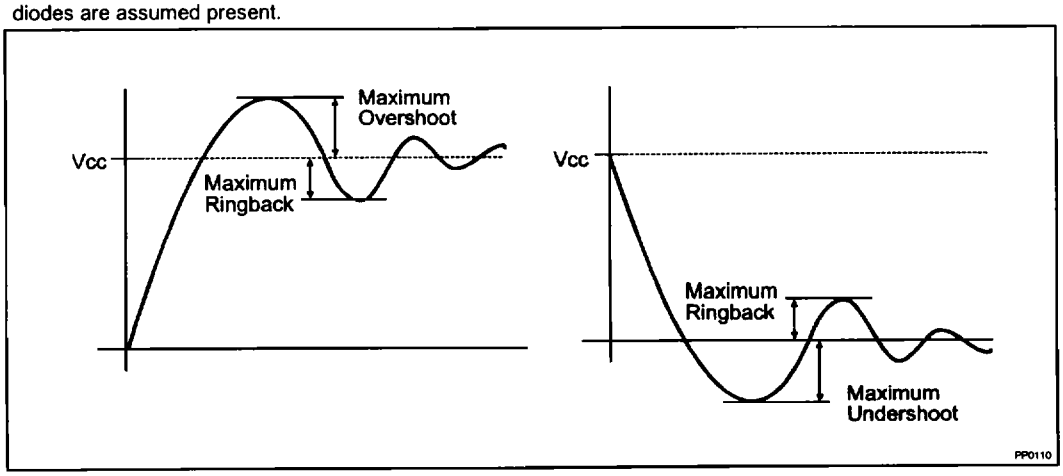


Figure 13. Overshoot/Undershoot and Ringback Guidelines

4.4.2.2. Settling Time

The settling time is defined as the time a signal requires at the receiver to settle within 10 percent of $V_{CC}3$ or V_{SS}. Settling time is the maximum time allowed for a signal to reach within 10 percent of its final value.

Most available simulation tools are unable to simulate settling time so that it accurately reflects silicon measurements. On a physical board, second-order effects and other effects serve to dampen the signal at the receiver. Because of all these concerns, settling time is a recommendation or a tool for layout tuning and not a specification.

Settling time is simulated at the slow corner, to make sure that there is no impact on the flight times of the signals if the waveform has not settled. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, settling time recommendation will be easier to meet.

Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts.

Use the following procedure to verify board simulation and tuning with concerns for settling time.

- Simulate settling time at the slow corner for a particular signal.
- If settling time violations occur, simulate signal trace with D.C. diodes in place at the receiver pin. The D.C. diode behaves almost identically to the actual (non-linear) diode on the part as long as excessive overshoot does not occur.
- If settling time violations still occur, simulate flight times for five consecutive cycles for that particular signal.
- If flight time values are consistent over the five simulations, settling time should not be a concern. If however, flight times are not consistent over the five simulations, tuning of the layout is required.
- Note that, for signals that are allocated two cycles for flight time, the recommended settling time is doubled.

A typical design method would include a settling time that ensures a signal is within 10 percent of $V_{CC}3$ or V_{SS} for at least 2.5 ns prior to the end of the CLK period.

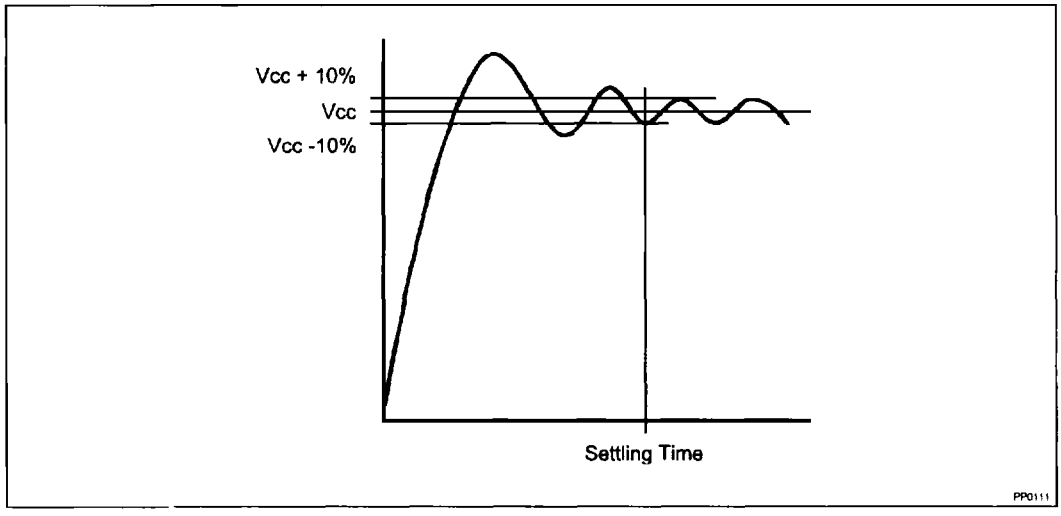


Figure 14. Settling Time

5.0. TCP PENTIUM® PROCESSOR MECHANICAL SPECIFICATIONS

Today's portable computers face the challenge of meeting desktop performance in an environment that is constrained by thermal, mechanical and electrical design considerations. These considerations have driven the development and implementation of Intel's Tape Carrier Package (TCP). The Intel TCP has been designed to offer a high pin count, low profile, reduced footprint package with uncompromised thermal and electrical performance. Intel continues to provide packaging solutions that meet our rigorous criteria for quality and performance, and this new entry into the Intel package portfolio is no exception.

Key features of the TCP include: surface mount technology design, lead pitch of 0.25 mm, polyimide body size of 24 mm and polyimide up for pick-and-place handling. TCP components are shipped with the leads flat in slide carriers, and are designed to be excised and lead formed at the customer manufacturing site. Recommendations for the manufacture of this package are included in Chapter 12 of the 1996 Packaging Data Book.

Figure 15 shows a cross-sectional view of the TCP as mounted on the Printed Circuit Board. Figures 16 and 17 show the TCP as shipped in its slide carrier, and key dimensions of the carrier and package. Figure 18 shows a cross-section detail of the package. Figure 19 shows an enlarged view of the outer lead bond area of the package.

Tables 24 and 25 provide the Pentium processor with voltage reduction technology TCP dimensions.

5.1. TCP Mechanical Diagrams

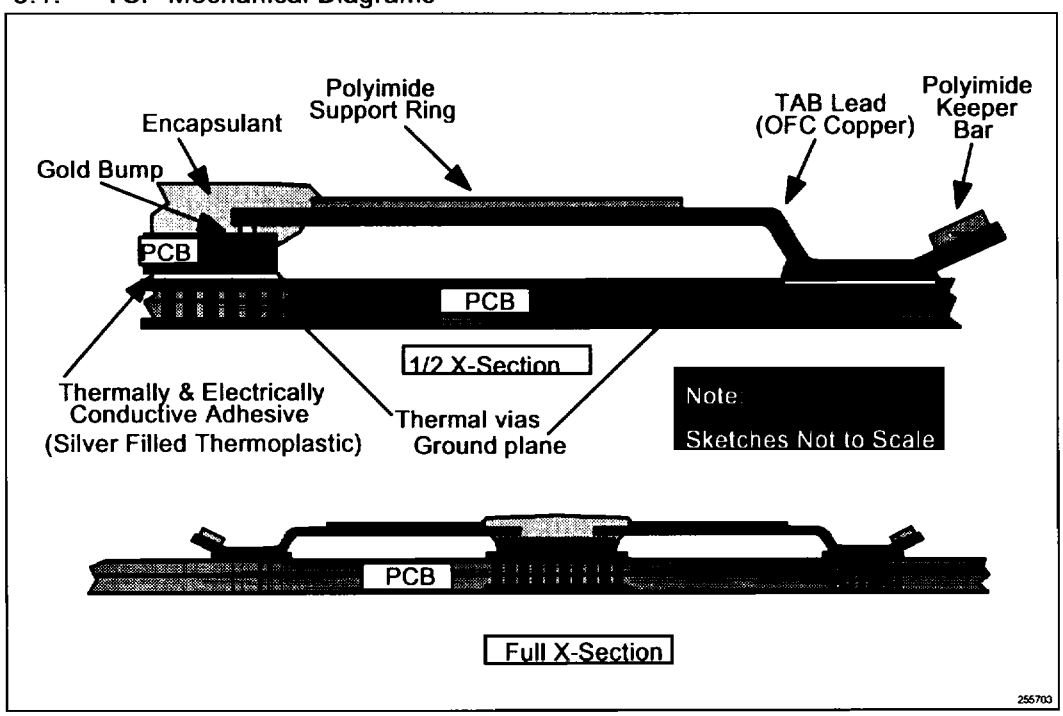


Figure 15. Cross-Sectional View of the Mounted TCP