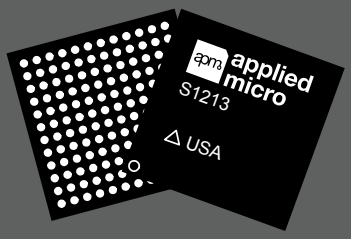
S1213

Quad Serial OC-3/12 - to - 8 Bit Transceiver

PRODUCT BRIEF



The S1213 device provides fully integrated serialization/de-serialization capabilities for Quad Transceiver. The device performs all necessary parallel-to-serial and serial-to-parallel functions in conformance with SONET/SDH transmission standards. The standard operating range is 155.52 Mbps or 622.08 Mbps.

Features

- CMOS 0.13 micron technology
- Complies with Bellcore and ITU-T specifications for jitter tolerance, jitter transfer, and jitter generation
- On-chip high-frequency PLLs for clock generation and clock recovery
- Supports Data Rates for 155.52 Mbps (OC-3) and 622.08 Mbps (OC-12).
- 8-bit LVCMOS Parallel data path
- Diagnostic loopback, Line loopback, Serial Clock loop timing and Parallel loop back modes
- Selectable reference frequencies of 77.76 or 155.52 MHz
- Directly compatible with 2.5 V or 3.3 V LVDS DC, 3.3 V LVPECL DC as well as AC interface
- Minimizes external components: No external loop filter component, Internally biased outputs, Internally provided common mode bias for AC input and internally provided bias for external LVPECL driver
- 255 Ball Grid Array Package
- 1.2 V and 3.3 V/2.5 V supply. No power sequencing required
- Lock detect
- Signal detect input (SD[3:0])
- Typical 635 mW power in LVDS mode
- Quad configuration, mixed OC-3/12
- Transmit FIFO, maximizing transmit timing
- BIST features

Applications

- SONET/SDH modules & test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

Overview

The S1213 operates in either OC-3 or OC-12 with a Clock Data Recovery feature.

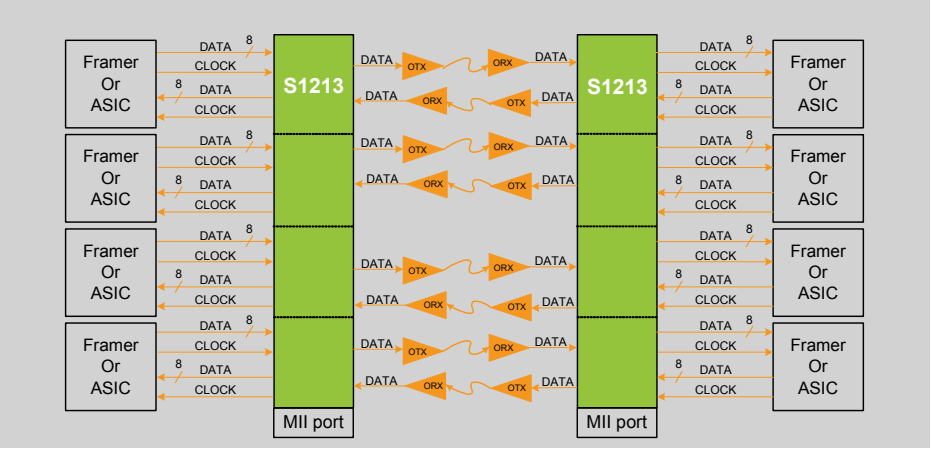
The S1213 can also be provisioned as a mix between OC-3 and OC-12 data for individual channels.

The S1213 can be configured in MII (Media Independent Interface) mode (MII Mode) and in Non-MII mode.

The figure below, System Block Diagram, shows a typical network application.

The quad S1213 transceiver implements SONET/SDH serialization/deserialization, and transmission functions. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The system timing circuitry consists of management of the data stream and clock distribution throughout the front end.

S1213 System Block Diagram



For technical support inquiries, submit your product related questions to support@appliedmicro.com.

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