PS20060
MOPLL with IF AGC Amplifier
Preliminary Information

Data Sheet 291359 issue 1 Aug-11

DESCRIPTION

The PS20060 is a 3 band MOPLL with IF AGC amplifier. It down-converts the RF channel to a standard IF followed by filtering and IF AGC amplification for the digital channel. Each band consists of a low noise preamplifier / mixer and local oscillator with an external varactor tuned tank circuit. An IF level detector is included for control of the RFAGC. The Take Over Point (TOP) and time constant are both programmable. The PS20060 has excellent signal level handling performance in the presence of high level unwanted signals. All chip control is via I2C bus.

If higher performance is required, an alternative part, PS20063 is available with image reject down conversion.

APPLICATIONS

• DVB-T receiver systems
• ISDB-T receiver systems
• DVB-C cable receiver systems
• Terrestrial analog receivers

Ordering Information

PS20060C1Q1AT 48 QFN Tape & Reel
PS20060C1Q1A5 48 QFN Trays

-20°C to +85°C

Equivalent parts: CE5060

FEATURES

• Highly integrated mixer/oscillator PLL and IF AGC amplifier for multi band analog / digital terrestrial tuners and/or cable tuners
• Low phase noise PLL frequency synthesizer
• AGC output level detect with digital controlled threshold
• >50 dB Desired/Undesired ratio without pre filtering
• Separate analog and digital IF outputs
• >41 dB IF AGC Control range
• Power down modes to support power reduction initiatives
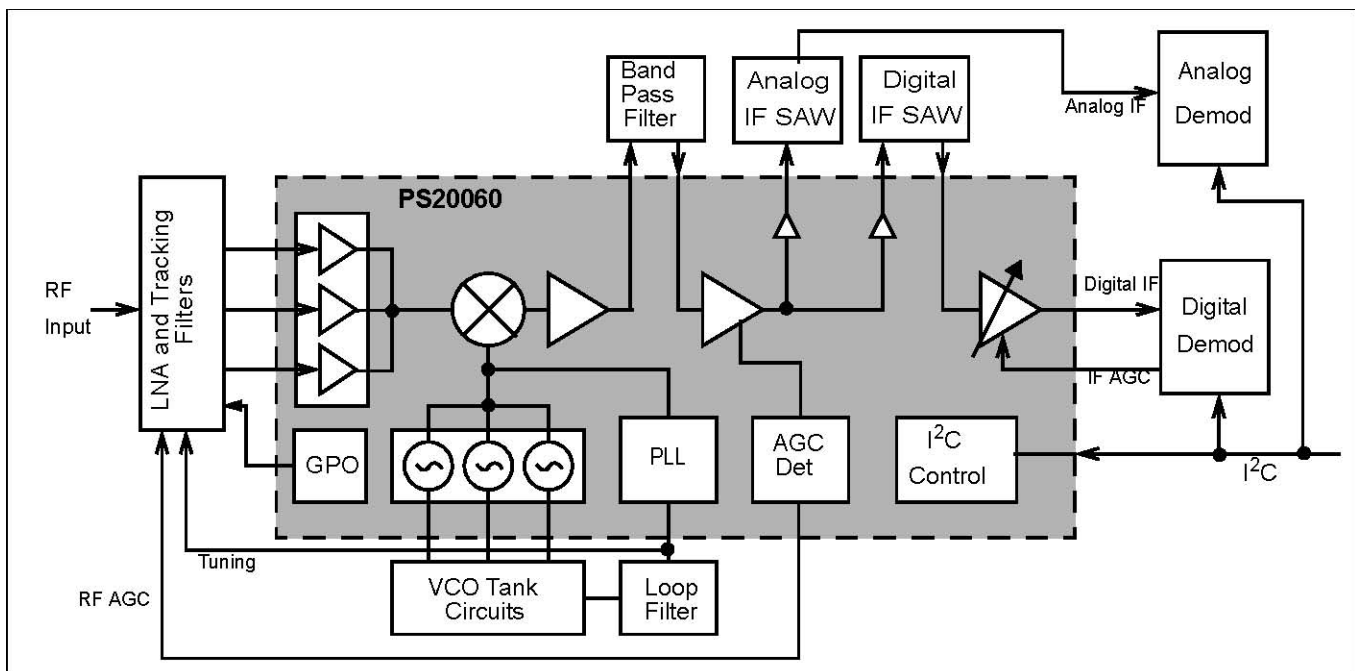• Four independent switching ports
• 48 pin QFN Package

Figure 1 -Basic Block Diagram

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Figure 2 - Pin Diagram

Table 1 - Pin Names

Pin No.	Port Name	Function
1	IFAGC	IF amplifier AGC input
2	SAB	Analog SAW filter driver differential outputs
3	SA	
4	ADC	External ADC input
5	SDA	I^2C bus serial data input/output
6	SCL	I^2C bus serial clock input
7	ADD	I^2C bus address selection input
8	AGCOP	AGC output
9	CNOPB	Converter differential outputs
10	CNOP	
11	CONT	Paddle (Ground)
12	VccRF	RF section supply
13	SIPB	SAW filter driver differential inputs
14	SIP	
15	GPP0	General purpose switching port
16	GPP1	General purpose switching port

Table 1 - Pin Names (continued)

Pin No.	Port Name	Function
17	GPP2	General purpose switching port
18	VeeRF	RF section ground
19	LOIP	Low band (VHF1) input
20	IPREF	Reference input for low and mid band inputs
21	MIDIP	Mid band (VHF3) input
22	HIIP	High band (UHF) differential inputs
23	HIIPB	
24	GPP3	General purpose switching port
25	LLOP	Low band local oscillator outputs
26	LLOPB	
27	LMOP	Mid band local oscillator outputs
28	LMOPB	
29	LHIP	High band local oscillator input
30	LHOP	High band local oscillator outputs
31	LHOPB	
32	LHIPB	High band local oscillator inverse input
33	VeeOSC	Oscillator section ground
34	VccOSC	Oscillator supply
35	IFIP	IF AGC amplifier differential inputs
36	IFIPB	
37	DRIVE	PLL Loop amplifier drive output
38	PUMP	PLL Loop amplifier charge pump output
39	VccDIG	Digital section supply
40	SD	Digital SAW filter driver differential outputs
41	SDB	
42	VccIF	IF amplifier section supply
43	XCAP	Reference oscillator feedback input
44	XTAL	Reference oscillator crystal drive
45	VccIF	IF amplifier section supply
46	VeeIF	IF section ground
47	IFOP	IF AGC amplifier differential outputs
48	IFOPB	
Paddle	Vee	Global ground
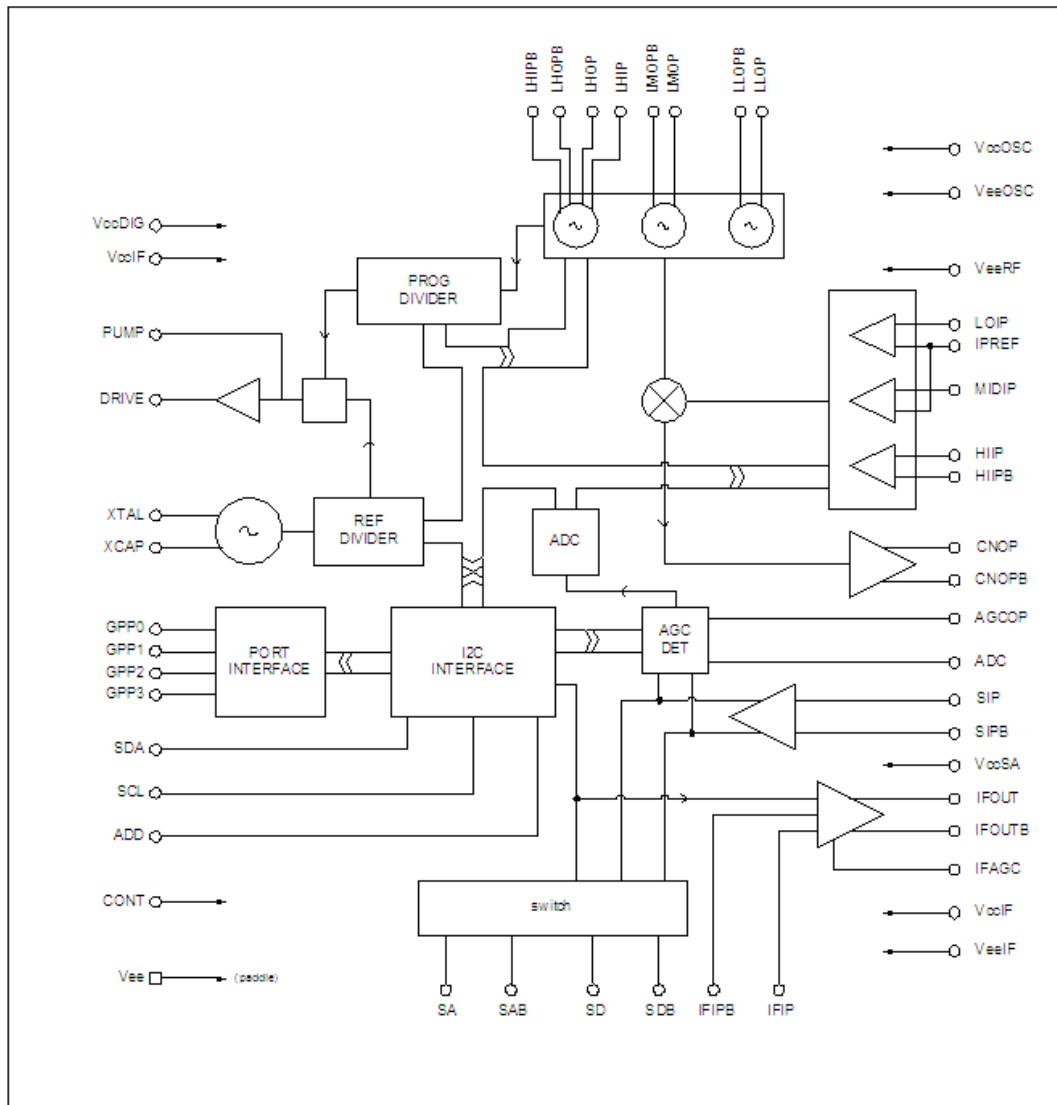
Figure 3 - Detailed Block Diagram

1.0   Functional Description

The PS20060 is a three-band RF mixer oscillator with on-board frequency synthesizer and IF AGC amplifier, integrating all tuner active circuitry after the tracking filter into a single package.

It is intended for use in all band terrestrial tuners, and requires a minimum external component count. It contains all elements required for RF down conversion to a standard IF with the exception of external VCO tank circuits.

In normal applications the RF input is interfaced to the selected mixer oscillator preamplifier through the tuner pre-filter and AGC stages. The PS20060 provides an RF AGC control signal, which can be used to control the RF gain.

The preamplifier output feeds the mixer stage where the required channel is down converted to the IF frequency. The local oscillator frequency for the down conversion is obtained from the on board PLL and local oscillator, with an external varactor tuned tank.

The downconverted signal is then passed through an external filter into a SAW filter driver amplifier. This provides two output channels for hybrid analog and digital applications.

An AGC IF amplifier is included which provides an output signal to a digital demodulator.

The device is controlled through an I^2C compatible interface.

1.1   RF Converter

The PS20060 contains three input stages to cover the VHF1, VHF3 and UHF frequency bands. The inputs would normally be driven by front end amplifiers and tracking filters. All three inputs are differential, however, the VHF1 and VHF3 inputs would normally be driven single ended. These inputs therefore can share a common input reference pin. The UHF input should be driven with a differential signal. The inputs are all high impedance. The differential converter IF output is then passed through an external interstage filter. This can be tuned for 36 MHz for DVB-T applications but can also be used at 44 MHz and 57 MHz to be compatible with other TV standards. The recommended filter circuit is shown in figure 11. The design of this filter provides an impedance transformation as well as rejection of adjacent channels. A 0.5 dB Chebychev filter with 10 MHz bandwidth is recommended. This gives a flat response across the pass band and takes into account normal component tolerances.

1.2   SAW Driver Amplifier

The output of the interstage filter then passes to the SAW filter drive amplifier. This provides further amplification and interfaces to the SAW filter. Two SAW filter drive outputs are provided for hybrid analog and digital applications. Both output stages are identical, however, the digital output (SD, SDB) should always be used for digital applications, as the pin out of the device has been optimized to give the best isolation performance in this configuration. Output selection is programmable however it should be noted that the unselected output is not powered off but operates at a lower power level which means that a signal will still be present on the output, but with reduced output drive capability.

The differential outputs will drive a balanced SAW filter with a tuning inductor to resonate with the SAW filter input capacitance. The SAW filter can also be driven without the tuning inductor but this requires the addition of 360 ohm resistors to ground on the SAW driver outputs to increase the output drive capability. This will increase total current consumption by approximately 14 mA.

1.3   AGC Detector and ADC

The PS20060 contains a broadband AGC detector circuit which provides an output to provide gain control for the RF frontend gain stages. The detector input signal is derived from the signal level in the SAW driver amplifier. The composite signal at this point is the wanted signal plus adjacent channels (N +/- 1, N +/- 2, N +/- 3). The AGC detector threshold point at which the agc output becomes active can be programmed to one of eight levels via the I^2C interface. When the composite level reaches the agc threshold, the agc output pin will be active. The AGC attack current is fixed, however, the decay current can be programmed to two levels. The agc output can only drive a high impedance e.g., a dual gate FET. If RF gain control uses a PiN diode then a simple buffer circuit will be required.

An AGC flag output is also available through the I^2C interface. This indicates when the AGC output is active i.e., less than 4 volts.

The agc output level can also be monitored by an on chip 3 bit ADC. Although the ADC is 3 bits, only 5 levels are available. Alternatively the ADC can be programmed to measure the voltage on an external pin (ADC Pin 4).

1.4   IF AGC Amplifier

The AGC amplifier amplifies the output of the SAW filter for the digital channel and provides a differential output to the demodulator. The analog gain control signal is normally derived from the demodulator. At least 41 dB of gain control is provided.

The AGC amplifier can be powered down independently of the rest of the device if not required. This mode could be used in analog applications to reduce overall power consumption.
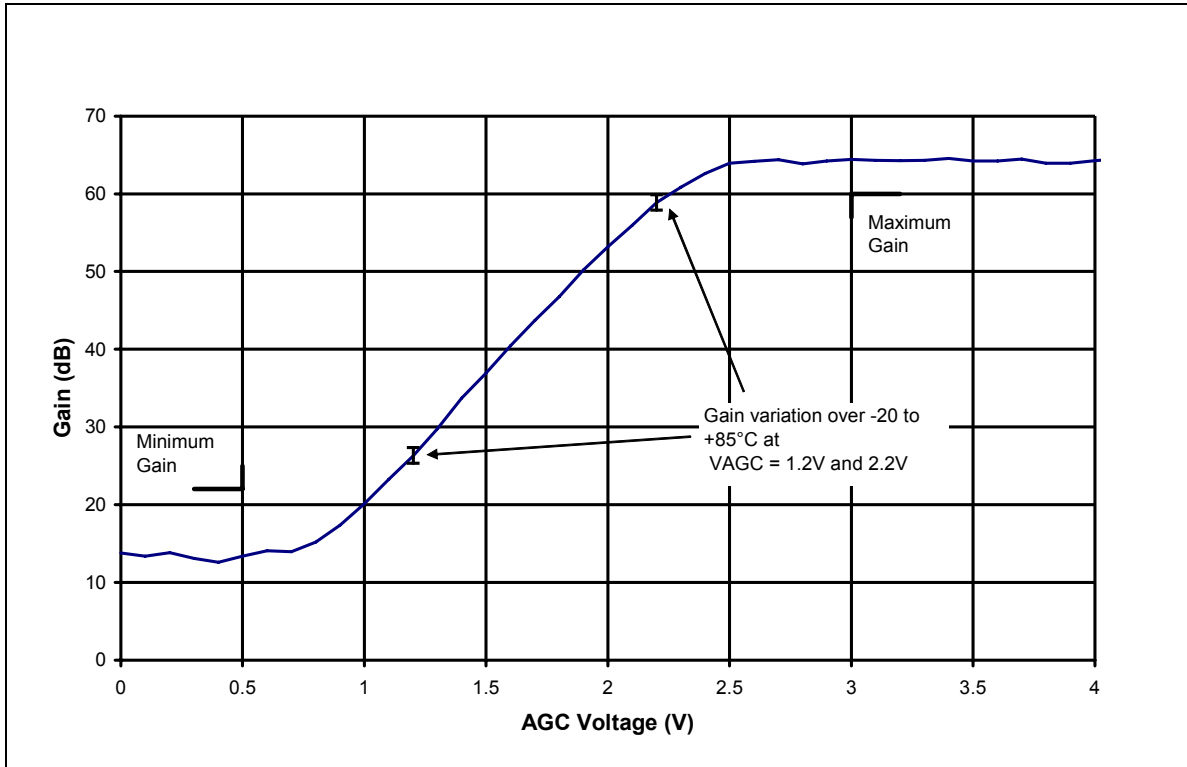
Figure 4 - Typical AGC Characteristic

1.5 VCO

Separate VCO's are provided for each band. The oscillator circuits are on chip however the tank circuitry is external. All three oscillators are differential. The typical external tank circuits are shown in Figures 5, 6 and 7. It is essential to take care to minimize track lengths and parasitics when designing the PCB layout to obtain best performance. The close-in phase noise of the local oscillator can be optimized at the programmed operating frequency by a programming bit which increases bias current in the VCO.
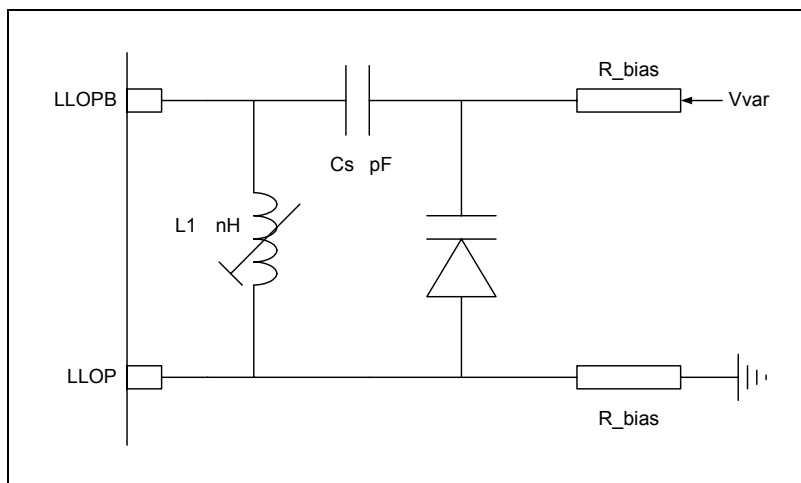
Figure 5 - Low Band (VHF1) External Tank Circuit
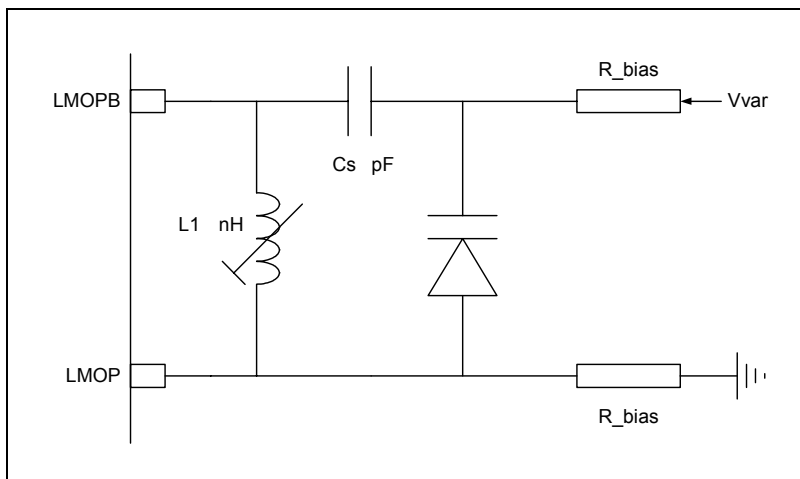
Figure 6 - Mid Band (VHF3) External Tank Circuit
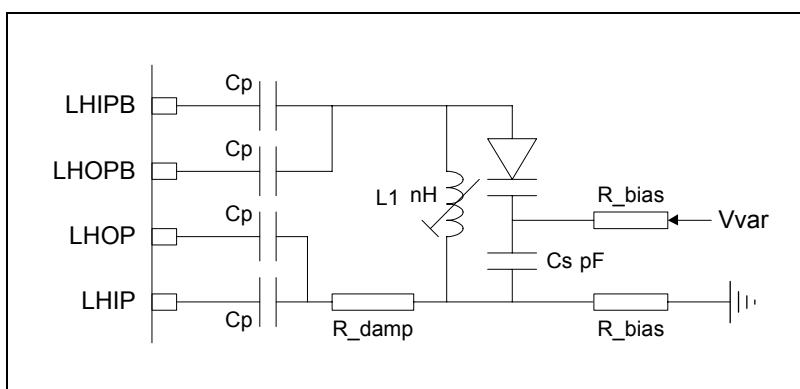
Figure 7 - High Band (UHF) External Tank Circuit

1.6   PLL Frequency Synthesizer

The PLL frequency synthesizer section contains all the elements necessary, with the exception of a frequency reference and loop filter to control a varicap tuned local oscillator, to form a complete PLL frequency synthesized source. The device allows operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with good phase noise performance. It can be operated with comparison frequencies appropriate for frequency offsets as required in digital terrestrial (DTT) receivers.

The LO input signal from the selected oscillator section is routed to an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier interfaces directly to the 15-bit programmable divider, which is of MN+A architecture, with a 16/17 dual modulus prescaler. The A counter is 4-bits, and the M counter is 11 bits.

The output of the programmable divider is fed to the phase comparator together with the comparison frequency, which is derived either from the on-board crystal controlled oscillator, or from an external reference source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider, which is programmable into 1 of 16 ratios.

The output of the phase detector feeds a charge pump and loop amplifier section, which when used with an external loop filter, integrates the current pulses into the varactor control voltage.

Test modes allow both the divider outputs to be monitored via output port GPP0 for debug and test purposes.

The PLL includes a lock detect circuit. The lock detect output is available by reading the Status byte on the I^{2}C interface

1.7   General Purpose Switching Ports

The PS20060 has four output switching ports. Three of these ports (GPP[3:1]) incorporate a 10 kohm pull up resistor. The remaining port (GPP0) is an open collector switch. These ports can be used for switching external RF input stages for example. Ports GPP[1:0] can also be used as test outputs for debug purposes.

1.8   I^{2}C Interface

The PS20060 is controlled by an I^{2}C data bus and is compatible with both 3.3 V and 5 V control levels.

Data and Clock are fed in on the SDA and SCL lines respectively as defined by I^{2}C bus format. The device can either accept data (write mode), or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low, and read mode if it is high. The device can be programmed to respond to 1 of 4 addresses, which enables the use of more than one device in an I^{2}C bus system. The address is selected by applying a voltage to the 'ADD' input.

When the device receives a valid address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are received. When the device is programmed into read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

2.0   Programming

The PS20060 is fully programmable through the I^{2}C interface. The device can also output data to the controller.

2.1   Programmable Features

Table 2 - Programmable Features

Feature	Description
RF programmable divider	Programs PLL main divider
Reference programmable divider	Programs PLL reference divider to set required frequency step
Band selection	Selects RF input and appropriate LO oscillator.
AGC Threshold	Sets the Input Power Level Threshold at which the AGC detector starts to generate a control level.
AGC Decay	Sets the AGC decay current.
Charge pump current	Selects one of the four charge pump current settings.
IF amplifier function	The IF amplifier can be enabled independently of other circuit blocks.
SAWF output select	Select the analog or digital SAW driver output.
Ports GPP[3:1]	These are configured as NPN buffers with 10 kohm pull-up resistors to V_{cc}. Logic '1' = on Logic '0' = off; default on power up
PORT GPP0	This is configured as a NPN open collector buffer. Logic '1' = on Logic '0' = off; default on power up
VCO Trim	Adjusts the VCO bias current to provide optimum phase noise performance.
ADC input Select	Select either the internal AGC detect output level or the external level applied to the ADC input pin.
Programmable power	The PS20060 has various power saving modes.
Test modes	Test modes to monitor and control internal PLL signals.

2.2   Register Map

There are a total of 7 write registers, the first of which is the Address register. The control registers are described in detail in the following section. The MSB of each register is written first.

After reception and acknowledgement of a correct address (Byte 1), the MSB of the following byte determines whether that byte is interpreted as a Byte 2 or Byte 4; a logic '0' indicating Byte 2, and a logic '1' indicating Byte 4. The next data byte will then be interpreted as Byte 3 or Byte 5 respectively. Byte 5 can be followed by Byte 6 and Byte 7 if required. A STOP condition can be generated after any data byte, however, if it occurs during a byte transmission, the previous byte data is retained. To facilitate smooth tuning, the frequency data bytes are only accepted by the device after all 15 bits of frequency data (i.e. Bytes 2 and 3) have been received, or after the generation of a STOP condition. It should also be noted that if it is necessary to program Bytes 6 or 7, then Bytes 4 and 5 must be programmed at the same time

Table 3 - Control Registers

	MSB							LSB	ACK	
	7	6	5	4	3	2	1	0		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	D14	D13	D12	D11	D10	D9	D8	A	**Byte 2W**
Programmable divider	D7	D6	D5	D4	D3	D2	D1	D0	A	**Byte 3W**
Control data	1	C1	C0	R4	R3	R2	R1	R0	A	**Byte 4W**
Control data	BS1	BS0	SL1	SL0	P3	P2	P1	P0	A	**Byte 5W**
Control Data	LO1	LO0	ATC	IFE	X	AT2	AT1	AT0	A	**Byte 6W**
Control Data	SAS	X	AGD	ADS	T3	T2	T1	T0	A	**Byte 7W**

A	Acknowledge bit
MA1, MA0	Address bits
D14-D0	Programmable division ratio control bits
R4-R0	Reference division ratio select
C1, C0	Charge pump current select
BS1-BS0	Band select bits
SL1-SL0	Power down modes
SAS	SAWF drive output select
P3-P0	P3-P0 port output states
ADS	ADC input select
ATC	AGC Decay Current
AGD	AGC Disable
AT2:AT0	AGC Onset threshold Control
LO1:LO0	LO trim control bits
T3-T0	Test mode control bits
IFE	IF AGC amplifier enable
X	Don't Care

Details of the programming registers are shown in the following sections. Default values on power up are also shown.

2.3   Address Register

The PS20060 address (MA1, MA0) are determined by the voltage set at the address pin (ADD) as shown in Table 4.

Table 4 - Address Bit MA1 and MA0 Settings

Address Select (Byte 1)		
MA1	**MA0**	**Address Input Voltage Level**
0	0	0 - 0.1Vcc (Connect to V_{ee})
0	1	$0.2V_{cc} – 0.3V_{cc}$ (Open circuit)
1	0	$0.4 V_{cc} – 0.6 V_{cc}$ (30KΩ to V_{cc})
1	1	$0.9 V_{cc} - 1.0 V_{cc}$ (Connect to V_{cc})

2.4   PLL Registers

Bytes 2,3 and 4 are used to program the PLL.

Table 5 - Byte 2- LO Divider (MSB)

Bit Field	Name	Default	Description
7	-	0	Must be set to 0 (Byte 2)
6:0	D[14:8]	0	MSB bits of LO Divider register.

Bit Field	Name	Default	Description
7:0	D[7:0]	0	LSB bits of LO Divider register.

Table 6 - Byte 3 LO Divider (LSB)

The LO frequency will not be updated until both Byte 1 and Byte 2 have been programmed.

Table 7 - Byte 4 PLL Control

Bit Field	Name	Default	Description
7	-	1	Must be set to 1(Byte 4)
6:5	C[1:0]	0	Charge pump current.
4:0	R[4:0]	10011	Reference divider control.

The charge pump current values are selected from the following table:

Table 8 - Charge Pump Current Selection

C1	C0	Current
		μA
0	0	+-155
0	1	+-330
1	0	+-690
1	1	+-1450
Default State on power up = 00		

The reference divider ratio can be selected from the following table:

Table 9 - Reference Divide Ratio Settings

R4	R3	R2	R1	R0	Ratio
0	0	0	1	1	16
0	0	1	0	0	32
0	0	1	0	1	64
0	0	1	1	0	128
0	1	0	1	1	20
0	1	1	0	0	40
0	1	1	0	1	80
0	1	1	1	0	160
1	0	0	1	1	24
1	0	1	0	0	48
1	0	1	0	1	96
1	0	1	1	0	192
1	1	0	1	1	28
1	1	1	0	0	56
1	1	1	0	1	112
1	1	1	1	0	224
Default State on power up = 10011					

2.5 Control Register - Byte 5

Table 10 - Byte 5 Control

Bit Field	Name	Default	Description
7:6	BS[1:0]	11	Band Switching
5:4	SL[1:0]	01	Power-up modes
3:0	P[3:0]	0	General Purpose Output ports

The band switching is controlled as shown below:

Table 11 - Band Selection

BS1	BS0	Band Selected
0	0	LO Band
0	1	MID Band
1	0	HI band
1	1	All off
		Default state on power up = 11

The various power-up modes are shown below. The IF AGC amplifier is controlled separately by IFE bit (see table 14). The I^{2}C interface and crystal oscillator circuit is active in all modes.

Table 12 - Internal Circuit Block Control

		Power Mode	Section Status			
SL1	SL0		I^{2}C interface and registers	Crystal oscillator	PLL & VCO	Converter and IF stages
0	X	Sleep	Enabled	Enabled	Disabled	Disabled
1	0	PLL and VCO enabled	Enabled	Enabled	Enabled	Disabled
1	1	Full	Enabled	Enabled	Enabled	Enabled

The PS20060 has four output ports. Ports GPP[3:1] have an internal 10 kohm pull up resistor to Vcc. GPP0 is open collector.

Table 13 - GPPO Output Port Control

Function	Bit	0	1
GPP0 output Enable	P0	Off (High Impedance)	On (Current Sink)
GPP1 output Enable	P1	Off	On (Current Sink)
GPP2 output Enable	P2	Off	On (Current Sink)
GPP3 output Enable	P3	Off	On (Current Sink)

2.6 Control Register - Byte 6

Table 14 - Byte 6 Control

Bit Field	Name	Default	Description
7	LO1	0	VCO Bias Trim
6	LO0	0	Not used
5	ATC	0	AGC Decay current select
4	IFE	0	IF AGC Amplifier enable (1 = On)
3	X	0	Not used
2:0	AT[2:0]	0	AGC Threshold Select

The VCO bias trim adjusts the VCO bias to give optimum close-in phase noise. In general this should be set to 1 for the lower third of the VCO frequency range.

The AGC attack current is fixed at 100 μA, however, the agc decay current can be programmed to one of two values as shown below. If the PLL is unlocked (FL = 0), then the ATC control is over-ridden and the AGC decay current is set to 10μA. When the PLL locks (FL = 1) the decay current reverts to the programmed ATC value. The decay current is always present even when the attack current is on. This means that if the 10μA decay current is selected, then the effective attack current is reduced to 90μA

.

Table 15 - AGC Decay Current Setting

ATC	AGC Decay Current (μA)
0	10.0
1	0.3

The AGC threshold can be programmed using the AT[2:0] bits. Note that the programmed value is dBμV peak. This is the signal level at the SAW driver outputs

Table 16 - AGC Threshold Selection

AT2	AT1	AT0	AGC Threshold (peak signal in dBμV into detector)
0	0	0	120
0	0	1	118
0	1	0	116
0	1	1	114
1	0	0	112
1	0	1	110
1	1	0	107
1	1	1	104
			Default state on power up = 000

2.7   Control Register - Byte 7

Table 17 - Byte 7 Control

Bit Field	Name	Default	Description
7	SAS	1	Digital SAW Drive Output Select (1 = Digital)
6	X	0	Not used
5	AGD	1	AGC Detector Enable (0 = Enabled)
4	ADS	0	ADC Input select
3:0	T[3:0]	0	Test Bits

The ADC input selection is shown in the table below

Table 18 - ADC Input Selection

ADS	ADC Function
0	AGC Output
1	External ADC input

The test bits T[3:0] allow internal PLL signals to be monitored and also to manually control charge pump current and AGC detector output. This facility may be useful during debug. The test bit selection is shown below. The reserved test modes should not be used.

Table 19 - Test Modes

T3	T2	T1	T0	Test Mode Description
0	0	0	0	Normal operation
0	0	0	1	Reserved Test Mode
0	0	1	0	AGC Sink, Force I_{agc} = -100 μA
0	0	1	1	AGC Source, Force I_{agc} = 10 μA P0 = Output of AGC bias DAC
0	1	0	0	Reserved Test Mode
0	1	0	1	Reserved Test Mode
0	1	1	0	Reserved Test Mode
0	1	1	1	Reserved Test Mode
1	0	0	0	Reserved Test Mode
1	0	0	1	Charge pump sink * Status byte FL set to logic '0'
1	0	1	0	Charge pump source * Status byte FL set to logic '0'
1	0	1	1	Charge pump disabled * Status byte FL set to logic '1'
1	1	0	0	Port P0 = $F_{pd}/2$
1	1	0	1	Charge pump sink * Status byte FL set to logic '0' Port P0 = F_{comp}

Table 19 - Test Modes (continued)

T3	T2	T1	T0	Test Mode Description
1	1	1	0	Charge pump source * Status byte FL set to logic '0' Port P0 = F_{comp}
1	1	1	1	Charge pump disabled * Status byte FL set to logic '1' Port P0 = F_{comp}

2.8 Read Mode

When the device is in read mode, the status byte read from the device takes the form shown in Table 20.

Table 20 - Read Data Format (MSB is transmitted first)

	MSB							LSB	ACK	
	7	6	5	4	3	2	1	0		
Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status Byte	POR	FL	0	0	AGF	V2	V1	V0	A	**Byte 2R**

The following describes data read through the read byte;

Bit 7 (POR) is the power-on reset indicator, and this is set to a logic '1' if the V_{cc} supply to the device has dropped below 3 V (at 25°C), e.g., when the device is initially turned ON. The POR is reset to '0' when the read sequence is terminated by a STOP command. When POR is set high this indicates that the programmed information may have been corrupted and the device reset to power up condition.

Bit 6 (FL**)** is the PLL lock flag and indicates whether the device is phase locked, a logic '1' is present if the device is locked, and a logic '0' if the device is unlocked. The FL bit is set after 64 consecutive comparison cycles in lock.

Bit 3 (AGF) is the AGC detector flag and indicates whether the AGC detector is active.

Table 21 - AGC Activity Flag Settings

AGF	AGC Activity Flag
0	AGC active, V_{AGC} < 4 V External RF LNA gain is reduced
1	AGC not active, V_{AGC} >4 V External RF LNA gain is at maximum

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Bits 2:0 (V2:V0) contain the ADC output data. The ADC output is sampled on the ACK clock of the read address byte.

Table 22 - ADC Output Values

Input Level (V)	V2	V1	V0
< 0.32 Vcc	0	0	0
0.32Vcc to 0.48Vcc	0	0	1
0.48Vcc to 0.64Vcc	0	1	0
0.64Vcc to 0.80Vcc	0	1	1
> 0.80Vcc	1	0	0

3.0　Applications Information

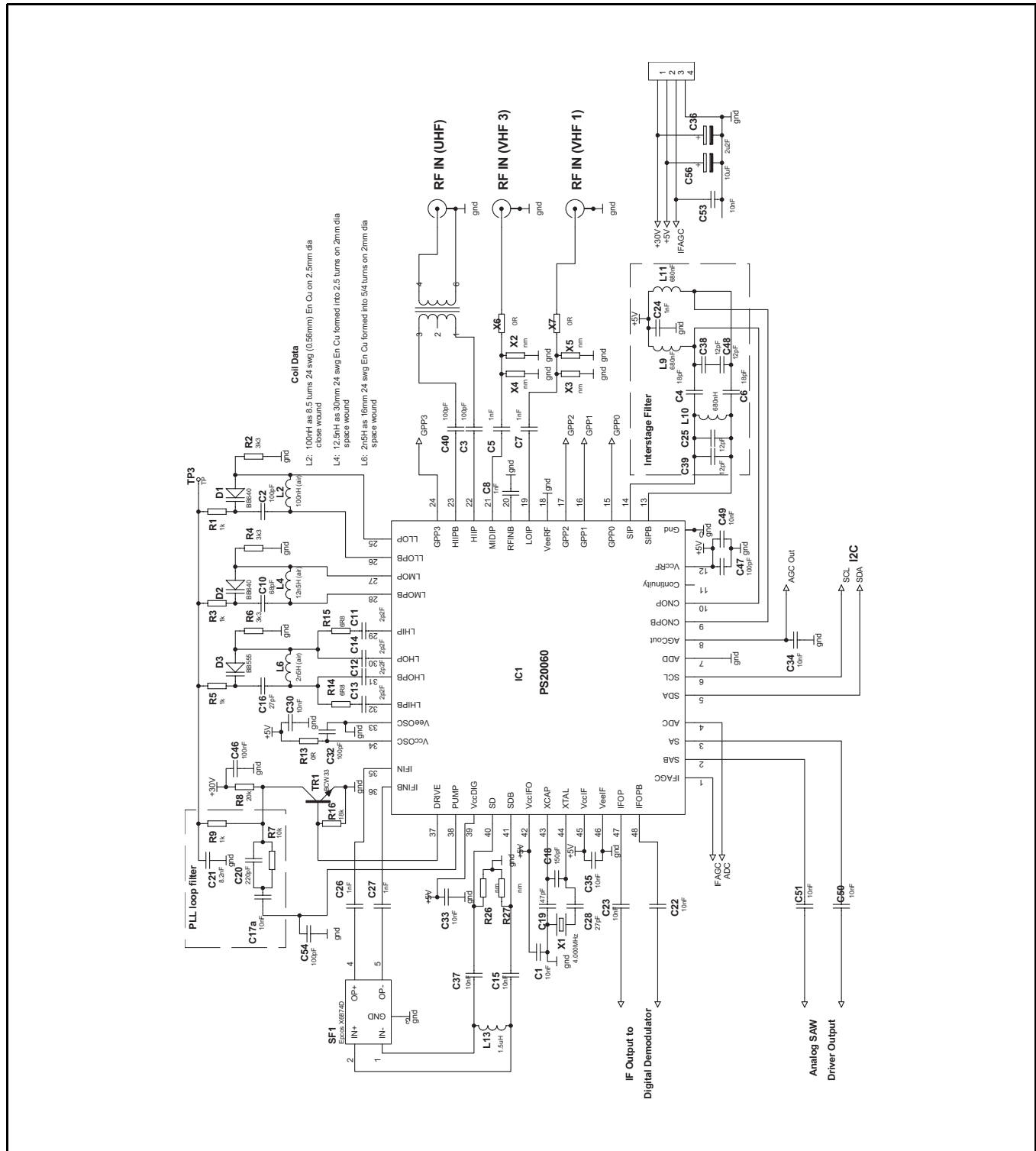Typical application circuits are shown for the PS20060 in the following diagrams.

Figure 8 - Typical Application Circuit (DVB-T)
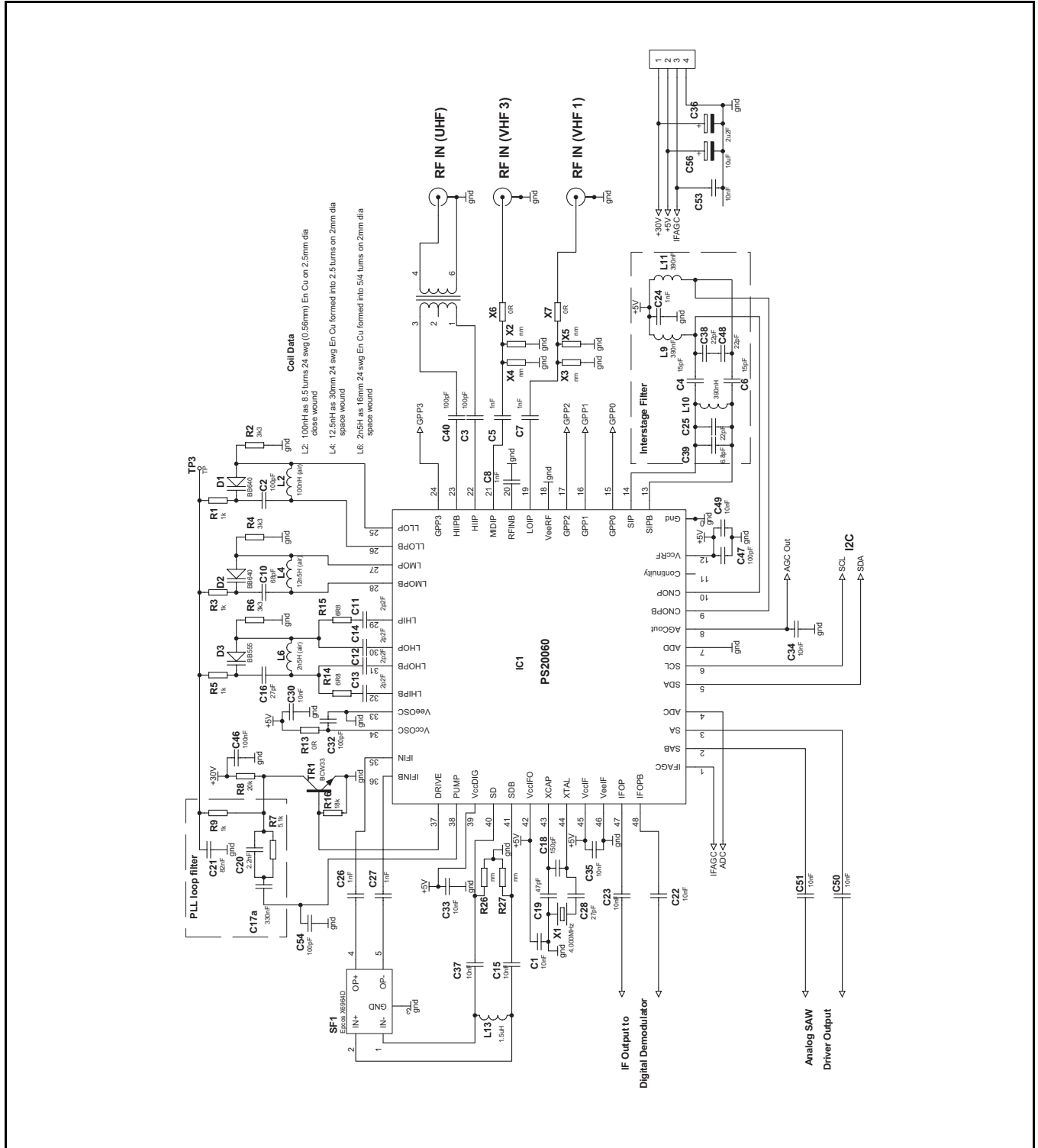
Figure 9 - Typical Application Circuit (ATSC)

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The low (VHF1) and Mid (VHF3) bands are single ended however the high band (UHF) should be differential. All IF signals are differential.

It is essential to have good RF layout around the RF stages, i.e., RF inputs and the VCOs. Track lengths around the VCO's should be minimized to reduce track inductance.

The layout should be organized to give good isolation between the IF signal paths. In particular good isolation is required between the outputs and inputs of the IF AGC amplifier. Isolation across the SAW filter is also important to ensure rejection of unwanted adjacent signals. This can be achieved by routing input and output tracks on opposite sides of the board.

It is also important to have good isolation between the high level IF signal and the crystal oscillator circuit to minimize any interactions. Care should be taken when locating IF tuning inductors to ensure there is no radiation to other parts of the circuit.

The crystal oscillator can also provide a clock signal to the demodulator. This can be done by taking the oscillator signal from the crystal series capacitor (27 pF) as shown in the following diagram.
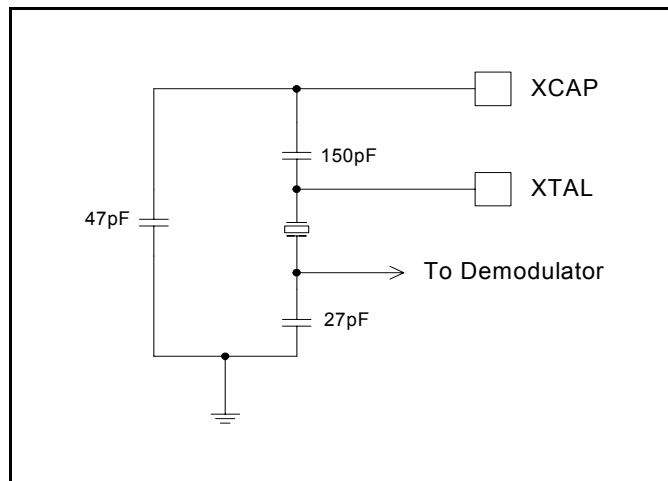

Figure 10 - Crystal Oscillator Circuit (4 MHz)

The interstage filter between the converter outputs provides some rejection of adjacent channels (N +/- 2).The recommended values are shown in Figure 11. The choice of components is important not only to give a flat response but also to provide an impedance transformation.

The specified noise figure for the low and mid bands assumes that there will be a network before the device to provide image rejection. In a tuner this would be part of the input tracking filters but for test purposes a network is shown in Figure 12.

Type	IF	0.5 dB BW	Component values						
	MHz	MHz	R_{source}	R_{term}	L1	L2	C1	Cc	C2
0.5 dB Chebychev	36	10	500	250	680	680	12	18	12
0.5 dB Chebychev	44	10	500	250	390	390	22	15	7.5
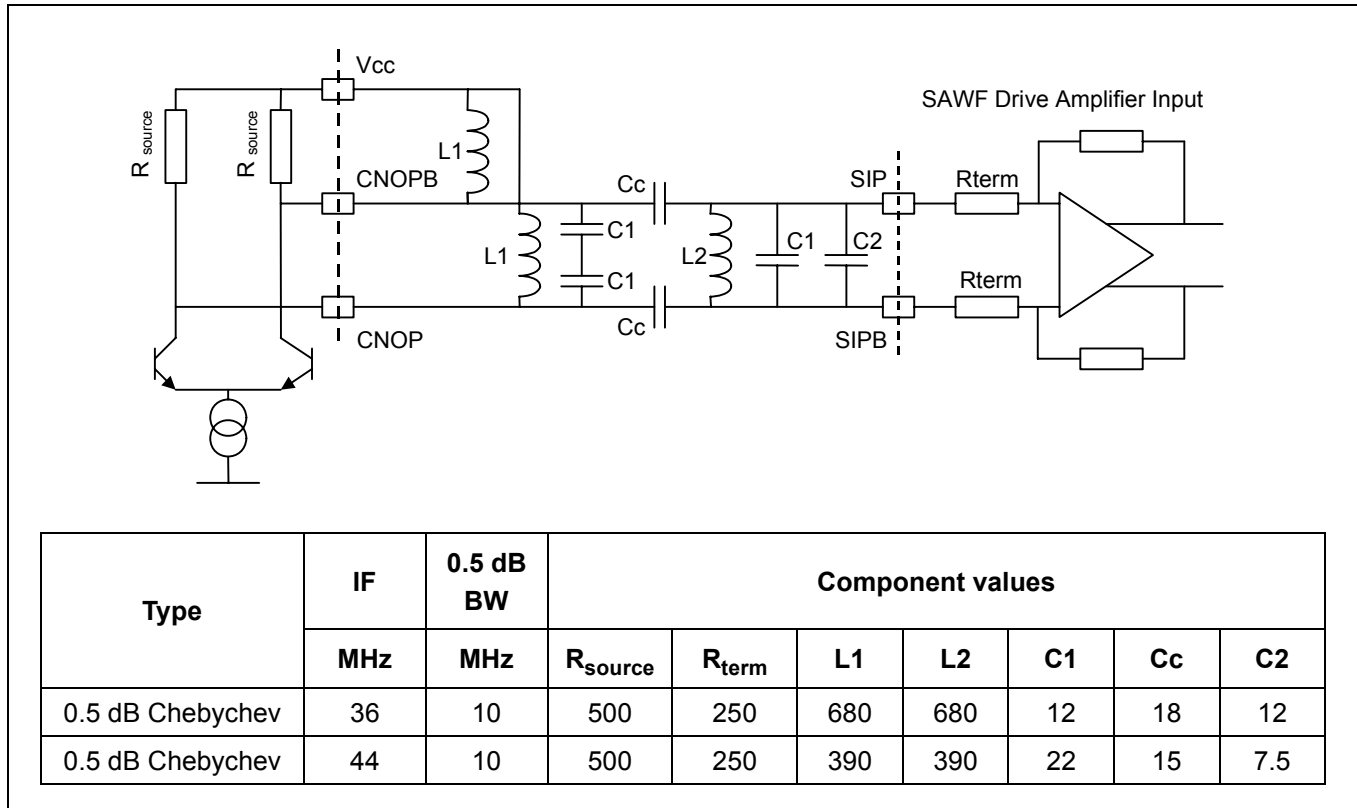
Figure 11 - Interstage Filter
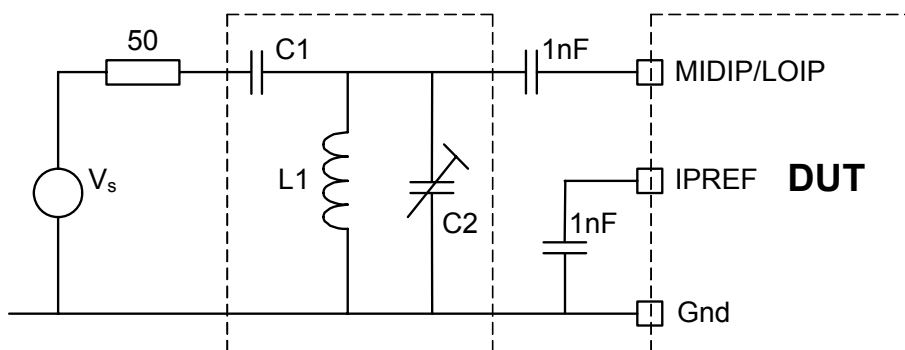
Band	Frequency		C1	L1	C2
	LO	RF IN			
	MHz	MHz	pF	nH	pF
LOW	90	46	20	299	20
LOW	200	156	8	65	8
MID	240	196	8	41	8
MID	500	446	2.1	21	4

Figure 12 - Noise Figure Measurement Conditions

The optimum charge pump and LO trim settings for the application circuits shown in Figure 8,9 are shown in the table below. These give the optimum phase noise performance for the circuit shown. The changes in charge pump current compensate for frequency and VCO gain variations.

Table 23 - Optimum CP and LO Trim Settings

Frequency Range	Charge Pump Setting CP	LO Trim LO1
VHF1 50 -110 MHz	01	1
VHF1 100 -160 MHz	10	1
VHF3 160 - 250 MHz	10	1
VHF3 250 - 350 MHz	01	1
VHF3 350 - 450 MHz	10	0
UHF 450 - 500 MHz	00	1
UHF 500 - 700 MHz	01	1
UHF 700 - 800 MHz	10	1
UHF 800 - 850 MHz	11	1
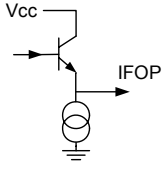
4.0   PIn Circuit Information

Pin No.	Pin Name	Port Sense	Function	Schematic
1	IFAGC	Input	IF AGC control	
2, 3	SAB, SA	Output, Output	SAW filter driver output A inverse SAW filter driver output A	
4	ADC	Input	ADC input	
5	SDA	Bi-directional	I^2C bus serial data input/output	
6	SCL	Input	I^2C bus serial clock input	

Pin No.	Pin Name	Port Sense	Function	Schematic
7	ADD	Input	I^2C address select	
8	AGCOP	Output	AGC output	
9, 10	CNOPB, CNOP	Output, Output	Converter Output inverse Converter Output	
11	Cont	-	Paddle	-
12	VccRF	Supply	RF section supply	-
13, 14	SIPB SIP	Input, Input	SAW filter driver input inverse, SAW filter driver input	
15	GPP0	Output	Switching port/Test output 1	

Pin No.	Pin Name	Port Sense	Function	Schematic
16	GPP1	Output	Switching port/Test output 2	
17	GPP2	Output	Switching port	As GPP1 (pin16)
18	VeeRF	Supply	RF section ground	-
19, 20, 21	LOIP IPREF MIDIP	Input, Input, Input	Low band input, Mid- and Low-band i/p reference, Mid-band input	
22, 23	HIIP, HIIPB	Input, Input	Hi-band input, Hi-band input inverse	
24	GPP3	Output	Switching Port	As GPP1 (pin16)
25, 26	LLOP, LLOPB	Output	Low band oscillator output, Low-band oscillator output inverse	
27, 28	LMOP, LMOPB	Output, Output	Mid-band oscillator output, Mid-band oscillator output inverse	

Pin No.	Pin Name	Port Sense	Function	Schematic
29, 30, 31, 32	LHIP, LHOP, LHOPB, LHIPB	Input, Output, Output, Input	High band oscillator input, High-band oscillator output, High-band oscillator output inverse, High-band oscillator input inverse	
33	VeeOSC	Supply	LO ground	-
34	VccOSC	Supply	LO supply	-
35, 36	IFIP, IFIPB	Input, Input	IF AGC amp input, IF AGC amp input inverse	
37, 38	DRIVE, PUMP	Output, Output	Loop amplifier drive output, Loop amp charge pump output	
39	VccDIG	Supply	Digital section supply	-
40, 41	SD, SDB	Output, Output	SAW filter driver output D, SAW filter driver o/p D inverse	
42	VccIF	Supply	SAWF output supply	-
43	XCAP	Input	Reference osc feedback input	
44	XTAL	Output	Reference osc crystal drive	See XCAP (pin 43)

Pin No.	Pin Name	Port Sense	Function	Schematic
45	VccIF	Supply	IF AGC supply	-
46	VeeIF	Supply	IF AGC ground	-
47, 48	IFOP, IFOPB	Output, Output	IF AGC amp output, IF AGC amp inverse output	
Paddle	Vee	-	-	-

5.0   Absolute Maximum Ratings

All voltages are referred to V_{ee} at 0 V.

Characteristic	Min.	Max.	Units	Conditions
Supply voltage	-0.3	6	V	
Supply voltage differential		0.4	V	Note 1
RF input voltage		117	dBμV	
Maximum voltage on SDA, SCL		5.5	V	V_{cc} = 0 to 5.5V
Max voltage on all remaining signal pins	-0.3	V_{cc}+0.3	V	The voltage on any pin must not exceed 6 V
Total port current		20	mA	
Storage temperature	-55	150	^{o}C	
Junction temperature		125	^{o}C	Power applied
Package thermal resistance (chip to ambient)		27	^{o}C/W	Package paddle soldered to ground
ESD protection	2.0		kV	All pins except 9,10
Mil-std 883B method 3015 cat1	1.25		kV	Pins 9, 10 only

Note 1:   The V_{CCOSC}, V_{CCDIG} (Pins 39,42) can be operated at a lower supply voltage than the remaining V_{CC} pins, but the voltage differential must not exceed the figure quoted in the table above.

6.0   Operating Range

All voltages are referred to V_{ee} at 0 V.

Characteristic	Min.	Max.	Units.	Conditions
Supply voltage	4.5	5.5	V	Functional operation, specification not guaranteed
Supply voltage (V_{CCRF} and V_{CCIF})	4.75	5.25	V	Full specification
Supply voltage (V_{CCDIG} and V_{CCOSC})	4.60	5.25	V	
Ambient Temperature	-20	85	^{o}C	
Low Band Input Frequency	50	170	MHz	
Mid Band Input Frequency	140	460	MHz	
High Band Input Frequency	400	900	MHz	

7.0 Electrical Characteristics

Test conditions (unless otherwise stated). T = 25°C, V_{ee}= 0 V, V_{cc} = 5 V, IF Frequency = 36 MHz. All signals are differential with the exception of VHF1 and VHF3 inputs.

Characteristic	Min.	Typ.	Max.	Units	Conditions
Supply current					
Normal operation		117	140	mA	Total Current – UHF band All switching ports off
All sections active		110	134	mA	Total Current - VHF Bands All switching ports off
All sections active except AGC IF amplifier		92		mA	UHF Band. Switching ports off
		85		mA	VHF Bands. Switching ports off
Sleep Mode		9		mA	Crystal oscillator and data interface enabled
		33		mA	PLL and crystal oscillator enabled
Composite system to SAW Filter driver outputs **VHF1 Band**					
Conversion gain	29	32	35	dB	RFin = 54 MHz. Single ended input
Conversion gain	29	32	35	dB	RFin = 155 MHz. Single ended input
Noise Figure		9	11	dB	Rs = 50 Ω, SSB with input matching network. See Figure 12.
OPIP3	135	146		dBµV	Two output tones at 110 dBµV
Output level causing 1% cross modulation	113	120		dBµV	Note 2
Output level causing 1.5 kHz FM	113	120		dBµV	Note 3
I^{2}C bus transmission induced LO frequency modulation		2.5		kHz	Transmission repetition rate of 20 msec minimum with no change to previously loaded data, at 100 kHz SCL rate
N+5 Direct modulation of VCO			-40	dBc	Local oscillator sidebands induced by an input carrier at 80 dBµV offset from local oscillator by 100 kHz
Supply ripple spurious			-40	dBc	Residual FM induced on local oscillator by 20 mV$_{p-p}$ ripple on V$_{cc}$ at 500 kHz
Local oscillator leakage to any band input		30		dBµV	

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Characteristic	Min.	Typ.	Max.	Units	Conditions
IPIP2	134	143		dBμV	Two input tones at 87 dBμV at 90 MHz and 66 MHz with local oscillator at 114 MHz
IPIP3	112	120		dBμV	Desired = 54 MHz at 45 dBμV Undesired = 60 and 72 MHz at 87 dBμV
IPIP3	112	119		dBμV	Desired = 155 MHz at 45 dBμV Undesired = 161 and 173 MHz at 87 dBμV
P1dB	93	106		dBμV	
Output Impedance		100		Ω	
		10		nH	
Phase Noise, SSB					PLL Loop Bandwidth ~ 3 kHz f_{comp} = 166.7 kHz
1 kHz		-90	-70	dBc/Hz	
10 kHz		-95	-86	dBc/Hz	
100 kHz		-115	-106	dBc/Hz	
10 MHz			-135	dBc/Hz	Noise Floor
Reference spurs		-90	-50	dBc	
Phase Noise, SSB					PLL Loop Bandwidth ~ 300 Hz f_{comp} = 62.5 kHz
10 kHz		-100	-86	dBc/Hz	
100 kHz		-115	-106	dBc/Hz	
Composite system to SAW Filter driver outputs VHF3 Band					
Conversion gain	29	32	35	dB	RFin = 164 MHz Single ended input
Conversion gain	29	32	35	dB	RFin = 442 MHz Single ended input
Noise Figure		9	11	dB	Rs = 50 Ω, SSB with input matching network. See Figure 12.
OPIP3	135	146		dBμV	Two output tones at 110 dBμV
Output level causing 1% cross modulation	113	120		dBμV	Note 2
Output level causing 1.5 kHz FM	113	120		dBμV	Note 3
I^2C bus transmission induced LO frequency modulation		2.5		kHz	Transmission repetition rate of 20 msec minimum with no change to previously loaded data, at 100 kHz SCL rate

Characteristic	Min.	Typ.	Max.	Units	Conditions
N+5 Direct modulation of VCO		-	-40	dBc	Local oscillator sidebands induced by an input signal at 80 dBμV offset from local oscillator by 100 kHz.
Supply ripple spurious			-40	dBc	Residual FM induced on local oscillator by 20 mV$_{p-p}$ ripple on V$_{cc}$ at 500 kHz
Local oscillator leakage to any band input		30		dBμV	
IPIP2	134	143		dBμV	Two input tones at 89 dBμV at 198 MHz and 398 MHz with local oscillator at 240 MHz
IPIP3	112	122		dBμV	Desired = 165 MHz at 45 dBμV Undesired = 171 and 183 MHz at 89 dBμV
IPIP3	112	119		dBμV	Desired = 438 MHz at 45 dBμV Undesired = 444 and 456 MHz at 89 dBμV
P1dB	-95	107		dBμV	
Output Impedance		100		Ω	
		10		nH	
Phase Noise, SSB					PLL Loop Bandwidth ~ 3 kHz f$_{comp}$ = 166.7 kHz
1 kHz		-87	-70	dBc/Hz	
10 kHz		-92	-86	dBc/Hz	
100 kHz		-114	-106	dBc/Hz	
10 MHz			-135	dBc/Hz	Noise Floor
Reference spurs		-90	-50	dBc	
Phase Noise, SSB					PLL Loop Bandwidth ~ 300 Hz f$_{comp}$ = 62.5 kHz
10 kHz		-95	-86	dBc/Hz	
100 kHz		-115	-106	dBc/Hz	
Composite system to SAW Filter driver outputs UHF Band					
Conversion gain	35	38	41	dB	RFin = 450 MHz
Conversion gain	35	38	41	dB	RFin = 866 MHz
Noise Figure		6	8	dB	Rs = 50 Ω, No image correction
OPIP3	135	146		dBμV	Two output tones at 110 dBμV

Characteristic	Min.	Typ.	Max.	Units	Conditions
Output level causing 1% cross modulation	113	120		dBμV	Note 2
Output level causing 1.5 kHz FM	113	120		dBμV	Note 3
I^{2}C bus transmission induced LO frequency modulation		2.5		kHz	Transmission repetition rate of 20 msec minimum with no change to previously loaded data, at 100 kHz SCL rate
N+5 Direct modulation of VCO			-30	dBc	Local oscillator sidebands induced by an input 750 MHz carrier at 80 dBμV offset from local oscillator by 100 kHz
Supply ripple spurious			-40	dBc	Residual FM induced on local oscillator by 20 mV$_{p-p}$ ripple on V$_{cc}$ at 500 kHz
Local oscillator leakage to any band input		60		dBμV	
IPIP2	125	159		dBμV	Two input tones at 89 dBμV at 198 MHz and 398 MHz with local oscillator at 240 MHz
IPIP3	108	115		dBμV	Desired = 438 MHz at 45 dBμV Undesired = 444 and 456 MHz at 85 dBμV
IPIP3	108	112		dBμV	Desired = 858 MHz at 45 dBμV Undesired = 864 and 876 MHz at 85 dBμV
P1dB	91	99		dBμV	
Output Impedance		100		Ω	
		10		nH	
Phase Noise, SSB					PLL Loop Bandwidth ~ 3 kHz f$_{comp}$ = 166.7 kHz
1 kHz		-78	-70	dBc/Hz	
10 kHz		-89	-84	dBc/Hz	
100 kHz		-113	-106	dBc/Hz	
10 MHz			-135	dBc/Hz	Noise Floor
Reference spurs		-80	-50	dBc	
Phase Noise, SSB					PLL Loop Bandwidth ~ 300 Hz f$_{comp}$ = 62.5 kHz
10 kHz		-92	-86	dBc/Hz	
100 kHz		-113	-106	dBc/Hz	

Characteristic	Min.	Typ.	Max.	Units	Conditions
AGC Detector and ADC					
Operating frequency range	16		72	MHz	
AGC Threshold Level		120		dBμV	AT[2:0] = 0
ADC leakage current			60	nA	V_{ADC} = 4.0 V
	-60			nA	V_{ADC} = 0.5V
AGC source current	6.8	10	13.3	μA	See Table 15
	0.25	0.35	0.45	μA	
AGC sink current	-65	-100	-145	μA	AGC attack current, triggered by detected level exceeding AGC attack point
AGC sink current 90% rise and fall time		1		μsec	
AGC input level response			1	dB	Change in input level for AGC sink current to change from high impedance to 90% of maximum value, with AGC operative
AGCOP output impedance	20			MΩ	AGC inactive
AGCOP output voltage range			0.5	V	Minimum gain required
	4			V	Maximum gain required
External AGC voltage	0.5		V_{cc} - 0.4	V	Maximum external voltage range which can be applied to AGCOP when disabled
AGCOP leakage current	-50		50	nA	Over normal operating range
ADC step size, LSB		0.16 x V_{cc}		V	See Table 22
ADC step size accuracy			0.01 x V_{cc}	V	See Table 22
AGCout_flag High threshold	V_{cc} - 0.66			V	AGF flag set to 1
AGCout_flag Low threshold			V_{cc} -0.76		AGF flag set to 0
IF amplifier					
Supply Current		25		mA	
Frequency range	16		72	MHz	
Input impedance	1.5	2	2.8	kΩ	
			1.5	pF	

Characteristic	Min.	Typ.	Max.	Units	Conditions
Gain (Voltage conversion gain, differential source to maximum load)	60	66		dB	V_{IFAGC} = 3.0 V
		17	22	dB	V_{IFAGC} = 0.5 V
Noise Figure		6.3	8.5		Rs=50 Ω
Gain control range	41	48		dB	See figure 4
Gain control slope	25	31	38	dB/V	$1.2{\leq}V_{AGC}{\leq}2.2$
Gain variation with temperature T = -20°C to 85°C	-1		+1	dB	V_{AGC} = 1.2V and 2.2V
Gain slope variation with temperature T = -20°C to 85°C	-1		+1	dB/V	V_{AGC} = 1.2V to 2.2V
Gain variation within channel			0.25	dB	Channel bandwidth 8 MHz within operating frequency range, with maximum load as defined below
OPIP3	130	141		dBμV	Two output tones at 109 dBμV within output channel Gain range = 21 dB to maximum
AGC input current			50	μA	
Output impedance			120	Ω	
Maximum load condition			4.7	kΩ	Differential load
			15	pF	
I^{2}C BUS SDA SCL					
Input high voltage	2.55		5.5	V	
Input low voltage	0		1.4	V	
Input current High			10	μA	V_{in}=5.5 V, V_{cc}=5.25 V
			10	μA	V_{in}=5.5 V, V_{cc}=0 V
Input Current Low	-10			μA	V_{in}= 0 V, V_{cc}=5.25 V
Hysteresis		0.4		V	
SDA output voltage			0.4	V	I_{sink}=3 mA
			0.6	V	I_{sink}=6 mA
SCL clock rate			400	kHz	
ADD (address) select					See Table 4
Input high current			1	mA	V_{in}=V_{ccD}

Characteristic	Min.	Typ.	Max.	Units	Conditions
Input low current			-0.5	mA	$V_{in}=V_{ee}$
PLL Synthesizer					
Charge pump output current					See Table 8 V_{PUMP}=2 V
Charge pump output leakage		+-3	±10	nA	Note 4
Charge pump drive output current	0.5			mA	V_{DRIVE}=0.7 V
Crystal frequency	4		16	MHz	Application as in Figure 10 with 4 MHz crystal
Recommended crystal series ESR	25	70	150	Ω	4 MHz parallel resonant crystal
External reference input frequency	4		20	MHz	Sine wave coupled through 10 nF capacitor
External reference drive level	0.2		2	V_{pp}	Sine wave coupled through 10nF capacitor
		0.5		V_{pp}	Recommended level for optimum phase noise at 4 MHz
Phase detector comparison frequency	31.25		250	kHz	
RF division ratio	240		32767		
Switching ports GPP3-GPP0					
Sink current	10			mA	V_{port} = 0.4
Pull up resistor GPP3- GPP1		10		kΩ	
Leakage current			10	μA	V_{port} = $V_{cc,}$ Port P0 only

Note 1:   0 dBm =107 dBμV. All input levels are specified as voltage that would be present if input signal generator was terminated in 50 ohms

Note 2:   Wanted signal (picture carrier) = 101 dBmV at output. Undesired signal (sound carrier) at 5.25 MHz offset modulated with 1 kHz 80% AM. Increase undesired signal to give 1% AM on wanted signal.

Note 3:   Wanted signal at 101 dBmV. Unwanted signal at 5.25 MHz offset modulated with 1 kHz 50% AM. Increase undesired signal to give 1.5 kHz FM on wanted signal

Note 4:   Current into PUMP pin with 20 μA current from DRIVE pin

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