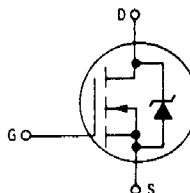
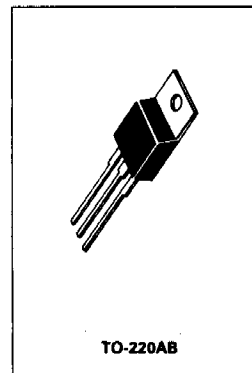


**Designer's Data Sheet**  
**TMOS IV**  
**Power Field Effect Transistor**  
**N-Channel Enhancement-Mode Silicon Gate**

**MTP20N10E**

**TMOS POWER FET**  
**20 AMPERES**  
 **$r_{DS(on)} \approx 0.15 \text{ OHM}$**   
**100 VOLTS**

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.



- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	100	Vdc
Drain-Gate Voltage ( $R_{GS} = 1 \text{ M}\Omega$ )	$V_{DGR}$	100	Vdc
Gate-Source Voltage — Continuous	$V_{GS}$	$\pm 20$	Vdc
— Non-repetitive ( $t_p < 50 \mu s$ )	$V_{GSM}$	$\pm 40$	Vpk
Drain Current — Continuous	$I_D$	20	Adc
— Pulsed	$I_{DM}$	60	Adc
Total Power Dissipation ( $\theta_{TC} = 25^\circ C$ ) Derate above 25°C	$P_D$	100 0.67	Watts W/°C
Operating and Storage Temperature Range	$T_J, T_{stg}$	-65 to 175	°C

**UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS ( $T_J \leq 175^\circ C$ )**

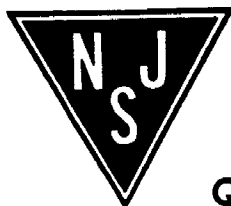
Single Pulse Drain-to-Source Avalanche Energy	$W_{DSS} (1)$	400	mJ
Repetitive Pulse Drain-to-Source Avalanche Energy	$W_{DSS} (2)$	100	
	$W_{DSR} (3)$	10	

**THERMAL CHARACTERISTICS**

Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.5	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	$T_L$	275	°C

(1)  $V_{DD} = 25 \text{ V}, I_D = 20 \text{ A}, L = 1.5 \text{ mH}$ , Initial  $T_C = 25^\circ C$   
(2)  $V_{DD} = 25 \text{ V}, I_D = 20 \text{ A}, L = 380 \mu H$ , Initial  $T_C = 100^\circ C$   
(3)  $f = 10 \text{ kHz}$

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design. TMOS and Designer's are trademarks of Motorola Inc.



MTP20N10E

ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
----------------	--------	-----	-----	------

OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ( $V_{GS} = 0, I_D = 0.25 \text{ mA}$ )	$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0$ ) ( $V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0, T_J = 125^\circ\text{C}$ )	$I_{DSS}$	—	10 80	$\mu\text{A}$
Gate-Body Leakage Current, Forward ( $V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$ )	$I_{GSSF}$	—	100	nAdc
Gate-Body Leakage Current, Reverse ( $V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$ )	$I_{GSSR}$	—	100	nAdc

ON CHARACTERISTICS\*

Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 1 \text{ mA}$ ) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance ( $V_{GS} = 10 \text{ Vdc}, I_D = 10 \text{ Adc}$ )	$r_{DS(on)}$	—	0.15	Ohm
Drain-Source On-Voltage ( $V_{GS} = 10 \text{ V}$ ) ( $I_D = 20 \text{ Adc}$ ) ( $I_D = 10 \text{ Adc}, T_J = 100^\circ\text{C}$ )	$V_{DS(on)}$	—	3.6 3	Vdc
Forward Transconductance ( $V_{DS} = 15 \text{ V}, I_D = 10 \text{ A}$ )	$g_{FS}$	6	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	( $V_{DS} = 25 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$ ) See Figure 16	$C_{iss}$	—	1600	pF
Output Capacitance		$C_{oss}$	—	600	
Reverse Transfer Capacitance		$C_{rss}$	—	200	

SWITCHING CHARACTERISTICS\* ( $T_J = 100^\circ\text{C}$ )

Turn-On Delay Time	( $V_{DD} = 25 \text{ V}, I_D = 0.5 \text{ Rated } I_D$ $R_{gen} = 50 \text{ ohms}$ ) See Figure 9	$t_{d(on)}$	—	50	ns
Rise Time		$t_r$	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		$t_f$	—	200	
Total Gate Charge	( $V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $I_D = \text{Rated } I_D, V_{GS} = 10 \text{ V}$ ) See Figures 17 and 18	$Q_g$	28 (Typ)	50	nC
Gate-Source Charge		$Q_{gs}$	15 (Typ)	—	
Gate-Drain Charge		$Q_{gd}$	13 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS\*

Forward On-Voltage	( $I_S = \text{Rated } I_D$ $V_{GS} = 0$ )	$V_{SD}$	1.4 (Typ)	1.9	Vdc
Forward Turn-On Time		$t_{on}$	Limited by stray inductance		
Reverse Recovery Time		$t_{rr}$	300 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	$L_d$	3.5 (Typ) 4.5 (Typ)	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	$L_s$	7.5 (Typ)	—	

\*Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

