

## SANYO Semiconductors DATA SHEET

# LA7137M — Monolithic Linear IC DVD Analog Video Output I/F IC

#### Overview

The LA7137M is a video output interface IC for DVD players and is optimal as the driver IC for DVD players that provide composite signal/S signal, component signal, and RGB signal video outputs.

Since this IC integrates a Y/C mixer on the same chip, the D/A converter composite output can be omitted. The LA7137M also integrates S1 and S2 DC voltage and D/A converter reference voltage generation on chip, allowing most components other than the drivers to be omitted.

#### **Functions**

• Clamps

• Y/C mixer

• Amplifier

• S1 and S2 DC output

75Ω driver

• D/A converter reference voltage output

#### **Features**

• Video signal-to-noise ratio : -80dB

• Frequency characteristics : flat to 10MHz

- Y/C time difference : less than 2ns
- Signal dynamic range: 170IRE.
- Can support all major signal types: composite/S signals, component signals, and baseband (RGB) signals. Furthermore, the IC input type can be switched by the system microcontroller (since the input capacitors are shared).
- $\bullet$  Two 75 $\Omega$  driver systems that can be independently muted by the system microcontroller.
- The clamp pulses required for component signal input are generated internally in the IC.
- Either of two amplifier gain levels, 8.5 and 6dB, can be selected.
- A built-in regulator circuit provides a stable DC voltage output that is independent of V<sub>CC</sub> fluctuations.

#### **Specifications**

#### **Maximum Ratings** at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>CC</sub> max		10.0	V
Allowable power dissipation	Pd max	Ta ≤ 75°C * Mounted on a board	525	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-40 to +150	°C

<sup>\*</sup> Only when mounted on a 114.3×76.1×1.6mm³ glass epoxy board

- A. and all SANYO Semiconductor products described or contained herein do not have specifications that c. handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO Semiconductor representative nearest you before using any SANYO Semiconductor products described or contained herein in such applications.
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## Operating Conditions at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	VCC		8.0	٧
Operating supply voltage range	V <sub>CC</sub> op		7.6 to 8.4	V

## **Electrical Characteristics** at Ta = 25°C, $V_{CC} = 7.6$ to 8.4V

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Parameter	Symbol	Input signal	Test point	Conditions	min	Ratings typ	may	Unit
Current drain 1	I <sub>CC</sub> 1	oignai	point	Video system current drain	14.3	17.9	max 21.5	mA
Current drain 2	ICC2			75Ω driver current drain ; no signal	14.4	18.0	21.6	mA
(A) For a pin 10 (Y signal) ii		omnosite/S	selected	7 OSZ GITVOT COTTOTIC GRAINT, NO SIGNAL	14.7	10.0	21.0	46.
Amplifier gain (low)	G <sub>Y</sub> M	Sig.1	T13/15	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G <sub>Y</sub> H	Sig.1	T13/15	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Clamp voltage	C <sub>10</sub> H	Sig.1	T10	The T10 sync tip potential for a 761mVp-p	3.85	4.20	4.55	V
Clamp voltage	01011	Olg. I	110	input	3.00	4.20	4.55	V
(B) For a pin 6 (chrominanc	e signal) inr	l out when co	mnosite/S s				-//-	
Amplifier gain (low)	G <sub>C</sub> M	Sig.2	T17/19	The gain for a 711mVp-p 3.58MHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G <sub>C</sub> H	Sig.2	T17/19	The gain for a 544mVp-p 3.58MHz signal	7.38	7,6	7.81	dB
Chrominance signal input	D <sub>6</sub> H	Sig.2	T6	The T6 offset voltage for a 544mVp-p	4.4	4.75	5.1	V
DC voltage	2611	Olg.2	10	input	4.4	/	0.1	v
(C) For a pin 3 (composite s	ignal) input	when com	oosite selec	ted				
Amplifier gain (low)	G <sub>S</sub> M1	Sig.3	T21/23	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G <sub>S</sub> H1	Sig.3	T21/23	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Clamp voltage	C <sub>3</sub> H	Sig.3	T3	The T3 sync tip potential for a 761mVp-p	4.0	4.35	4.7	V
Ciamp rollage	3	O.g.o		input				·
(D) For a pins 6 and 10 (S s	ignal) input	when S is s	selected					
Amplifier gain (low)	G <sub>S</sub> M2	Sig.1	T21/23	The gain for a 996mVp-p 100kHz signal or	4.92	5.27	5.61	dB
p g ()	-3=	Sig.2		a 711mVpp 3.58kHz signal				-
Amplifier gain (high)	G <sub>S</sub> H2	Sig.1	T21/23	The gain for a 761mVp-p 100kHz signal or	7.25	7.6	7.94	dB
		Sig.2		a 544mVpp 3.58kHz signal				
(E) The gain ratios between	the differer	nt signals w	hen compos	site is selected	I.			
Y/chrominance amplifier	ΔYC	Sig.1	T13/15	The ratio of the G <sub>Y</sub> H gain for (A) and the	-3	0	3	%
gain ratio		Sig.2	T17/19	G <sub>C</sub> H gain for (B)				
Y/composite amplifier	ΔY <sub>S</sub> 1	Sig.1	T13/15	The ratio of the GYH gain for (A) and the	-3	0	3	%
gain ratio		Sig.3	T21/23	G <sub>S</sub> H1 gain for (C)				
Chrominance/composite	ΔC <sub>S</sub> 1	Sig.2	T17/19	The ratio of the G <sub>C</sub> H gain for (B) and the	-3	0	3	%
amplifier gain ratio		Sig.3	T21/23	G <sub>S</sub> H1 gain for (C)				
(F) The gain ratios between		nt signals wh	hen S is sel	ected				
Y/S amplifier gain ratio	ΔY <sub>S</sub> 2	Sig.1	T13/15	The ratio of the G <sub>Y</sub> H gain for (A) and the	-4.5	0	4.5	%
		Sig.2	T21/23	GgH2 gain for (D)				
Chrominance/S amplifier	∆C <sub>S</sub> 2	Sig.1	T17/19	The ratio of the G <sub>C</sub> H gain for (B) and the	-4.5	0	4.5	%
gain ratio		Sig.2	T21/23	G <sub>S</sub> H2 gain for (D)				
(G) The pin 10 (Y signal) in	put when co	mponent is	_//		ı	1		
Amplifier gain (low)	G <sub>Y</sub> M	Sig.1	T13/15	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G <sub>Y</sub> H	Sig.1	T13/15	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Y input clamp voltage	C <sub>10</sub> H	Sig.1	T10	The T10 sync tip potential for a 761mVp-p input	3.85	4.20	4.55	V
(H) The pin 6 (B-Y or R-Y s	ignal) input	when comp	onent is sal		l			1
Amplifier gain (low)	G <sub>N</sub> M	Sig.4	T17/19	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Amplifier gain (high)	G <sub>N</sub> H	Sig.4	T17/19	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
	P <sub>6</sub> H		T6		4.4	4.75	5.1	V
Input pedestal clamp voltage		Sig.4	10	The T6 pedestal potential for a 761 mVp-p input	4.4	4.70	ა. 1	v
Amplifier gain (low)	G <sub>N</sub> M	Sig.4	T21/23	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
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(1) The pin 3 (8-V or R-V signal in policy in components is selected	Parameter	Symbol	Input	Test	Conditions		Ratings		Unit
Amplifier gain (high)   GNH   Sig.4   T3   T3   The gain for a 761 mVp-p 1004 to signal   7.38   7.6   7.81   of 5   V violating   GNH   Sig.4   T3   The T3 possestip chemical for a 761 mVp-p   4.4   4.75   5.1   V violating   GNH   Sig.4   T3   T3   The T3 possestip chemical for a 761 mVp-p   4.4   4.75   5.1   V violating   GNH   Sig.4   T3   T3   The T3 possestip chemical for a 761 mVp-p   4.4   4.75   5.1   V violating   GNH   Sig.4   T3   T3   T3   The T3 possestip chemical for a 761 mVp-p   3.3   0   3   M violating   GNH   Sig.4   T3   T3   T3   The T3 to of the GNH gain for (E) and the GNH gain for (S)   GNH   T3   T3   The T3 to of the GNH gain for (E) and the GNH gain for (S)   GNH   T3   T3   T3   The T3 to of the GNH gain for (F) and the GNH gain for (S)   GNH   T3   T3   T3   The T3 to of the GNH gain for (F) and the GNH gain for (S)   GNH   T3   T3   T3   T3   T3   T3   T3   T	Parameter	Symbol	signal	point	Conditions	min	typ	max	Unit
Input pedestatic clamp	(I) The pin 3 (B-Y or R-Y sig	nal) input w	hen compo	nent is sele	cted				
Voltage   Imput   Im	Amplifier gain (high)	G <sub>N</sub> H	Sig.4	T21/23	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Yeomponent amplifier   ΔY1   Sig1   T13/15   The ratio of the GyH gain for (E) and the   3   0   3   % (spin ratio 1)   Sig4   T17/19   GyH gain for (F) and the   3   0   3   % (spin ratio 2)   Sig4   T17/19   GyH gain for (F) and the   5   0   3   % (spin ratio 2)   Sig4   T17/23   GyH gain for (G)   T17/19   The ratio of the GyH gain for (F) and the   5   0   3   % (spin ratio 2)   Sig4   T17/23   GyH gain for (G)   T17/19   The ratio of the GyH gain for (F) and the   5   0   3   % (spin ratio 2)   Sig4   T17/23   GyH gain for (G)   T17/19   The ratio of the GyH gain for (F) and the   5   0   3   % (spin ratio 2)   Sig4   T17/23   GyH gain for (G)   T17/19   The ratio of the GyH gain for (F) and the   5   0   3   % (spin ratio 2)   Sig4   T17/23   GyH gain for (G)   T17/24   T17/		P <sub>3</sub> H	Sig.4	Т3		4.4	4.75	5.1	V
Yeomponent amplifier   ΔY1   Sig1   T13/15   The ratio of the GyH gain for (E) and the   3   0   3   % (spin ratio 1)   Sig4   T17/19   GyH gain for (F) and the   3   0   3   % (spin ratio 2)   Sig4   T17/19   GyH gain for (F) and the   5   0   3   % (spin ratio 2)   Sig4   T17/23   GyH gain for (G)   T17/19   The ratio of the GyH gain for (F) and the   5   0   3   % (spin ratio 2)   Sig4   T17/23   GyH gain for (G)   T17/19   The ratio of the GyH gain for (F) and the   5   0   3   % (spin ratio 2)   Sig4   T17/23   GyH gain for (G)   T17/19   The ratio of the GyH gain for (F) and the   5   0   3   % (spin ratio 2)   Sig4   T17/23   GyH gain for (G)   T17/19   The ratio of the GyH gain for (F) and the   5   0   3   % (spin ratio 2)   Sig4   T17/23   GyH gain for (G)   T17/24   T17/	(J) The gain ratios between	the differen	ıt signals wh	nen compon	ent is selected				
Sign   1717   1719   Spht   pain for (F)	· · · · · · · · · · · · · · · · · · ·		1	1		-3	0	3	%
gain ratio 2 Sig. 4 17:1/23 C <sub>N</sub> N4 gain for (G)	•		_		G <sub>N</sub> H gain for (F)		//		
Fig.	•	ΔΥ2	_		• = ::	-3	0	3	%
K  The pin 10 (RGB signal) input when baseband is selected   Amplifier gain (low)   G_BM   Sig.1   T13/15   The gain for a 996m/Vp-p 100kHz signal   4.05   5.87   5.46   dB   Amplifier gain (high)   G_BH   Sig.1   T13/15   The gain for a 761m/Vp-p 100kHz signal   7.68   7.88   7.68   7.81   dB   Input clamp voltage   C10H   Sig.1   T13/15   The gain for a 761m/Vp-p 100kHz signal   7.38   7.6   7.81   dB   Input clamp voltage   G10H   Sig.1   T13/15   The gain for a 996m/Vp-p 100kHz signal   7.38   7.6   7.81   dB   Input clamp voltage   G2H   Sig.1   T13/15   The gain for a 781m/Vp-p 100kHz signal   7.38   7.6   7.81   dB   Input clamp voltage   C2H   Sig.1   T10   The T10 sync tip potential for a 781m/Vp-p 100kHz signal   7.38   7.6   7.81   dB   Input clamp voltage   C2H   Sig.1   T10   The T10 sync tip potential for a 781m/Vp-p   4/0   4.35   4.7   V   Input clamp voltage   C3H   Sig.1   T13/15   The gain for a 781m/Vp-p 100kHz signal   5.05   5.27   5.48   dB   Amplifier gain (high)   G2H   Sig.1   T13/15   The gain for a 781m/Vp-p 100kHz signal   5.05   5.27   5.48   dB   Input clamp voltage   C3H   Sig.1   T13/15   The gain for a 781m/Vp-p 100kHz signal   7.38   7.6   7.81   dB   Input clamp voltage   C3H   Sig.1   T13/15   The gain for a 781m/Vp-p 100kHz signal   7.38   7.6   7.81   dB   Input clamp voltage   C3H   Sig.1   T13/15   The gain for a 781m/Vp-p 100kHz signal   7.38   7.6   7.81   dB   Input clamp voltage   C3H   Sig.1   T13/15   The gain for a 781m/Vp-p 100kHz signal   7.38   7.6   7.81   dB   Input clamp voltage   C3H   Sig.1   T13/15   The gain for a 781m/Vp-p 100kHz signal   7.38   7.6   7.81   dB   Input clamp voltage   C3H   Sig.1   T13/15   The ratio of the G9H gain for (l) and the   -3   0   3   %   7.81   T10		ΔΝ	_		'' - ''	-3	0	3	%
Amplifier gain (low)	(K) The pin 10 (RGB signal)	l Linnut when			I N S ()				
Amplifier gain (high)		1			The gain for a 996mVn-n 100kHz signal	5.05	5.27	5.48	dВ
Input clamp voltage			_		11 9/	$\overline{}$			
(L) The pin 6 (RGB signal) input when baseband is selected  Amplifier gain (low)			_						
Amplifier gain (low)   GgM   Sig.1   T13/15   The gain for a 996m/yph (00kHz signal   5.05   6.27   5.48   dB					input			7	<u> </u>
Amplifile gain (high)	(L) The pin 6 (RGB signal) i	nput when b	paseband is	selected					
Input clamp voltage	Amplifier gain (low)	G <sub>B</sub> M	Sig.1	T13/15	The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Imput   Impu	Amplifier gain (high)	G <sub>B</sub> H	Sig.1	T13/15	The gain for a 761mVp-p 100kHz signal	7.38	7.6	7.81	dB
Amplifier gain (low)         G <sub>B</sub> M         Sig.1         T13/15         The gain for a 996mVp-p 100kHz signal         5.05         5.27         5.48         dB           Amplifier gain (high)         G <sub>B</sub> H         Sig.1         T13/15         The gain for a 761mVp-p 100kHz signal         7.38         7.6         7.81         dB           Input clamp voltage         C <sub>3</sub> H         Sig.1         T10         Tpf 710 synctip potential for a 761mVp-p         4.0         4.35         4.7         V           (N) The gain ratios between the different signals when basepland is selected.         T13/15         The ratio of the G <sub>B</sub> H gain for (I) and the signal part for	Input clamp voltage	C <sub>6</sub> H	Sig.1	T10		4.0	4.35	4.7	V
Amplifier gain (low)         G <sub>B</sub> M         Sig.1         T13/15         The gain for a 996mVp-p 100kHz signal         5.05         5.27         5.48         dB           Amplifier gain (high)         G <sub>B</sub> H         Sig.1         T13/15         The gain for a 761mVp-p 100kHz signal         7.38         7.6         7.81         dB           Input clamp voltage         C <sub>3</sub> H         Sig.1         T10         Tpf 710 synctip potential for a 761mVp-p         4.0         4.35         4.7         V           (N) The gain ratios between the different signals when basepland is selected.         T13/15         The ratio of the G <sub>B</sub> H gain for (I) and the signal part for	(M) The pin 3 (RGB signal)	input when	baseband i	s selected		//			
Amplifier gain (high)         GBH         Sig.1         T13/15         The gain for a 761mVp-p 100kHz signal         7.38         7.6         7.81         dB           Input clamp voltage         C <sub>3</sub> H         Sig.1         T10         The f10 sync tip patential for a 761mVp-p (hout for a 761mVp-p)         4.0         4.35         4.7         V           (N) The gain ratios between the different signals when baselyand is selected         Baseband amplifier gain ratio         ΔB1         Sig.1         T13/15         The ratio of the GBH gain for (I) and the Sig.1         -3         0         3         %           Baseband amplifier gain ratio 2         ΔB2         Sig.1         713/15         The ratio of the GBH gain for (I) and the Sig.1         -3         0         3         %           Baseband amplifier gain ratio 3         ΔB3         Sig.1         713/15         The ratio of the GBH gain for (I) and the Sig.1 gain for (I) and the Sig.1 for 72/12 GBH gain for (K)         -3         0         3         %           (O) Gain frequency characteristics (Common to all modes and input signals offer than Y/C mixed mode)         The difference between GYH and the gain for (J) and the gain for J) sig.1         -0.5         0         +0.5         dB           6(P) DC voltage when output muting applied (Common to all modes)         T13/15         The difference between GYH and the gain for (J) and the gain for J) sig.		1			The gain for a 996mVp-p 100kHz signal	5.05	5.27	5.48	dB
Input clamp voltage									
(N) The gain ratios between the different signals when baseband is selected		_	_		The T10 sync tip potential for a 761mVp-p				V
Baseband amplifier gain ratio 1   AB1   Sig.1   T13/15   The ratio of the GgH gain for (J) and the GgH gain for (J) and the Sig.1   T17/19   T12/123   GgH gain for (J) and the Sig.1   T12/123   T12/123   GgH gain for (J) and the Sig.1   T12/123   GgH gain for (J) and the Sig.1   T12/123   GgH gain for (J) and the Sig.1   T12/123   T12/123   GgH gain for (J) and the Sig.1   T12/123	(NI) The gain ratios hatuses	the differen	at aignala w	han haasha					
Ratio 1   Sig. 1   T/7//19   G <sub>B</sub> H gain for (J)   Sig. 1   T/3/15   The ratio of the G <sub>B</sub> H gain for (J) and the ratio 2   Sig. 1   T/3/15   The ratio of the G <sub>B</sub> H gain for (J) and the ratio 3   Sig. 1   T/3/15   The ratio of the G <sub>B</sub> H gain for (J) and the ratio 3   Sig. 1   T/3/12   G <sub>B</sub> H gain for (K)   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J) and the ratio 3   Sig. 1   T/3/12   G <sub>B</sub> H gain for (K)   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J) and the ratio 3   Sig. 1   T/3/12   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J) and the ratio 3   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J) and the ratio 3   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J) and the ratio 3   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J)   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J)   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J)   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J)   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J)   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J)   Sig. 1   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J)   Sig. 1   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J)   Sig. 1   Sig. 1   Sig. 1   T/3/12   The ratio of the G <sub>B</sub> H gain for (J)   Sig. 1   Sig. 1						2	0	2	0/
Ratio 2   Sig.1   T21/23   GBH gain for (K)   Sig.1   T21/23   GBH gain for (K)   Sig.1   T17/19   The ratio of the GBH gain for (J) and the sig.1   T21/23   SgH gain for (K)   Sig.1   Sig.1   T13/15   The difference between GγH and the gain for a 76 fm/Vp-p, 6MHz input   Sig.1   Sig.1   T13/15   The difference between GγH and the gain for 2.0.5   Sig.1   Sig.1   Sig.1   T13/15   The difference between GγH and the gain for 2.0.5   Sig.1   Sig.	· -	ДБТ	_		5 -	, ,	U	3	70
ratio 3         Sig.f.         T21/23         GeH gain for (K)         Leading frequency characteristics (Component to all modes and Journal signals other than Y/C mixed mode)         Leading frequency characteristics (Component to all modes and Journal signals other than Y/C mixed mode)         -0.5         0         +0.5         dB           6MHz low-pass filter attenuation         Fy6         Sig.1         T13/15         The difference between GyH and the gain for a 761mVp-p, 6MHz input         -0.5         0         +0.5         dB           10MHz low-pass filter attenuation         Fy10         Sig.1         T13/15         The difference between GyH and the gain for a 761mVp-p, 6MHz input         -0.5         0         +0.5         dB           10MHz low-pass filter attenuation         Fy10         Sig.1         T13/15         The difference between GyH and the gain for a 761mVp-p, 6MHz input         -0.5         0         +0.5         dB           10MHz low-pass filter attenuation         Fy10         Sig.1         T13/15         The difference between GyH and the gain for a 761mVp-p, 6MHz input         -0.5         0         +0.5         dB           10MHz low-pass filter attenuation         Fy10         T13         T13         T14         T14         T14         T14         T15         T15         T15         T15         T15         T15         T15         T	· -	ΔΒ2	- 4	/ / .		-3	0	3	%
(O) Gain frequency characteristics (Common to all modes and input signals other than Y/C mixed mode)  6MHz low-pass filter attenuation  Fy 6 Sig.1 T13/15 The difference between GyH and the gain for a 76fmVp-p, 6MHz input  10MHz low-pass filter attenuation  Fy 10 Sig.1 T13/15 The difference between GyH and the gain for a 76fmVp-p, 6MHz input  (P) DC voltage when output muting applied (Common to all modes)  Fin 13 voltage  V18 T18 3.7 4.05 4.4 V  Fin 15 voltage  V19 T17 17 3.9 4.25 4.6 V  Fin 19 voltage  V19 T19 3.9 4.25 4.6 V  Fin 21 voltage  V21 T21 3.9 4.25 4.6 V  Fin 23 voltage  V22 T23 3.9 4.25 4.6 V  (Q) Output DC voltage characteristics  D/A converter reference voltage  V18 T12 When driving an 800μA load current  3.2 3.4 3.6 V  Letterbox output DC  VLB T16 In letterbox control mode (when driving a south of the property of the pr	· =	ΔΒ3	///			-3	0	3	%
6MHz low-pass filter attenuation  Fy6 Sig.1 T13/15 The difference between GyH and the gain for a 761mVp-p, 6MHz input  10MHz low-pass filter attenuation  Fy10 Sig.1 T13/15 The difference between GyH and the gain for a 761mVp-p, 6MHz input  (P) DC voltage when output muting applied (Common to all modes)  Fin 13 voltage V13 T13 T13 3.7 4.05 4.4 V  Fin 15 voltage V15 T15 T15 T17 T17 T17 T17 T17 T19		eristics (Cor	//		4-//				
attenuation         for a /76 fmVp-p, 6MHz input         —           10MHz low-pass filter attenuation         Fy10         Sig.1         T13/15         The difference between GyH and the gain for a 761mVp-p, 10MHz input         -0.5         0         +0.5         dB           (P) DC voltage when output muting applied (Common to all modes)           Pin 13 voltage         V13         T18         3.7         4.05         4.4         V           Pin 15 voltage         V15         716         3.7         4.05         4.4         V           Pin 17 voltage         V17         717         3.9         4.25         4.6         V           Pin 19 voltage         V19         T19         3.9         4.25         4.6         V           Pin 21 voltage         V21         T21         3.9         4.25         4.6         V           Pin 23 voltage         V23         T23         3.9         4.25         4.6         V           Q) Output DC voltage othar-cristics         VDA         T12         When driving an 800µA load current         3.2         3.4         3.6         V           4 : 3 output mode DC         V43         T16         In letterbox control mode (when driving a 800µA load current)         2.05         2.2 </td <td>• • •</td> <td>· ·</td> <td></td> <td></td> <td></td> <td>-0.5</td> <td>n</td> <td>+0.5</td> <td>dВ</td>	• • •	· ·				-0.5	n	+0.5	dВ
attenuation         for a 761mVp-p, 10MHz input         (P) DC voltage when output muting applied (Common to all modes)           Pin 13 voltage         V13         T18         3.7         4.05         4.4         V           Pin 15 voltage         V15         T16         3.7         4.05         4.4         V           Pin 17 voltage         V17         T17         3.9         4.25         4.6         V           Pin 19 voltage         V19         T19         3.9         4.25         4.6         V           Pin 21 voltage         V21         T21         3.9         4.25         4.6         V           Pin 23 yoltage         V23         T23         3.9         4.25         4.6         V           QO Output DC voltage characteristics         VDA         T12         When driving an 800μA load current         3.2         3.4         3.6         V           D/A converter reference voltage         VDA         T16         In 4 : 3 control mode (no load)         0         0.01         0.35         V           Letterbox output DC         VLB         T16         In letterbox control mode (when driving a 500μA load current)         1.0         2.0         2.2         2.35         V	•			10/13		-0.5	U	+0.0	uБ
Pin 13 voltage         V13         T18         3.7         4.05         4.4         V           Pin 15 voltage         V15         T15         3.7         4.05         4.4         V           Pin 15 voltage         V17         T17         3.9         4.25         4.6         V           Pin 19 voltage         V19         T19         3.9         4.25         4.6         V           Pin 21 voltage         V21         T21         3.9         4.25         4.6         V           Pin 23 voltage         V23         T23         3.9         4.25         4.6         V           Q(Q) Output DC voltage characteristics         V <t< td=""><td>•</td><td>F<sub>Y</sub>10</td><td>Sig.1</td><td>T13/15</td><td>, ,</td><td>-0.5</td><td>0</td><td>+0.5</td><td>dB</td></t<>	•	F <sub>Y</sub> 10	Sig.1	T13/15	, ,	-0.5	0	+0.5	dB
Pin 15 voltage         V15         T15         3.7         4.05         4.4         V           Pin 17 voltage         V17         T17         3.9         4.25         4.6         V           Pin 19 voltage         V19         T19         3.9         4.25         4.6         V           Pin 21 voltage         V21         T21         3.9         4.25         4.6         V           Pin 23 voltage         V23         T23         3.9         4.25         4.6         V           QO Output DC voltage characteristics         V         T12         When driving an 800μA load current         3.2         3.4         3.6         V           Voltage         T12         When driving an 800μA load current         3.2         3.4         3.6         V           Letterbox output mode DC         V43         T16         In 4 : 3 control mode (no load)         0         0.01         0.35         V           Letterbox output DC         VLB         T16         In letterbox control mode (when driving a 500μA load current)         2.05         2.2         2.35         V           Squeezed output DC         VSQ         T16         In squeeze control mode (when driving a 600μA load current)         4.4         4.7         5.0<	(P) DC voltage when output	muting app	olied (Comn	non to all mo	odes)				
Pin 15 voltage       V15       T16       3.7       4.05       4.4       V         Pin 17 voltage       V17       T17       3.9       4.25       4.6       V         Pin 19 voltage       V19       T19       3.9       4.25       4.6       V         Pin 21 voltage       V21       T21       3.9       4.25       4.6       V         Pin 23 voltage       V23       T23       3.9       4.25       4.6       V         (Q) Output DC voltage characteristics         D/A converter reference voltage       VDA       T12       When driving an 800μA load current       3.2       3.4       3.6       V         voltage       T12       When driving an 800μA load current       3.2       3.4       3.6       V         Letterbox output mode DC       V43       T16       In 4 : 3 control mode (no load)       0       0.01       0.35       V         Letterbox output DC       VLB       T16       In letterbox control mode (when driving a 500μA load current)       2.05       2.2       2.35       V         Squeezed output DC       VSQ       T16       In squeeze control mode (when driving a 4.4       4.7       5.0       V	Pin 13 voltage	V <sub>13</sub>		T13		3.7	4.05	4.4	V
Pin 17 voltage         V <sub>17</sub> T17         3.9         4.25         4.6         V           Pin 19 voltage         V <sub>19</sub> T19         3.9         4.25         4.6         V           Pin 21 voltage         V <sub>21</sub> T21         3.9         4.25         4.6         V           Pin 23 voltage         V <sub>23</sub> T23         3.9         4.25         4.6         V           (Q) Output DC voltage characteristics         D/A converter reference voltage         V <sub>DA</sub> T12         When driving an 800μA load current         3.2         3.4         3.6         V           4 : 3 output mode DC         V <sub>43</sub> T16         In letterbox control mode (no load)         0         0.01         0.35         V           Letterbox output DC         V <sub>LB</sub> T16         In letterbox control mode (when driving a 500μA load current)         2.05         2.2         2.35         V           Squeezed output DC         V <sub>SQ</sub> T16         In squeeze control mode (when driving a 4.4         4.7         5.0         V	Pin 15 voltage			T15		3.7	4.05	4.4	V
Pin 19 voltage         V19         T19         3.9         4.25         4.6         V           Pin 21 voltage         V21         T21         3.9         4.25         4.6         V           Pin 23 voltage         V23         T23         3.9         4.25         4.6         V           (Q) Output DC voltage characteristics         D/A converter reference voltage         VDA         T12         When driving an 800μA load current         3.2         3.4         3.6         V           4 : 3 output mode DC         V43         T16         In 4 : 3 control mode (no load)         0         0.01         0.35         V           Letterbox output DC         VLB         T16         In letterbox control mode (when driving a 500μA load current)         2.05         2.2         2.35         V           Squeezed output DC         VSQ         T16         In squeeze control mode (when driving a 4.4         4.7         5.0         V	Pin 17 voltage			<b>T</b> 17		3.9	4.25	4.6	V
Pin 21 voltage	Pin 19 voltage			T19		3.9	4.25	4.6	V
Pin 23 voltage         V23         T23         3.9         4.25         4.6         V           (Q) Output DC voltage characteristics           D/A converter reference voltage         VDA         T12         When driving an 800μA load current         3.2         3.4         3.6         V           4 : 3 output mode DC         V43         T16         In 4 : 3 control mode (no load)         0         0.01         0.35         V           Letterbox output DC         VLB         T16         In letterbox control mode (when driving a 500μA load current)         2.05         2.2         2.35         V           Squeezed output DC         VSQ         T16         In squeeze control mode (when driving a 4.4         4.7         5.0         V	Pin 21 voltage			T21		3.9	4.25	4.6	V
(Q) Output DC voltage characteristics  D/A converter reference voltage  4:3 output mode DC  V <sub>LB</sub> T16  In 4:3 control mode (no load)  O 0.01  O.35  V  Letterbox output DC  V <sub>LB</sub> T16  In letterbox control mode (when driving a 500μA load current)  Squeezed output DC  V <sub>SQ</sub> T16  In squeeze control mode (when driving a 4.4 4.7 5.0 V)	Pin 23 voltage			T23		3.9	4.25	4.6	V
voltage         4: 3 output mode DC         V <sub>43</sub> T16         In 4: 3 control mode (no load)         0         0.01         0.35         V           Letterbox output DC         V <sub>LB</sub> T16         In letterbox control mode (when driving a 500μA load current)         2.05         2.2         2.35         V           Squeezed output DC         V <sub>SQ</sub> T16         In squeeze control mode (when driving a 4.4         4.7         5.0         V	(Q) Output DC voltage char	_		•					
4: 3 output mode DC         V <sub>43</sub> T16         In 4: 3 control mode (no load)         0         0.01         0.35         V           Letterbox output DC         V <sub>LB</sub> T16         In letterbox control mode (when driving a 500μA load current)         2.05         2.2         2.35         V           Squeezed output DC         V <sub>SQ</sub> T16         In squeeze control mode (when driving a 4.4         4.7         5.0         V		V <sub>DA</sub>		T12	When driving an 800μA load current	3.2	3.4	3.6	V
Letterbox output DC     V <sub>LB</sub> T16     In letterbox control mode (when driving a 500μA load current)     2.05     2.2     2.35     V       Squeezed output DC     V <sub>SQ</sub> T16     In squeeze control mode (when driving a 4.4     4.7     5.0     V		V <sub>43</sub>		T16	In 4 : 3 control mode (no load)	0	0.01	0.35	V
Squeezed output DC V <sub>SQ</sub> T16 In squeeze control mode (when driving a 4.4 4.7 5.0 V	Letterbox output DC	-		T16	, ,	2.05	2.2	2.35	V
	Squeezed output DC	V <sub>SQ</sub>		T16	·	4.4	4.7	5.0	V

Note: The amplifier gain and amplifier gain ratios are the values when the components shown in the test circuit diagram are all connected.

## **Switching Characteristics** ("-" indicates OK under all conditions)

Switching Char		, marcate			110)			
Symbol	1/06:	\/20=		age (unit: V)	V207	1/205-	0	conditions
	VDC1	VDC2	VDC4	VDC5	VDC11	VDC22	SW1	SW2
I <sub>CC</sub> 1	0	0	3.3	0	3.3	3.3	ON	ON
I <sub>CC</sub> 2	0	0	3.3	0	3.3	3.3	ON	ON
(A) For a pin 10 (Y sig	<u> </u>			<del></del>				
GγM	0/3.3	0	-	-	0	3.3	ON/OFF	ON
G <sub>Y</sub> H	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
C <sub>10</sub> H	0/3.3	0	-	<u> </u>	3.3	3.3	ONOFF	ON
(B) For a pin 6 (chrom	1 ,	<u> </u>	osite/S selecte	d T			//	
G <sub>C</sub> M	0/3.3	0	-	-	0	3.3	ON/OFF	ON
G <sub>C</sub> H	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
C <sub>6</sub> H	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
(C) For a pin 3 (compo	1		ite selected	<del>                                     </del>				
G <sub>S</sub> M1	0/3.3	0	-	-	0	3.3	ON/OFF	ON
G <sub>S</sub> H1	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
C <sub>3</sub> H	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
(D) For a pins 3 (S sig			1	1				ı
G <sub>S</sub> M2	0/3.3	0	-	-	0	3.3	ON/OFF	ON
G <sub>S</sub> H2	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
(E) The gain ratios be	tween the differe	nt signals when	composite is s	elected				T
ΔYC	0/3.3	0	-	- //	3.3	3.3	ON/OFF	ON
ΔY <sub>S</sub> 1	0/3.3	0	-	-//	3.3	3.3	ON/OFF	ON
ΔC <sub>S</sub> 1	0/3.3	0	-	<u> -</u>	3.3	3.3	ON/OFF	ON
(F) The gain ratios be	tween the differe	nt signals when	S is selected					T
ΔY <sub>S</sub> 2	0/3.3	0	-	// -	3.3	0	ON/OFF	ON
ΔC <sub>S</sub> 2	0/3.3	0	- /		3.3	0	ON/OFF	ON
(G) The pin 10 (Y sign	nal) input when co	omponent is sel	lected		7 /			T
G <sub>Y</sub> M	0/3.3	3.3			0	3.3	ON/OFF	ON
GγH	0/3.3	3.3	//-		3,3	3.3	ON/OFF	ON
C <sub>10</sub> H	0/3.3	3.3	// -		3,3	3.3	ON/OFF	ON
(H) The pin 6 (B-Y or	R-Y signal) input	when compone	ent is selected					
G <sub>N</sub> M	0/3.3	3.3		- /	0	3.3	ON/OFF	ON
G <sub>N</sub> H	0/3.3	3.3		- //	3.3	3.3	ON/OFF	ON
P <sub>6</sub> H	0/3.3	3.3		-//	3.3	3.3	ON/OFF	ON
(I) The pin 3 (B-Y or R	R-Y signal) input	when componer	nt is selected					
G <sub>N</sub> M	0/3.3	3.3	- '	//-	0	3.3	ON/OFF	ON
G <sub>N</sub> H	0/3.3	3.3	-	/ -	3.3	3.3	ON/OFF	ON
P <sub>3</sub> H	0/3.3	3.3	- //	-	3.3	3.3	ON/OFF	ON
(J) The gain ratios bet	ween the differen	nt signals when	component is	selected				
ΔΥ1	0/3.3	3.3	/-/	-	3.3	3.3	ON/OFF	ON
ΔΥ2	0/3.3	3.3	//-	-	3.3	3.3	ON/OFF	ON
ΔΝ	0/3.3	3.3	-	-	3.3	3.3	ON/OFF	ON
(K) The pin 10 (RGB s	signal) input whe	n baseband is a	selected					
G <sub>B</sub> M	0/3.3	-//	-	-	0	3.3	ON/OFF	OFF
G <sub>B</sub> H	0/3.3	/-/	-	-	3.3	3.3	ON/OFF	OFF
C <sub>10</sub> H	0/3.3	//-	-	-	3.3	3.3	ON/OFF	OFF
(L) The pin 6 (RGB sig	gnal) input when	baseband is se	lected					
G <sub>B</sub> M	0/3.3	-	-	-	0	3.3	ON/OFF	OFF
G <sub>B</sub> H	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
С <sub>6</sub> Н	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
(M) The pin 3 (RGB si	ignal) input when	baseband is so	elected					
G <sub>B</sub> M	0/3.3	-	-	-	0	3.3	ON/OFF	OFF
G <sub>B</sub> H	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
	- 1 <del></del>	1	i ———	. —		. —		

a	c	4.	
Continued	from	preceding	page.

			Control volt	age (unit: V)			Switching	conditions
Symbol	VDC1	VDC2	VDC4	VDC5	VDC11	VDC22	SW1	SW2
(N) The gain ratios b	etween the differe	nt signals whe	n baseband is s	elected	•	•		
ΔΒ1	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
ΔΒ2	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
ΔΒ3	0/3.3	-	-	-	3.3	3.3	ON/OFF	OFF
(O) Gain frequency	characteristics (Co	mmon to all me	odes and input	signals other that	an Y/C mixed m	node)		
F <sub>Y</sub> 6	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
F <sub>Y</sub> 10	0/3.3	0	-	-	3.3	3.3	ON/OFF	ON
(P) DC voltage when	n output muting ap	plied (Commor	to all modes)					
V <sub>13</sub>	0	-	-	-	0/3.3	0/3.3	ON	- 7/
V <sub>15</sub>	3.3	-	-	-	0/3.3	0/3.3	ON	4//
V <sub>17</sub>	0	-	-	-	0/3.3	0/3.3	ON	//
V <sub>19</sub>	3.3	-	-	-	0/3.3	0/3.3	ON	//-
V <sub>21</sub>	0	-	-	-	0/3.3	0/3.3	ON	// -
V <sub>23</sub>	3.3	-	-	-	0/3.3	0/3.3	ON	-
(Q) Output DC volta	ge characteristics							,
$V_{DA}$	-	-	-	-	0/3.3	0/3.3	-//	-
V <sub>43</sub>	-	-	0	0	0/3.3	0/3.3	<u> - </u>	-
$V_{LB}$	-	-	0	3.3	0/3.3	0/3.3	//-	-
V <sub>SQ</sub>	-	-	3.3	0	0/3.3	0/3.3	// -	-

#### **Control Pin Functions**

Pin No.	Pin state	Low	Ope	n	High
1	Pin voltage	0 to 0.6V	1.55 to 1	1.75V	2.7 to 5V
	75Ω driver muting	13, 17, 21 muted	Not mu	uted	15, 19, 23 muted
2	Pin voltage	0 to 0.6V	1.55 to 1	1.75V	2.7 to 5V
	Signal input type switching	Composite/S mode	Baseband	d mode	Component mode
11	Pin voltage	0 to 1V		:	2.7 to 8V (note)
	Amplifier gain switching	6dB			8.5dB
22	Pin voltage	0 to 1V 2		2.7 to 8V (note)	
	Y/C mixer control	Y/C mixed mod	е	Composite mode	

Note: Never apply a voltage higher than the V<sub>CC</sub> voltage at pins 9 and 20 to pin 11 or pin 22.

- \*: Y/C mixed mode is illegal in modes other than composite/S mode.
- \*: In composite mode, use pin 6 to input the chrominance signal capacitor-coupled, pin 3 for the clamped composite signal, and pin 10 for the clamped Y signal. However, in S mode, pin 3 will have no input.

In component mode, pins 3 and 6 will be pedestal clamped B-Y and R-Y signals, respectively, while pin 10 will be the clamped Y signal input.

In baseband mode, pins 3, 6, and 10 are all clamped inputs, for the RGB signals, respectively.

Pins 11 and 22 must never be left open.

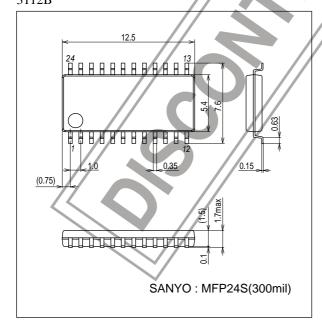
Pin 4	Pin 5	Pin 16 output DC
0 to 1V	0 to 1V	Low (0V) $\rightarrow$ 4 : 3 mode
0 to 1V	2.6 to 5V	$Middle\ (2.5V) \to Letterbox\ mode$
2.6 to 5V	0 to 1V	$High\; (5V) \to Squeezed\; mode$
2.6 to 5V	2.6 to 5V	Illegal values

### **Design Guaranteed Items** (at $Ta = 25^{\circ}C$ )

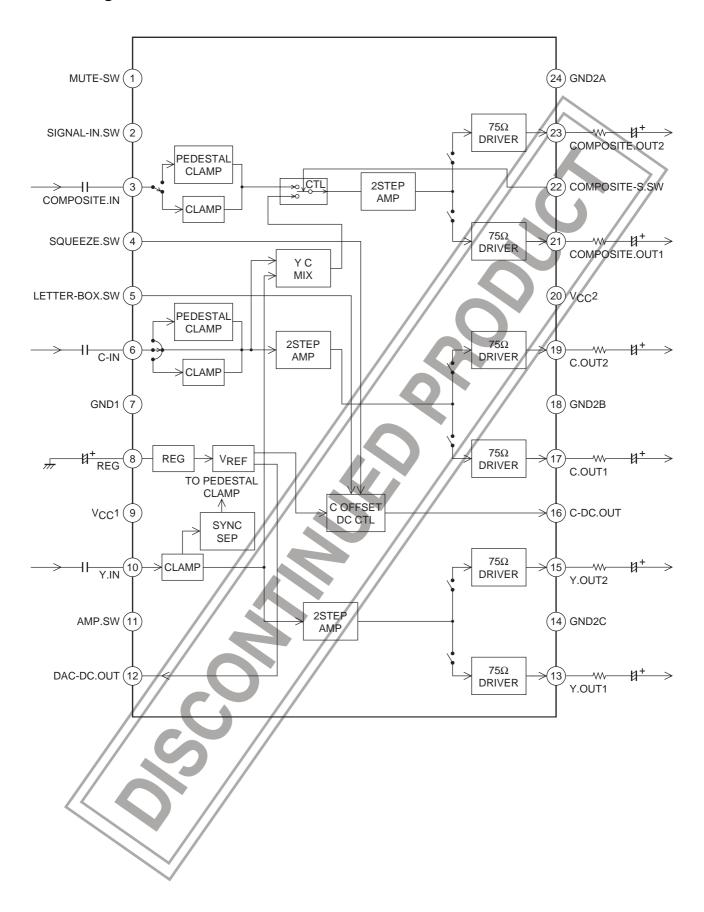
Parameter	Sumbal	Conditions			Unit	
Parameter	Symbol	Conditions	min	typ	max	Offic
<modes c="" mix<="" other="" td="" than="" y=""><td>ed Mode&gt;</td><td></td><td></td><td></td><td></td><td></td></modes>	ed Mode>					
Inter-channel crosstalk	CT	Input an f = 4MHz signal to another channel such that the		-65	-60	dB
		capacitor-coupled output becomes 1Vp-p. Measure the				
		amplitude of the 4MHz component on the monitored channel.				
		This parameter is stipulated to be the ratio of that level with the				
		amplitude of the 4MHz component on that other channel.				
Video signal-to-noise ratio	SN	Input a white 100% signal and apply a 3.3V level to pin 11.		-80	-78	dB
		Measure the signal-to-noise ratio in the output signal.				
Differential gain	DG	Input a standard 1Vp-p staircase signal (color) and leave pin 11		0.5	2	%
		open. Measure the differential gain in the output signal. Note				7/
		that the components shown in the test circuit diagram for this				
		parameter must be inserted at this time.				
Differential phase	DP	Input a standard 1Vp-p staircase signal (color) and leave pin 11	-1	0		dB
		open. Measure the differential phase in the output signal. Note	`			
		that the components shown in the test circuit diagram for this				
		parameter must be inserted at this time.				
<y c="" mixed="" mode=""></y>						
Inter-channel crosstalk	CT	Input an f = 4MHz signal to another channel such that the		-65	-60	dB
		capacitor-coupled output becomes 1Vp-p. Measure the				
		amplitude of the 4MHz component on the monitored channel.				
		This parameter is stipulated to be the ratio of that level with the				
		amplitude of the 4MHz component on that other channel.				
Video signal-to-noise ratio	SN	Input a white 100% signal and apply a 3.3V level to pin 11.		-74	-72	dB
		Measure the signal-to-noise ratio in the output signal.				
Differential gain	DG	Input a standard 761mVp-p staircase signal (color) and apply a		4	5.5	%
		3.3V level to pin 11. Measure the differential gain in the output				
		signal. Note that the components shown in the test circuit	ľ			
		diagram for this parameter must be inserted at this time.				
Differential phase	DP	Input a standard 761mVp-p staircase signal (color) and apply a	-1	0.5	1.5	dB
		3.3V level to pin 11. Measure the differential gain in the output				
		signal. Note that the components shown in the test circuit				
		diagram for this parameter must be inserted at this time.				

## **Package Dimensions**

unit: mm (typ) 3112B



#### **Block Diagram**



#### **Pin Functions**

For more information on the pin functions, see the I/O circuit diagrams, and for an operating description, see the block diagram.

Note that the data shown below consists of typical values and that detailed ratings are provided in the Electrical Characteristics.

Chara	acteristics.		1	1		
Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
10	Y-IN	ı	4.2V	Clamp form	Input pin for either the Y or a baseband signal. This pin is used for the Y signal for composite/S and component signal input, and for one of the RGB signals with sync. Keyed clamping (clamping at the lowest point in the signal, that is, at the sync tip) is applied whichever signal is input.  If a component signal is input, sync separation is performed and a clamp pulse for pedestal clamping is produced. The clamped signal is amplified by an amplifier that can be switched between two levels so that it becomes 2Vp-p with an output amplitude of 140IRE.	100kn
13	Y.OUT1	0	2.7V	11.6Ω	$75\Omega$ driver output for the signal input to pin 10. The pin 10 output signal is split into two, and one is passed through a muting circuit that mutes when pin 1 is low (0V) and output to the $75\Omega$ driver.	VCC VCC VCC VCC OUT
15	Y.OUT2	0	2.7V	11.60	$75\Omega$ driver output for the signal input to pin 10. Of the pin 10 input signals, the other signal is passed through a muting circuit that mutes when pin 1 is high (3.3 to 5.0V) and output to the $75\Omega$ driver.	VCC VCC VCC VCC
6	C-IN		4.8\	10kΩ	Input pin for chrominance, component, and baseband signals. The chrominance signal must be input to this pin when a composite/S signal input is used. The signal must be capacitor coupled. The B-Y or R-Y signal must be input to this pin when a component signal is input. The signal is clamped at the pedestal level. Any one of the RGB with sync signals must be input to this pin when a baseband signal is input. Keyed clamping will be applied to the signal. The capacitor coupled or clamped signal is amplified by an amplifier that can be switched between two levels so that it becomes 2Vp-p with an output amplitude of 140IRE.	200μΑ Δ Σ Σ Σ Σ Σ Σ Σ Σ Σ Σ Σ Σ Σ Σ Σ Σ Σ Σ

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Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
17	C.OUT1	0	3.9V	11.6kΩ	$75\Omega$ driver output for the signal input to pin 6. The pin 6 output signal is split into two, and one is passed through a muting circuit that mutes when pin 1 is low (0V) and output to the $75\Omega$ driver.	VCC VCC VCC OUT
19	C.OUT2	0	3.9V	11.6kΩ	$75\Omega$ driver output for the signal input to pin 6. Of the pin 10 input signals, the other signal is passed through a muting circuit that mutes when pin 1 is high (3.3 to 5.0V) and output to the $75\Omega$ driver.	VCC SG VCC OUT
3	COMPOSITE.IN	1	4.5V	Clamp form	Input pin for composite, component, and baseband signals. If a composite signal is input, it must be input to this pin, and if a baseband signal is input, any one of the RGB with sync signals must be input to this pin.  Keyed clamping will be applied to the signal.  For S signal input, this pin must be dropped to ground. For component signal input, input either the B-Y or R-Y signal to this pin. The signal will be clamped at the pedestal level.  The clamped signal is amplified by an amplifier that can be switched between two levels so that it becomes 2Vp-p with an output amplitude of 140IRE.	100kn   10kn   1
21	COMPOSITE. OUT1		3.57V	11.6Ω	75Ω driver output for the signal input to pin 3. The pin 3 output signal is split into two, and one is passed through a muting circuit that mutes when pin 1 is low (0V) and output to the 75Ω driver.	VCC VCC VCC VCC

Continued	from	preceding page.	

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Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
23	COMPOSITE. OUT2	0	3.57V	11.6Ω	$75\Omega$ driver output for the signal input to pin 3. Of the pin 3 input signals, the other signal is passed through a muting circuit that mutes when pin 1 is high (3.3 to 5.0V) and output to the $75\Omega$ driver.	VCC VCC VCC OUT
1	MUTE-SW	1	1.7V	21kΩ	Controls the muting applied to the output signals. This pin can be controlled from a 3.3 to 5V power supply microcontroller. (See the control pin function table.)	4.25V VCC VIIIO02 VX
2	SIGNAL-IN.SW	ı	1.7V	21kΩ	Switches the input circuit types of pins 3 and 6 to match the type of the input signal. This pin can be controlled from a 3.3 to 5V power supply microcontroller. (See the control pin function table.)	4.25V VCC WM 33KG TSAKO VCC WM 33KG TSAKO VCC WM 30KG TSAKO VCC WM
4	SQUEEZE.SW		2.40V	9.0GΩ	Inputs squeeze control information from the system microcontroller. This pin can be controlled from a 3.3 to 5V power supply microcontroller. (See the control pin function table.)	VCC VIIOS IN SkΩ
5	LETTER-BOX.SW		2.43V	8.1GΩ	Inputs letterbox control information from the system microcontroller. This pin can be controlled from a 3.3 to 5V power supply microcontroller. (See the control pin function table.)	VCC Ψηθοοι 5kΩ

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Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
16	C-DC.OUT	0	4.7V	4.1Ω	The LA7137M creates, and outputs from this pin, a stabilized DC voltage based on the control information input to pins 4 and 5. This pin outputs a low level (0V) for 4 : 3 mode, a middle level (2.2V) for letterbox mode, and a high level (5V) for squeeze mode. A $10k\Omega$ resistor must be inserted to superimpose the DC voltage output from pin 17 on the capacitor coupled chrominance output. (See the application circuit diagram.)	VCC
11	AMP-SW	1	2.4V	9.0GΩ	Control pin that switches the amplifier gain to match the amplitude of the input signal. This pin's input level can be switched between V <sub>CC</sub> and ground on the printed circuit board even by a 3.3 to 5.0V power supply microcontroller. (See the control pin functions table.)	VCC VTIOOE  VX  VX  VX  VX  VX  VX  VX  VX  VX  V
22	COMPOSITE- S.SW	Р	2.4V	9.0GΩ	Controls the on/off state of the Y/C mixer. When using a D/A converter that omits the composite output, the Y/C mixer must be turned on. At the same time as mixing the Y signal input to pin 10 with the chrominance signal input to pin 6, pin 3 will be dropped to ground. When pin 2 control specifies a signal type other than composite/S signal, this pin must be tied high, This pin's input level can be switched between VCC and ground on the printed circuit board even by a 3.3 to 5.0V power supply microcontroller. (See the control pin functions table.)	VCC Ψησοι 5kΩ π
12	DAC-DC.OUT	0	3.4V	4.0Ω	Outputs a DC reference voltage for use by a D/A converter. In particular, it outputs a 3.3V level. This reference voltage is unaffected by V <sub>CC</sub> fluctuations or temperature and can be used in conjunction with a resistor divider to produce the DC level required by the D/A converter.	VCC

Ground for systems other than the  $75\Omega$ 

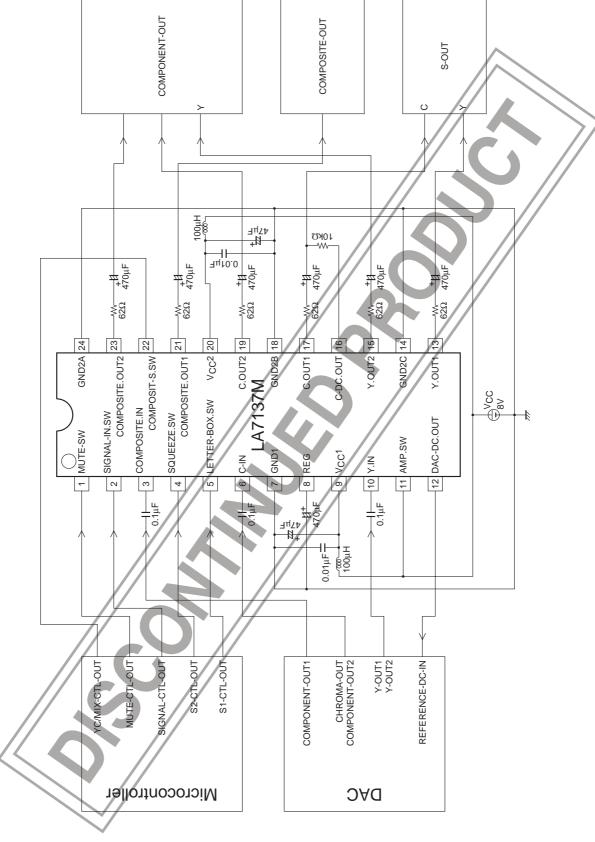
drive<u>r system.</u>

GND1

Continu	aed from preceding page.					
Pin No.	Pin	I/O	Pin voltage	I/O impedance	Description	Equivalent circuit
8	REG	0	4.35V	1.5kΩ	External pin for the regulator circuit that creates the IC internal reference voltage. Since the IC internal noise is influenced by the stability of this regulator, we recommend connecting a 470µF capacitor to this pin to if assuring a -80dB signal-to-noise ratio is required.	12kΩ 29.2kΩ 12kΩ 29.2kΩ 10kΩ 11kΩ 10kΩ 15kΩ 10kΩ 15kΩ 10kΩ 15kΩ
9	V <sub>CC</sub> 1	Р	8V		$V_{CC}$ (8V applied) for systems other than the 75Ω driver system. Insert a 47μF capacitor between this pin and pin 7.	
20	V <sub>CC</sub> 2	P	8V		$V_{CC}$ (8V applied) for the 75 $\Omega$ driver system. Insert a 47 $\mu$ F capacitor between this pin and pin 14, 18, or 24. The PCB layout related to this pin requires care due to the large amplitude output signals handled.	
14	GND2C	Р	0V		Ground for the 75\Omega driver system (pin 13 or 15). The PCB layout related to this pin requires care due to the large amplitude output signals handled.	
18	GND2B	Р	0V		Ground for the $75\Omega$ driver system (pin 17 or 19). The PCB layout related to this pin requires care due to the large amplitude output signals handled.	
24	GND2A	Р	0V		Ground for the 75 $\Omega$ driver system (pin 21 or 23). The PCB layout related to this pin requires care due to the large amplitude output signals handled.	

#### **Sample Application Circuit**

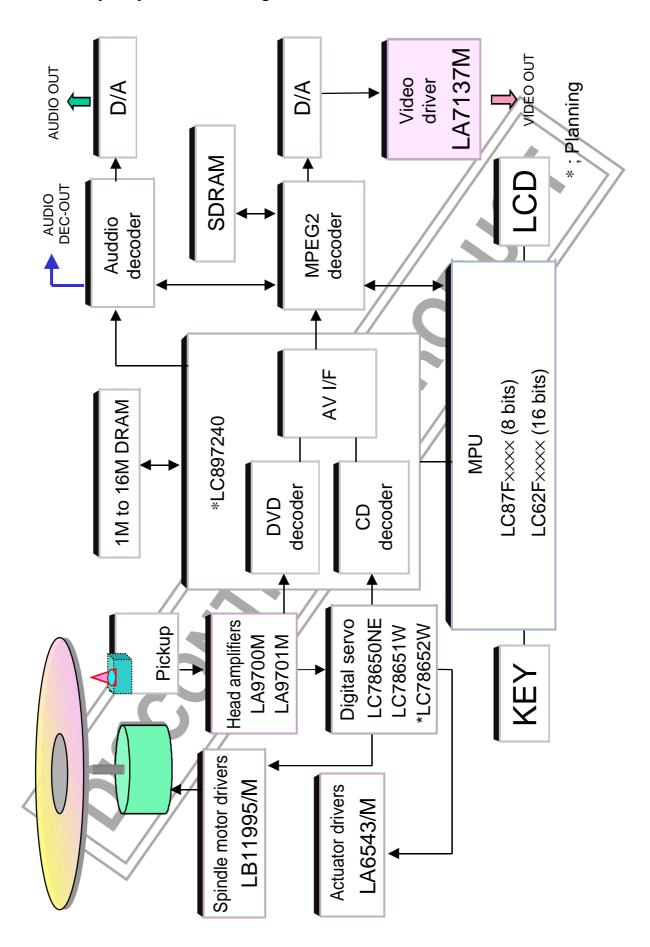
Single composite/S signal plus single component signal application using a single D/A converter



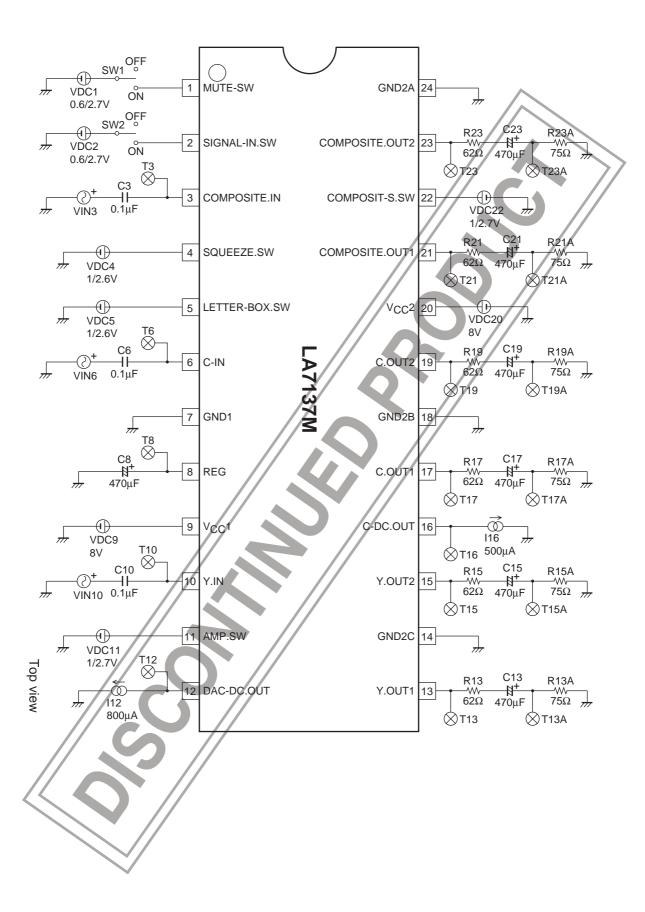
Application circuit diagram for end product that provides one output system each for composite/S and component outputs and the D/A converter output pin is shared between the S signal and the component signal systems. The muting control can be used to switch between the composite/S and component outputs.

The system microcontroller must be programmed to turn the Y/C mixer off when the component signal system is used.

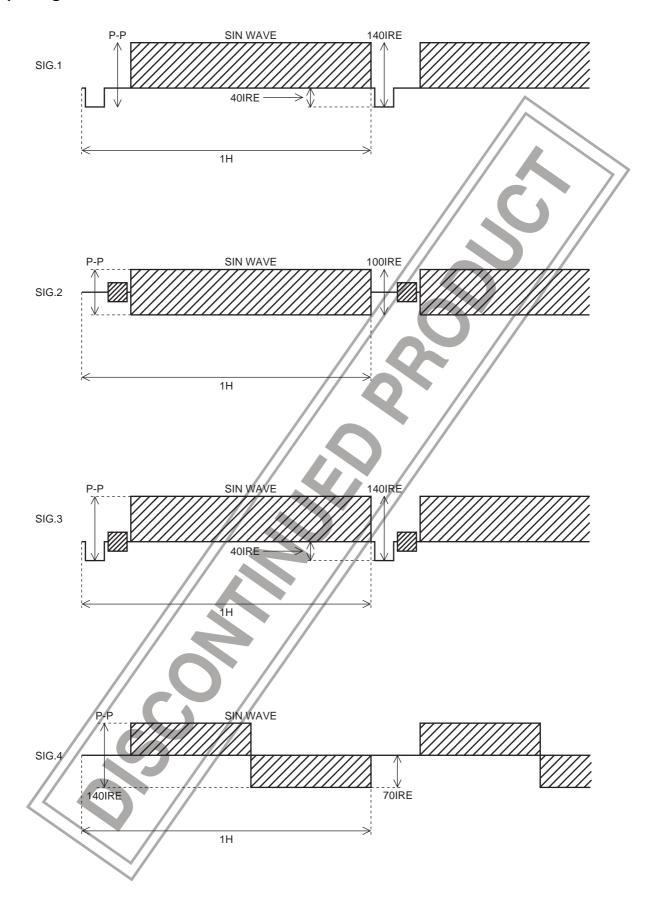
## **DVD Video Player System Block Diagram**



#### **Test Circuit**



## **Input Signal for Test**





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