B9940L

2.5V / 3.3V, 200 MHz, 1:18 Clock Distribution Buffer

Product Features

- 200MHz Clock Support
- LVPECL or LVCMOS/LVTTL Clock Input
- LVCMOS/LVTTL Compatible Inputs
- 18 Clock Outputs: Drive up to 36 Clock Lines
- 150ps Maximum Output-to-Output Skew
- Dual or Single Supply Operation:
  - 3.3V Core and 3.3V Outputs
  - 3.3V Core and 2.5V Outputs
  - 2.5V Core and 2.5V Outputs
- Pin Compatible with MPC940L
- Industrial Temp. Range: -40°C to +85°C
- 32-Pin LQFP Package

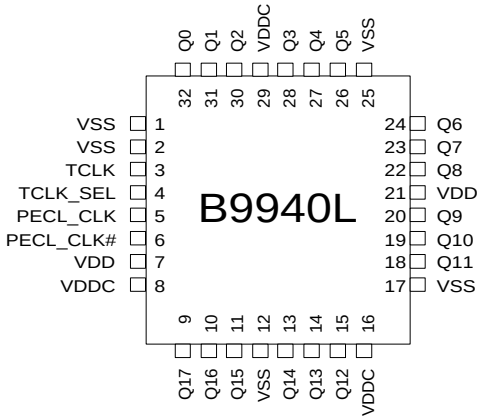
Description

The B9940L is a low voltage clock distribution buffer with the capability to select either a differential LVPECL or a LVCMOS/LVTTL compatible input clock. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The eighteen outputs are 2.5V or 3.3V compatible and can drive two series terminated 50Ω transmission lines. With this capability the B9940L has an effective fan-out of 1:36. Low output-to-output skews make the B9940L an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

Block Diagram

Figure 1

Pin Configuration



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Pin Description

PIN	NAME	PWR	I/O	Description
5	**PECL_CLK**		I, PU	PECL Input Clock.
6	**PECL_CLK#**		I, PD	PECL Input Clock.
3	**TCLK**		I, PD	External Reference/Test Clock Input.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	**Q(17:0)**	VDDC	O	Clock Outputs.
4	**TCLK_SEL**		I, PD	Clock Select Input. When low, PECL clock is selected and when high TCLK is selected.
8, 16, 29	**VDDC**			3.3V or 2.5V Power Supply for Output Clock Buffers.
7, 21	**VDD**			3.3V or 2.5V Power Supply
1, 2, 12, 17, 25	**VSS**			Common Ground

PD = Internal Pull-Down, PU = Internal Pull-Up.

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS - 0.3V
Maximum Input Voltage Relative to VDD: VDD + 0.3V
Storage Temperature: -65°C to + 150°C
Operating Temperature: -40°C to +85°C
Maximum ESD protection 2kV
Maximum Power Supply: 5.5V
Maximum Input Current: ±20mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

DC Parameters

Characteristic	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	VSS		0.8		All other inputs
Input High Voltage	VIH	2.0		VDD	V	All other inputs
Input Low Current (@VIL = VSS)	IIL[1]			-200	µA	
Input High Current (@VIL =VDD)	IIH[1]			200	µA	
Peak-to-Peak Input Voltage PECL_CLK	VPP	500		1000	mV	
Common Mode Range PECL_CLK	VCMR[2]	VDD-1.4	-	VDD-0.6	V	VDD = 3.3V
		VDD-1.0	-	VDD-0.6		VDD = 2.5V
Output Low Voltage	VOL[3]			0.5	V	IOL = 20mA
Output High Voltage	VOH[3]	2.4			V	IOH = -20mA, VDDC = 3.3V
		1.8				IOH = -20mA, VDDC = 2.5V
Quiescent Supply Current	IDD	-	2	5	mA	
Output Impedance	Zout	18	23	28	Ω	
Input Capacitance	Cin	-	4	-	pF	
VDD = 3.3V ±5% or 2.5V ±5%, VDDC = 3.3V ±5% or 2.5V ±5%, TA = -40°C to +85°C						

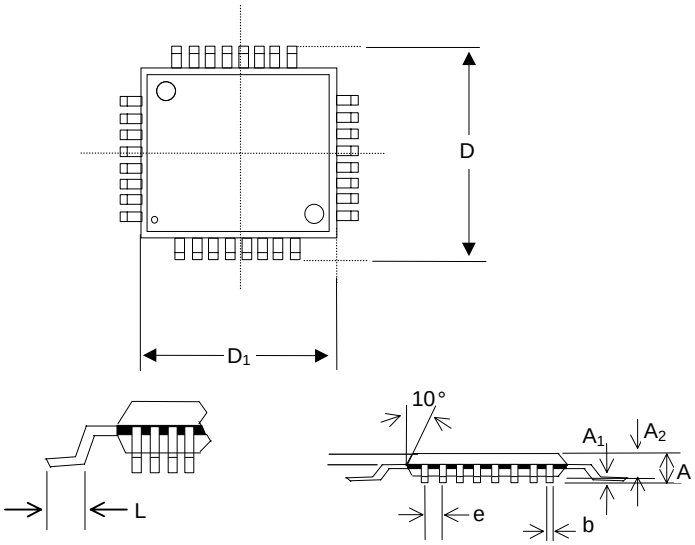
Note 1: Inputs have pull-up/pull-down resistors that effect input current.
Note 2: The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the “High” input is within the VCMR range and the input lies within the VPP specification.
Note 3: Driving series or parallel terminated 50Ω (or 50Ω to VDD/2) transmission lines.

AC Parameters[1]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Fmax	Maximum Input Frequency			200	MHz	
Tpd	PECL_CLK to Q Delay[2,4]	2.0	3.5	4.0	ns	VDD = 3.3V
		2.6	4.0	5.2		VDD = 2.5V
Tpd	TTL_CLK to Q Delay[2,4]	1.8	3.3	3.8	ns	VDD=3.3V
		2.3	3.8	4.4		VDD = 2.5V
FoutDC	Output Duty Cycle[2,3,4]	45		55	%	Measured at VDDC/2
Tskew	Output-to-Output Skew[2,4]			150	ps	VDD=3.3V, Fin = 150MHz
				200		VDD=2.5V, Fin = 150MHz
Tskew(pp)	Part-to-Part Skew[5]			1.4	ns	PECL, VDDC = 3.3V
				2.2		PECL, VDDC = 2.5V
Tskew(pp)	Part-to-Part Skew[5]			1.2	ns	TCLK, VDDC = 3.3V
				1.7		TCLK, VDDC = 2.5V
Tskew(pp)	Part to Part Skew[6]			850	ps	PECL_CLK
				750		TCLK
Tr / Tf	Output Clocks Rise / Fall Time[2,4]	0.3		1.1	ns	0.7V to 2.0V, VDDC = 3.3V
		0.3		1.2		0.5V to 1.8V, VDDC = 2.5V
VDD = 3.3V ±5% or 2.5V ±5%, VDDC = 3.3V ±5% or 2.5V ±5%, TA = -40°C to +85°C						

Note 1: Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
Note 2: Outputs driving 50Ω transmission lines.
Note 3: 50% input duty cycle.
Note 4: Outputs loaded with 30pF each
Note 5: Across temperature and voltage ranges, includes output skew
Note 6: For a specific temperature and voltage, includes output skew

Package Drawing and Dimensions (32 LQFP)



32 Pin LQFP Outline Dimensions

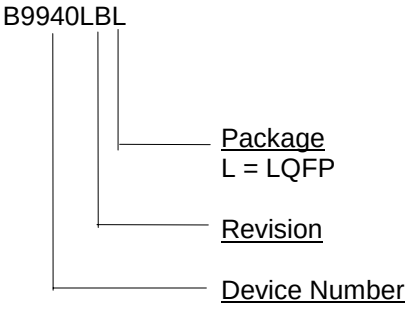
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.063	-	-	1.60
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.053	-	0.057	1.35	-	1.45
D	-	0.354	-	-	9.00	-
D_1	-	0.276	-	-	7.00	-
b	0.012	-	0.018	0.30	-	0.45
e	0.031 BSC			0.80 BSC		
L	0.018	-	0.030	0.45	-	0.75

Ordering Information

Part Number	Package Type	Production Flow
B9940LBL	32 PIN LQFP	Industrial, -40°C to +85°C

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI
B9940LBL
Date Code, Lot #



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Document Title: B9940L 2.5V / 3.3V, 200 MHz, 1:18 Clock Distribution Buffer **Document Number:** 38-07105				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107509	06/14/01	NDP	Convert from IMI to Cypress