MONOLITHIC 8-BIT PROGRAMMABLE DELAY LINE (SERIES 3D7438)

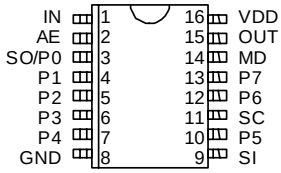
Super-Fine Resolution

FEATURES

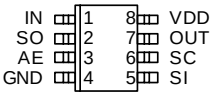
- All-silicon, low-power CMOS technology
- TTL/CMOS compatible inputs and outputs
- Vapor phase, IR and wave solderable
- Leading- and trailing-edge accuracy
- Programmable via serial or parallel interface
- **Increment range:** 50ps through 250ps
- **Delay tolerance:** 0.5% (See Table 1)
- **Supply current:** 3mA typical
- **Temperature stability:** ±1.5% max (-40C to 85C)
- **Vdd stability:** ±0.5% max (4.75V to 5.25V)

RoHS Compliant

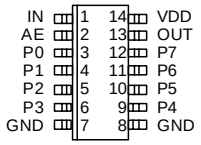
PACKAGES



3D7438S-xx SOW16



3D7438Z-xx SOIC8



3D7438D-xx SOIC14

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D7438 device is a versatile 8-bit programmable monolithic delay line. The input (IN) is reproduced at the output (OUT) without inversion, shifted in time as per the user selection. Delay values, programmed either via the serial or parallel interface, can be varied over 255 equal steps according to the formula:

$$T_{i,nom} = T_{inh} + i * T_{inc}$$

where i is the programmed address, T_{inc} is the delay increment (equal to the device dash number), and T_{inh} is the inherent (address zero) delay. The device features both rising- and falling-edge accuracy.

PIN DESCRIPTIONS

IN	Signal Input
OUT	Signal Output
MD	Mode Select
AE	Address Enable
P0-P7	Parallel Data Input
SC	Serial Clock
SI	Serial Data Input
SO	Serial Data Output
VDD	+5 Volts
GND	Ground

The all-CMOS 3D7438 integrated circuit has been designed as a reliable, economic alternative to hybrid TTL programmable delay lines. It is offered in a standard surface mount 16-pin SOL. An 8-pin SOIC package is available for applications where the parallel interface is not needed. Similarly, a 14-pin SOIC is offered for applications where the serial interface is not needed.

TABLE 1: PART NUMBER SPECIFICATIONS

PART NUMBER	DELAYS AND TOLERANCES			INPUT RESTRICTIONS			
	Inherent Delay (ns)	Delay Range (ns)	Delay Step (ps)	Max Freq (Addr=0)	Max Freq (Addr=255)	Min P.Width (Addr=0)	Min P.Width (Addr=255)
3D7438x-50	7.0 ± 0.5	12.750 ± .05	50 ± 25	150 MHz	98 MHz	3.3 ns	5.1 ns
3D7438x-60	7.0 ± 0.5	15.300 ± .06	60 ± 30	150 MHz	82 MHz	3.3 ns	6.1 ns
3D7438x-75	7.0 ± 0.5	19.125 ± .08	75 ± 38	150 MHz	65 MHz	3.3 ns	7.6 ns
3D7438x-80	7.0 ± 0.5	20.400 ± .08	80 ± 40	150 MHz	61 MHz	3.3 ns	8.1 ns
3D7438x-100	7.0 ± 0.5	25.500 ± .10	100 ± 50	150 MHz	49 MHz	3.3 ns	10.0 ns
3D7438x-125	7.0 ± 0.5	31.875 ± .13	125 ± 63	150 MHz	39 MHz	3.3 ns	12.7 ns
3D7438x-150	7.0 ± 0.5	38.250 ± .15	150 ± 75	150 MHz	32 MHz	3.3 ns	15.3 ns
3D7438x-200	7.0 ± 0.5	51.000 ± .20	200 ± 100	150 MHz	24 MHz	3.3 ns	20.4 ns
3D7438x-250	7.0 ± 0.5	63.750 ± .25	250 ± 125	150 MHz	19 MHz	3.3 ns	25.5 ns

NOTES: Replace the 'x' in the part number with D, S or Z, depending on choice of package.
Any dash number between 50 and 250 not shown is also available as standard.
See application notes section for more details

APPLICATION NOTES

GENERAL INFORMATION

The 8-bit programmable 3D7438 delay line architecture is comprised of a sequence of five identical delay cells connected in series, all of which are controlled by a common current. This current, in turn, is controlled by the user-selected programming data (the address). The delay cells produce at their output a replica of the signal present at the input, shifted in time. The change in delay from one address setting to the next is called the *increment*, or LSB. It is nominally equal to the device dash number. The minimum delay, achieved by setting the address to zero, is called the *inherent delay*.

For best performance, it is essential that the power supply pin be adequately bypassed and filtered. In addition, the power bus should be of as low an impedance construction as possible. Power planes are preferred. Also, signal traces should be kept as short as possible.

DELAY ACCURACY

There are a number of ways of characterizing the delay accuracy of a programmable line. The first is the *differential nonlinearity* (DNL), also referred to as the increment error. It is defined as the deviation of the increment at a given address from its nominal value. For all dash numbers, the DNL is within 0.5 LSB at every address (see Table 1: Delay Step).

The *integrated nonlinearity* (INL) is determined by first constructing the least-squares best fit straight line through the delay-versus-address data. The INL is then the deviation of a given delay from this line. For all dash numbers, the INL is within 1.0 LSB at every address.

The *relative error* is defined as follows:

$$e_{rel} = (T_i - T_0) - i * T_{inc}$$

where i is the address, T_i is the measured delay at the i'th address, T_0 is the measured inherent delay, and T_{inc} is the nominal increment. It is very similar to the INL, but simpler to calculate. For all dash numbers, the relative error is less than 1.0 LSB at every address (see Table 1: Delay Range).

The *absolute error* is defined as follows:

$$e_{abs} = T_i - (T_{inh} + i * T_{inc})$$

where T_{inh} is the nominal inherent delay. The absolute error is limited to 1.5 LSB or 1.0 ns, whichever is greater, at every address.

The *inherent delay error* is the deviation of the inherent delay from its nominal value. For all dash numbers, it is limited to 0.5 ns.

DELAY STABILITY

The delay of CMOS integrated circuits is strongly dependent on power supply and temperature. The 3D7438 utilizes novel compensation circuitry to minimize the delay variations induced by fluctuations in power supply and/or temperature.

The 3D7438 is designed to be most stable at the maximum address setting (255). At this operating condition, the thermal coefficient of the absolute delay is limited to ±250 PPM/C, which is equivalent to a variation, over the -40C to 85C operating range, of ±1.5% from the room-temperature delay. At smaller address settings the thermal coefficient will be somewhat larger.

At the maximum address, the power supply sensitivity of the absolute delay is ±0.5% over the 4.75V to 5.25V operating range, with respect to the delay at the nominal 5.0V power supply. At smaller address settings the sensitivity will be somewhat larger.

INPUT SIGNAL CHARACTERISTICS

The maximum input frequency and minimum input pulse width are both limited by the device. Exceeding either limit will cause the signal to be blocked by the line. Furthermore, for a given device, these limitations vary with the user-specified address. The relationships are:

$$F_{Max} = 1250 / (i * T_{inc})$$
$$PW_{Min} = 0.4 * (i * T_{inc}),$$

where F_{Max} is in MHz, and PW_{Min} & T_{inc} are in ns. These relationships break down for small delays: F_{Max} can never be greater than 150 MHz, and PW_{Min} can never be smaller than 3.3 ns.

PROGRAMMING INTERFACE

Figure 1 illustrates the main functional blocks of the 3D7438 delay program interface. Since the 3D7438 is a CMOS design, all unused input pins must be returned to well defined logic levels, VDD or Ground.

APPLICATION NOTES (CONT'D)

TRANSPARENT PARALLEL MODE (MD = 1, AE = 1)

The eight program pins P0 - P7 directly control the output delay. A change on one or more of the program pins will be reflected on the output delay after a time $\mathbf{t_{PDV}}$, as shown in Figure 2. A register is required if the programming data is bused.

LATCHED PARALLEL MODE (MD = 1, AE PULSED)

The eight program pins P0 - P7 are loaded by the falling edge of the Enable pulse, as shown in Figure 3. After each change in delay value, a settling time $\mathbf{t_{EDV}}$ is required before the input is accurately delayed.

SERIAL MODE (MD = 0)

While observing data setup ($\mathbf{t_{DSC}}$) and data hold ($\mathbf{t_{DHC}}$) requirements, timing data is loaded in MSB-to-LSB order by the rising edge of the clock (SC) while the enable (AE) is high, as shown in Figure 4. The falling edge of the enable (AE) activates the new delay value which is reflected at the output after a settling time $\mathbf{t_{EDV}}$. As data is shifted into the serial data input (SI), the previous contents of the 8-bit input register are shifted out of the serial output port pin (SO) in MSB-to-LSB order, thus allowing cascading of multiple devices by connecting the serial output pin (SO) of the preceding device to the serial data input pin (SI) of the succeeding device, as illustrated in Figure 5. The total number of serial data bits in a cascade configuration must be eight times the number of units, and each group of eight bits must be transmitted in MSB-to-LSB order.

To initiate a serial read, enable (AE) is driven high. After a time $\mathbf{t_{EQV}}$, bit 7 (MSB) is valid at the serial output port pin (SO). On the first rising edge of the serial clock (SC), bit 7 is loaded with the value present at the serial data input pin (SI), while bit 6 is presented at the serial output pin (SO). To retrieve the remaining bits seven more rising edges must be generated on the serial clock line. The read operation is destructive. Therefore, if it is desired that the original delay setting remain unchanged, the read data must be written back to the device(s) before the enable (AE) pin is brought low.

The SO pin, if unused, must be allowed to float if the device is configured in the serial programming mode.

The serial mode is the *only* mode available on the 8-pin version of the 3D7438, and this mode is *unavailable* on the 14-pin version of the 3D7438.

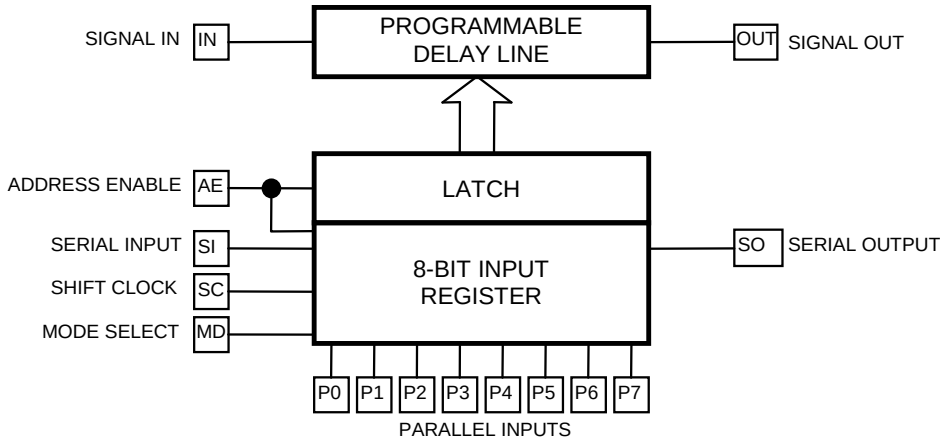


Figure1: Functional block diagram

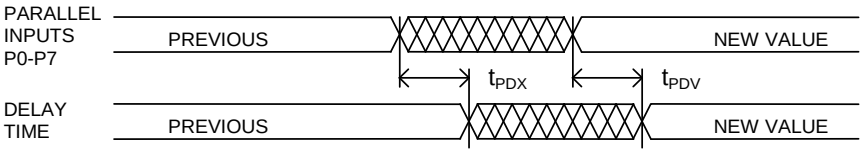


Figure 2: Non-latched parallel mode (MD=1, AE=1)

APPLICATION NOTES (CONT'D)

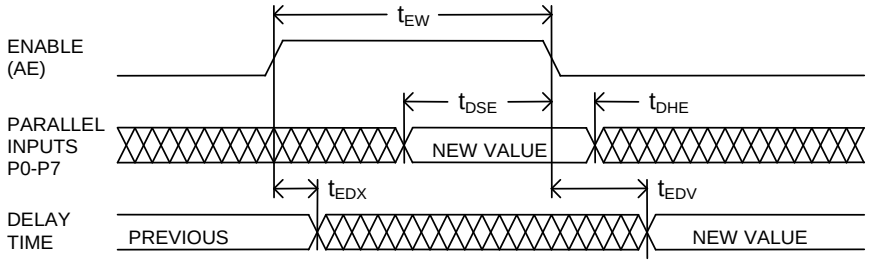


Figure 3: Latched parallel mode (MD=1)

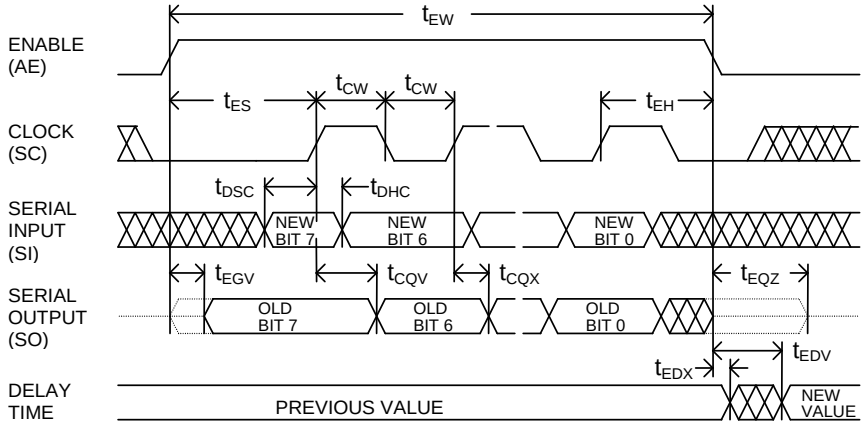


Figure 4: Serial mode (MD=0)

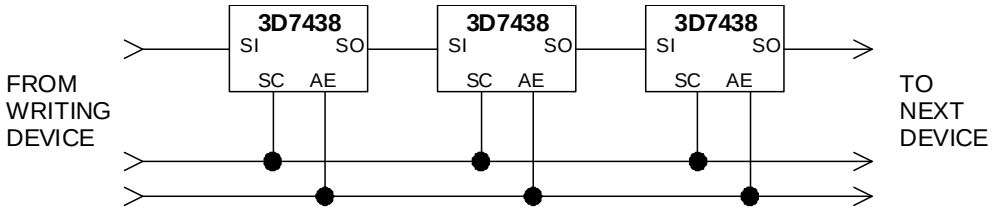


Figure 5: Cascading Multiple Devices

TABLE 2: DELAY VS. PROGRAMMED ADDRESS

	PROGRAMMED ADDRESS								NOMINAL DELAY (NS) PER 3D7438 DASH NUMBER						
PARALLEL	P7	P6	P5	P4	P3	P2	P1	P0							
SERIAL	Msb							Lsb	-50	-75	-100	-125	-150	-200	-250
STEP 0	0	0	0	0	0	0	0	0	7.000	7.000	7.000	7.000	7.000	7.000	7.000
STEP 1	0	0	0	0	0	0	0	1	7.050	7.075	7.100	7.125	7.150	7.200	7.250
STEP 2	0	0	0	0	0	0	1	0	7.100	7.150	7.200	7.250	7.300	7.400	7.500
STEP 3	0	0	0	0	0	0	1	1	7.150	7.225	7.300	7.375	7.450	7.600	7.750
STEP 4	0	0	0	0	0	1	0	0	7.200	7.300	7.400	7.500	7.600	7.800	8.000
STEP 5	0	0	0	0	0	1	0	1	7.250	7.375	7.500	7.625	7.750	8.000	8.250
STEP 253	1	1	1	1	1	1	0	1	19.650	25.975	32.300	38.625	44.950	57.600	70.250
STEP 254	1	1	1	1	1	1	1	0	19.700	26.050	32.400	38.750	45.100	57.800	70.500
STEP 255	1	1	1	1	1	1	1	1	19.750	26.125	32.500	38.875	45.250	58.000	70.750
CHANGE									12.750	19.125	25.500	31.875	38.250	51.000	63.750

DEVICE SPECIFICATIONS

TABLE 3: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-10	10	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 4: DC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		3.0	5.0	mA	Addr = 128
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Input Current	I_{IH}			1.0	µA	$V_{IH} = V_{DD}$
Low Level Input Current	I_{IL}			1.0	µA	$V_{IL} = 0V$
High Level Output Current	I_{OH}		-35.0	-4.0	mA	$V_{DD} = 4.75V$ $V_{OH} = 2.4V$
Low Level Output Current	I_{OL}	4.0	15.0		mA	$V_{DD} = 4.75V$ $V_{OL} = 0.4V$
Output Rise & Fall Time	T_R & T_F		2.0	2.5	ns	C_{LD} = 5 pf

*I_{DD}(Dynamic) = C_{LD} * V_{DD} * F
where: C_{LD} = Average capacitance load/line (pf)
F = Input frequency (GHz)

Input Capacitance = 10 pf typical
Output Load Capacitance (C_{LD}) = 25 pf max

TABLE 5: AC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_C			80	MHz	
Enable Width	t_{EW}	10			ns	
Clock Width	t_{CW}	10			ns	
Data Setup to Clock	t_{DSC}	10			ns	
Data Hold from Clock	t_{DHC}	3			ns	
Data Setup to Enable	t_{DSE}	10			ns	
Data Hold from Enable	t_{DHE}	3			ns	
Enable to Serial Output Valid	t_{EQV}			20	ns	
Enable to Serial Output High-Z	t_{EQZ}			20	ns	
Clock to Serial Output Valid	t_{CQV}			20	ns	
Clock to Serial Output Invalid	t_{CQX}	10			ns	
Enable Setup to Clock	t_{ES}	10			ns	
Enable Hold from Clock	t_{EH}	10			ns	
Parallel Input Valid to Delay Valid	t_{PDV}		20	40	ns	
Parallel Input Change to Delay Invalid	t_{PDX}	0			ns	
Enable to Delay Valid	t_{EDV}		35	45	ns	
Enable to Delay Invalid	t_{EDX}	0			ns	
Input Pulse Width	t_{WI}	40			% of Delay	See Table 1
Input Period	Period	80			% of Delay	See Table 1
Input to Output Delay	t_{PLH}, t_{PHL}				ns	See Table 2

SILICON DELAY LINE AUTOMATED TESTING

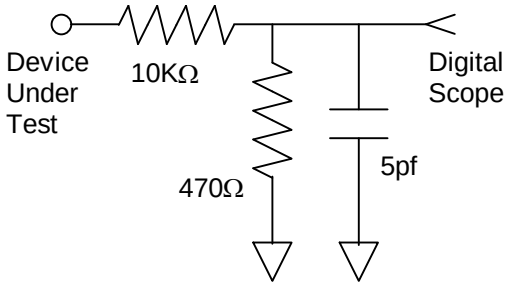
TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (Vcc):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V Low = 0.0V ± 0.1V
Source Impedance:	50Ω Max.
Rise/Fall Time:	3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width:	PW_{IN} = 2 x Max Delay
Period:	PER_{IN} = 10 x Max Delay

OUTPUT:

R_{load}:	10KΩ ± 10%
C_{load}:	5pf ± 10%
Threshold:	1.5V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

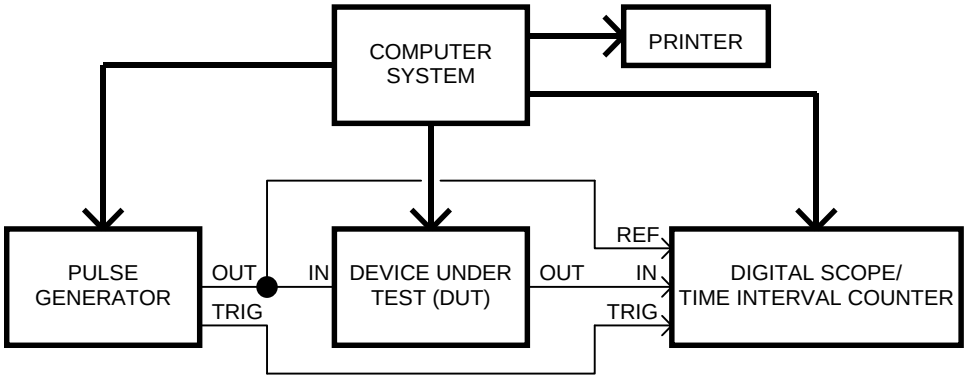


Figure 6: Test Setup

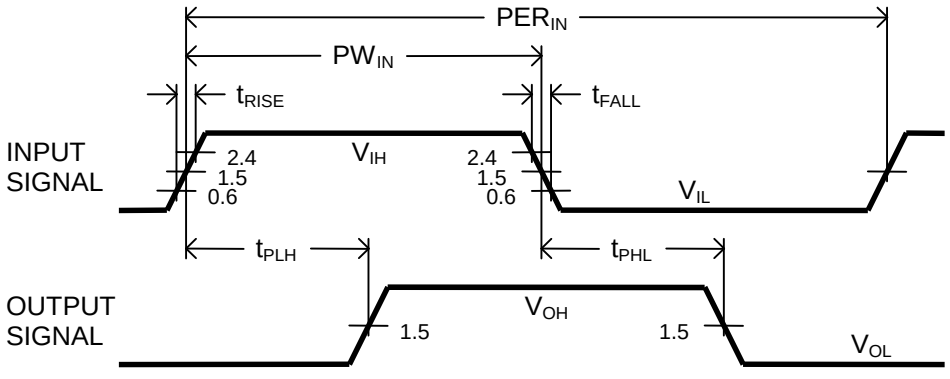


Figure 7: Timing Diagram