NEC
NEC Electronics Inc.

Bi-CMOS-4 ADVANCED PROCESS Bi-CMOS GATE ARRAYS

February 1988

Description

The Bi-CMOS-4 gate arrays feature the high speed of bipolar arrays and the low power dissipation of CMOS devices. NEC has achieved this combination on the same chip, plus latch-up-free operation, by utilizing a 1.6-micron silicon gate CMOS technology and an advanced bipolar process.

The gate array chip (figure 1) is divided into internal and external cell areas. The I/O (interface) cells are in the external cell area. Each internal cell consists of one resistor and 14 transistors: eight n-channel, four p-channel, and two npn bipolar. The internal cell is equivalent to two gates; the external cell is equivalent to one gate.

These application-specific integrated circuits (ASICs) have part numbers in the μPD67000 series. They are available in a variety of sizes (624 to 3140 gates) and packages, including low-cost plastic DIP, PGA, flat, and PLCC.

Gate arrays are intended for customers seeking cost-effective alternatives for VLSI designs. With gate arrays, designers can decrease system form factors by reducing component count and board size while increasing the reliability of their final design.

NEC's gate array program allows a semicustom IC to be developed quickly and reliably at a small fraction of the cost of a full-custom device.

NEC supports its ASIC products with a comprehensive CAD system that significantly reduces the time and expense usually associated with the development of semicustom devices. Advanced CAD tools—such as delay simulation before and after layout, racing check programs, automatic placement and routing, and test program generation—ensure accurate error-free designs.

Features

- ☐ High speed
  - — Internal gate: 0.8 ns (2-input NAND, F/O = 3, L = 3 mm)
  - — Output buffer: 3.0 ns (C_L = 15 pF, I_{OL} = 12 mA)
  - — Input buffer: 1.2 ns (F/O = 3, L = 3 mm)
  - — Toggle frequency: 120 MHz (worst case, F/O = 3, L = 3 mm)
- ☐ Low power
  - — Internal cell: 18 μW/MHz
  - — Output buffer:
    0.43 mW/MHz (C_L = 15 pF, I_{OL} = 12 mA)
    6.3 mW (standby)
  - — Input buffer:
    26 μW/MHz
    0.77 mW (standby)
- ☐ High-drive output blocks
  - — Buffers and inverters
  - — Logic functions (D-F/F, latch, AND, OR, etc)
  - — 12 mA standard
  - — 24 mA high-current version (two external cells)
  - — Bidirectional
  - — Open-collector
  - — Three-state
  - — Optional pull-up or pull-down resistor
- ☐ Input buffers
  - — CMOS level
  - — TTL level
  - — Schmitt trigger
  - — Optional pull-up resistor
- ☐ Large variety of packages
  - — DIP, PPGA, flat, PLCC
  - — 24 to 132 pins
- ☐ Quick turnaround time for prototypes: 8 to 12 weeks
- ☐ Simple interface to customer's logic diagram and test patterns
- ☐ Advanced CAD tools
  - — Delay simulation
  - — Racing check
  - — Automatic placement and routing
  - — Back annotation from layout (post-layout simulation)
  - — Test program generation
- ☐ Direct access to NEC design centers. Each design center is fully equipped with the latest CAD tools and an experieneced staff committed to service.

Figure 1. Chip Layout and Internal Cell Configuration

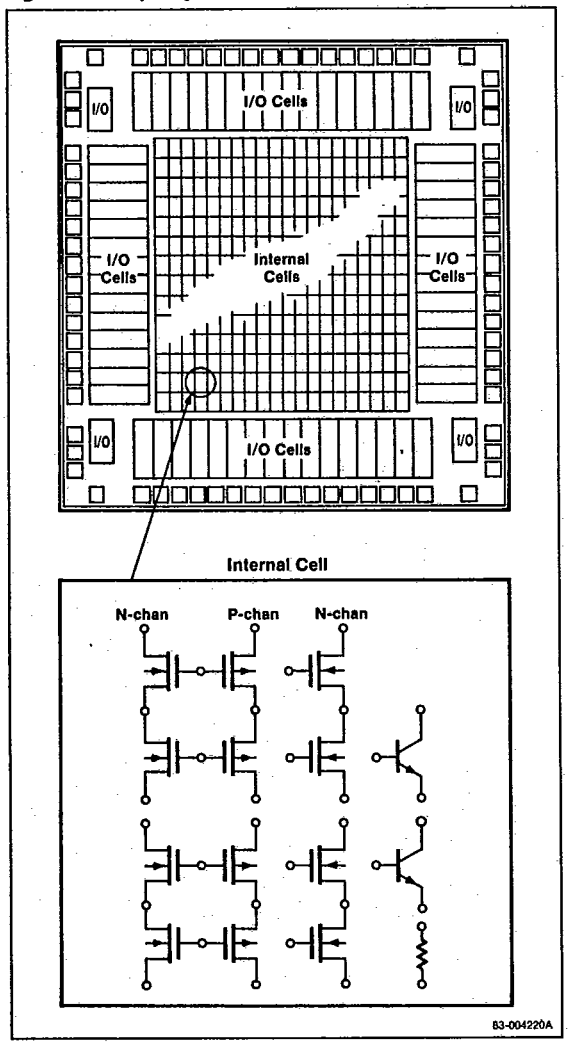
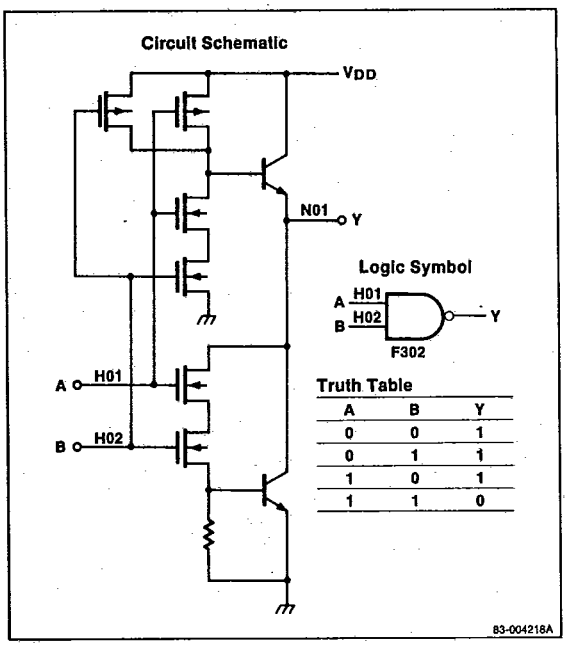


Figure 2. Cell Configured as Two-Input NAND Gate F302



Master Slice Data

T_A = 0 to +85°C

	μPD67001	μPD67010	μPD67020	μPD67030
Gate count	624	1124	2248	3140
Internal cell count	280	520	1064	1500
I/O cell count	64	84	120	140
Internal gate delay (typ)	0.8 ns (2-input NAND; F/O = 3, L = 3 mm)			
Input buffer delay (typ)	1.2 ns (F/O = 3, L = 3 mm)			
Output buffer delay (typ)	3.0 ns (C_L = 15 pF)			
Gate power	18 μW/MHz			
Output buffer power	430 μW/MHz (C_L = 15 pF; I_{OL} = 12 mA) + 6.3 mW (standby)			
Interface	CMOS or ALS-TTL inputs; ALS-TTL outputs			
Power source	5.0 V ±0.5 V; single			

Absolute Maximum Ratings

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to +7.0 V
Output voltage, V_O	−0.5 to +5.5 V
Operating temperature, T_{OPT}	0 to +85 °C
Storage temperature, T_{STG}	−65 to +150 °C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the Recommended Operating Conditions.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power supply voltage	V_{DD}	4.5	5.5	V
High-level input voltage (TTL)	V_{IH}	2.0	V_{DD}	V
Low-level input voltage (TTL)	V_{IL}	0	0.8	V
High-level input voltage (CMOS)	V_{IH}	0.7 V_{DD}	V_{DD}	V
Low-level input voltage (CMOS)	V_{IL}	0	0.3 V_{DD}	V
High-level output current	I_{OH}	−1	—	mA
Low-level output current	I_{OL}	—	12*	mA
Ambient temperature	T_A	0	+85	°C

*Standard output current (24 mA outputs are optional)

DC Characteristics

$V_{DD} = 5.0\ V \pm 0.5\ V$; $T_A = 0$ to +85 °C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input clamp voltage	V_{IC}	−1.5	−0.8	—	V	$I_{IN} = -18$ mA; $V_{DD} = 4.5$ V
High-level output voltage	V_{OH}	2.5	3.4	—	V	$I_{OH} = -1$ mA; $V_{DD} = 4.5$ V
Low-level output voltage	V_{OL}	—	0.3	0.5	V	$I_{OL} = 12$ mA; $V_{DD} = 4.5$ V
High-level output leakage current	I_{OHL}	—	—	100	μA	$V_O = 5.5$ V; $V_{DD} = 5.5$ V
Low-level input current	I_{IL}	−200	—	—	μA	$V_I = 0.4$ V; $V_{DD} = 5.5$ V
High-level input current	I_{IH}	—	—	20	μA	$V_I = 2.7$ V; $V_{DD} = 5.5$ V
Output short-circuit current	I_{OS}	−100	−40	−25	μA	$V_O = 0$ V; $V_{DD} = 5.5$ V
High-Z output leakage current	I_{OZ}	−20	—	20	μA	$V_{OH} = 2.7$ V; $V_{OL} = 0.4$ V; $V_{DD} = 5.5$ V
Input threshold voltage	V_{TH}	—	1.5	—	V	TTL level
		—	2.5	—	V	CMOS level
Positive Schmitt trigger input voltage	V_{THP}	1.6	1.8	2.0	V	TTL level; $V_{DD} = 5$ V
		2.6	2.8	3.0	V	CMOS level; $V_{DD} = 5$ V
Negative Schmitt trigger input voltage	V_{THN}	0.7	1.0	1.3	V	TTL level; $V_{DD} = 5$ V
		1.7	2.0	2.3	V	CMOS level; $V_{DD} = 5$ V
Hysteresis voltage	V_H	0.4	0.8	1.1	V	TTL level
		0.4	0.8	1.1	V	CMOS level
Pull-up or pull-down resistor	R	25	50	75	kΩ	

AC Characteristics

$V_{DD} = 5.0\ V \pm 0.5\ V$; $T_A = 0$ to +85 °C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Internal gate delay	t_{PD}	0.48	0.80	1.46	ns	2-input NAND; F/O = 3, L = 3 mm
Toggle frequency	f_{TOG}	120	200	—	MHz	F/O = 3, L = 3 mm
Input buffer delay	t_{PD}	0.7	1.2	2.2	ns	F/O = 3, L = 3 mm
Output buffer delay	t_{PD}	1.8	3.0	5.4	ns	$C_L = 15$ pF, $I_{OL} = 12$ mA
		2.6	4.3	7.7	ns	$C_L = 50$ pF, $I_{OL} = 12$ mA
Maximum output buffer operating frequency	f_{MAX}	100	160	—	MHz	$C_L = 15$ pF
		40	80	—	MHz	$C_L = 50$ pF
Output buffer rise time	t_R	2.3	3.8	6.8	ns	$C_L = 15$ pF
Output buffer fall time	t_F	1.6	2.6	4.7	ns	$C_L = 15$ pF

Figure 3. Example of a Circuit Diagram

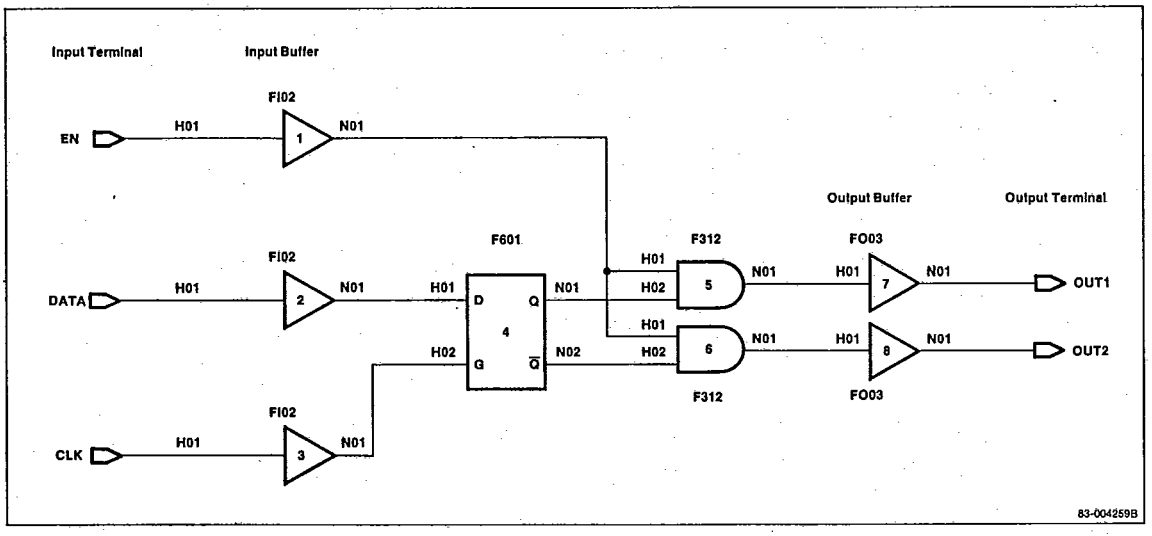
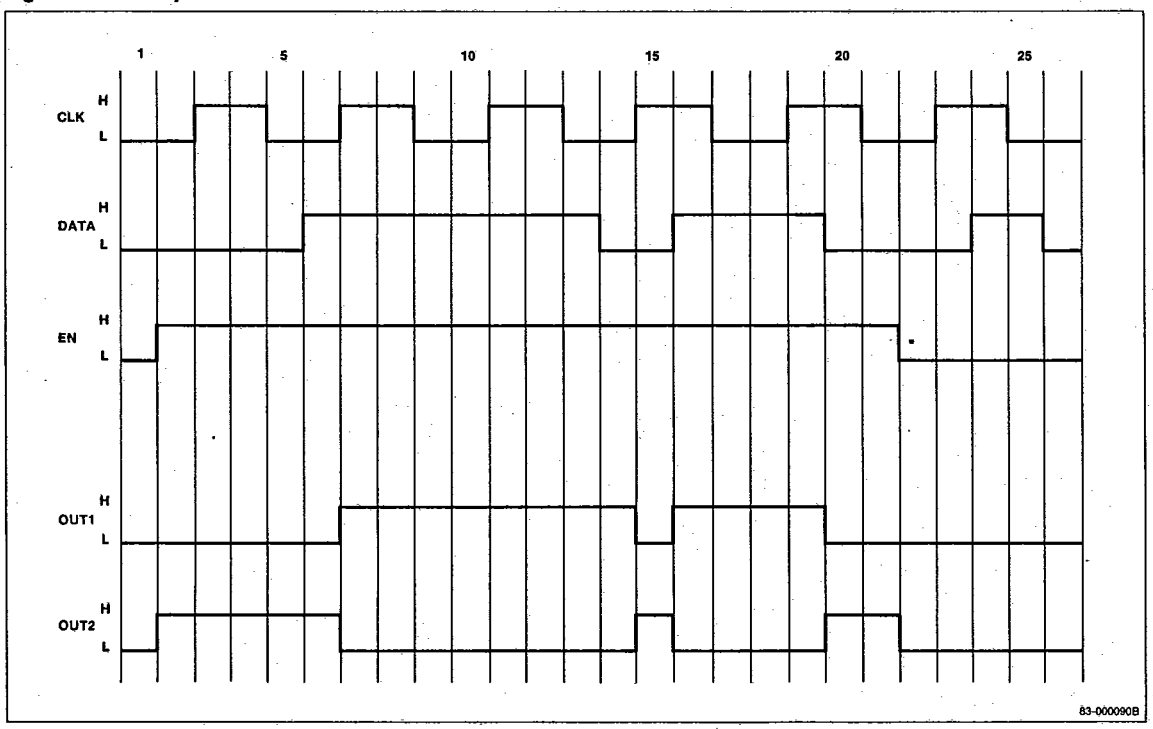


Figure 4. Example of a Test Pattern Chart



Development Procedure

The semicustom approach of gate arrays offers a unique and effective method of manufacturingg ICs at reduced cost and development time. NEC makes this possible by stocking wafers that are completely fabricated except for the final step of interconnection. This provides a designer the freedom of interconnecting the uncommitted components to achieve a unique circuit configuration.

Essential Documents

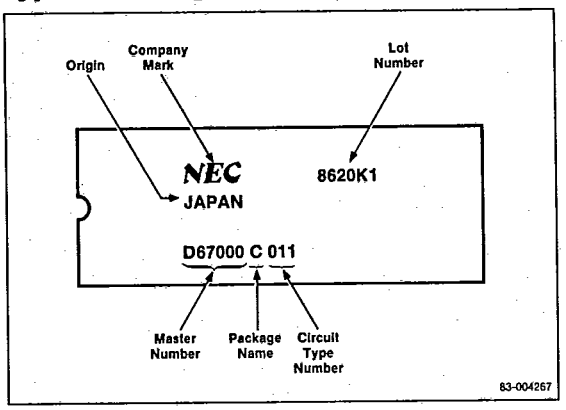
- ☐ Contract and nondisclosure agreement
- ☐ Circuit diagram based on the NEC Block Library
- ☐ Interconnection data file (LOGINC)
- ☐ Test pattern data file (LOGPAT)
- ☐ Pin assignment (if required)
- ☐ Critical path identification (if required)
- ☐ Design specification form

Package Availability

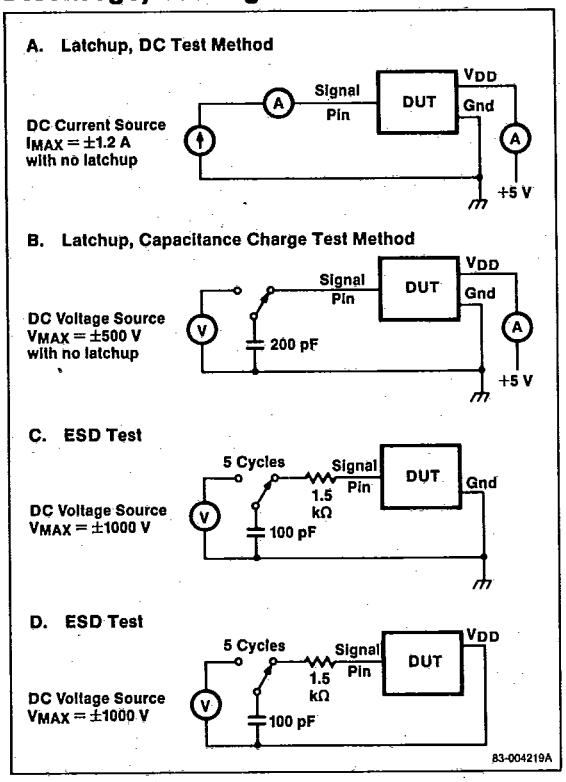
	μPD67001	μPD67010	μPD67020	μPD67030
Plastic DIP				
24-pin (600 mil)	A	A	—	—
28-pin (600 mil)	A	A	A	A
40-pin (600 mil)	A	A	A	A
48-pin (600 mil)	A	A	A	A
64-pin shrink (750 mil)	A	A	A	A
Plastic flatpack				
44-pin	A	A	—	—
52-pin	A	A	A	A
64-pin	A	A	A	A
80-pin	—	A	A	A
100-pin	—	—	A	A
120-pin	—	—	—	U
Plastic leaded chip carrier (PLCC)				
28-pin	A	—	—	—
44-pin	A	A	—	—
52-pin	A	A	A	U
68-pin	A	A	U	U
84-pin	—	—	U	U
Plastic pin grid array (PPGA)				
72-pin	—	A	A	A
132-pin	—	—	A	A
Ceramic pin grid array (CPGA)				
72-pin	—	A	A	A
132-pin	—	—	A	A

A = available now; U = under development

Typical Package Marking



Latchup and ESD (Electrostatic Discharge) Testing



Block Library List

Interface Blocks

Function	Block Type	Description (Note 1)
Input block	FI01	Buffer, CMOS-level
	FI02	Buffer, TTL-level
	M043	Inverter, CMOS-level
	M010	Inverter, TTL-level
	FIS1	Buffer, CMOS-level Schmitt
	FIS2	Buffer, TTL-level Schmitt
	M053	Inverter, CMOS-level Schmitt
	M033	Inverter, TTL-level Schmitt
	FIU1	Buffer, CMOS-level; 50-kΩ pullup
	FIU2	Buffer, TTL-level; 50-kΩ pullup
	M048	Inverter, CMOS-level; 50-kΩ pullup
	M018	Inverter, TTL-level; 50-kΩ pullup
	FUS1	Buffer, CMOS-level Schmitt; 50-kΩ pullup
	FUS2	Buffer, TTL-level Schmitt; 50-kΩ pullup
	M058	Inverter, CMOS-level Schmitt; 50-kΩ pullup
	M038	Inverter, TTL-level Schmitt; 50-kΩ pullup
Output block, totem-pole (I_{OL} = 12 mA)	F003	Buffer
	B101	Inverter
	B011	2-input AND
	B151	4-input OR
	B152	2-wide, 2-2-input OR-AND
	B153	D-latch with R-bar
	B154	2-input NOR
	B010	2-input NAND
	B159	2-input OR
Output block, open-collector (I_{OL} = 12 mA)	EXT5	Buffer
	B102	Inverter
	B035	2-input AND
	B251	4-input OR
	B252	2-wide, 2-2-input OR-AND
	B253	D-latch with R-bar
	B254	2-input NOR
	B036	2-input NAND
	B259	2-input OR
	EXT7	Buffer; 5-kΩ pullup
	B302	Inverter; 5-kΩ pullup
	B087	2-input AND; 5-kΩ pullup
	B351	4-input OR; 5-kΩ pullup
	B352	2-wide, 2-2-input OR-AND; 5-kΩ pullup
	B353	D-latch with R-bar; 5-kΩ pullup
	B354	2-input NOR; 5-kΩ pullup
	B088	2-input NAND; 5-kΩ pullup
	B359	2-input OR; 5-kΩ pullup
Output block, three-state (I_{OL} = 12 mA)	B009	Buffer
	B103	Inverter
	B165	2-input AND
	B452	2-wide, 2-2-input OR-AND
	B454	2-input NOR
	B166	2-input NAND
	B459	2-input OR
	B0D9	Buffer; 50-kΩ pulldown
	B556	Inverter; 50-kΩ pulldown
	B557	2-input AND; 50-kΩ pulldown
	B552	2-wide, 2-2-input OR-AND; 50-kΩ pulldown
	B554	2-input NOR; 50-kΩ pulldown
	B558	2-input NAND; 50-kΩ pulldown
	B559	2-input OR; 50-kΩ pulldown
	B0U9	Buffer; 50-kΩ pullup
	B656	Inverter; 50-kΩ pullup
	B657	2-input AND; 50-kΩ pullup
	B652	2-wide, 2-2-input OR-AND; 50-kΩ pullup
	B654	2-input NOR; 50-kΩ pullup
	B658	2-input NAND; 50-kΩ pullup
	B659	2-input OR; 50-kΩ pullup
Bidirectional block, totem-pole (I_{OL} = 12 mA)	B005	Buffer, CMOS level in
	B006	Buffer, TTL level in
	BA04	Inverter, CMOS level in
	BA12	Inverter, TTL level in
	BA05	2-input AND, CMOS level in
	BA02	2-input AND, TTL level in
Bidirectional block, open-collector (I_{OL} = 12 mA)	BA09	Buffer, CMOS level in
	BA06	Buffer, TTL level in
	BA10	Inverter, CMOS level in
	BA07	Inverter, TTL level in
	BA11	2-input AND, CMOS level in
	BA08	2-input AND, TTL level in
Output block, high-current (I_{OL} = 24 mA)	T001	Buffer, totem-pole
	T101	Inverter, totem-pole
	T002	Buffer, open-collector
	T102	Inverter, open-collector
	T402	Buffer, open-collector; 2.5-kΩ pullup
	T302	Inverter, open-collector; 2.5-kΩ pullup
	T003	Buffer, 3-state
	T103	Inverter, 3-state
	T555	Buffer, 3-state; 50-kΩ pulldown
	T556	Inverter, 3-state; 50-kΩ pulldown
	T655	Buffer, 3-state; 50-kΩ pullup
	T656	Inverter, 3-state; 50-kΩ pullup

Notes:

(1) Each interface block has one I/O cell except the high-current (24 mA) output blocks have two.

(2) Symbols:

EN	Enable
R	Reset
S	Set
-bar	Active low

Internal Blocks

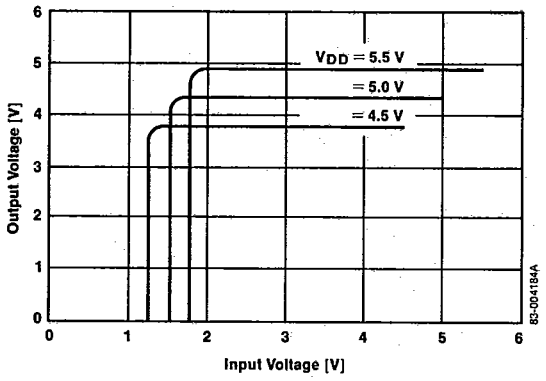
Function	Block Type	Description	Cells
Inverter	F101	Inverter	1
	F120	Dual inverter; high fan-out	2
Buffer	F111	Noninverting buffer	1
	F121	Dual noninverting buffer; high fan-out	2
NOR	F202	2-input NOR	1
	F203	3-input NOR	1
	F204	4-input NOR	1
	F208	8-input NOR	4
OR	F212	2-input OR	1
	F213	3-input OR	2
	F214	4-input OR	2
NAND	F302	2-input NAND	1
	F303	3-input NAND	1
	F304	4-input NAND	1
	F305	5-input NAND	3
	F306	6-input NAND	3
	F308	8-input NAND	3
AND	F312	2-input AND	1
	F313	3-input AND	2
	F314	4-input AND	2
AND-NOR	F421	2-wide, 1-2-input AND-NOR	1
	F422	3-wide, 1-1-2-input AND-NOR	1
	F423	2-wide, 1-3-input AND-NOR	1
	F424	2-wide, 2-2-input AND-NOR	1
	F425	3-wide, 2-2-2-input AND-NOR	2
	F426	2-wide, 3-3-input AND-NOR	2
	F429	4-wide, 2-2-2-2-input AND-NOR	4
	F442	2-wide, 4-4-input AND-NOR	2
OR-NAND	F431	2-wide, 1-2-input OR-NAND	1
	F432	3-wide, 1-1-2-input OR-NAND	1
	F433	2-wide, 1-3-input OR-NAND	1
	F434	2-wide, 2-2-input OR-NAND	1
	F435	2-wide, 2-3-input OR-NAND	2
	F436	2-wide, 3-3-input OR-NAND	2
	F454	4-wide, 2-2-2-2-input OR-NAND	4

Function	Block Type	Description	Cells
Clock driver	F501	Single driver	2
	F502	Dual driver	4
Exclusive-OR	F511	2-input XOR	2
	F513	2-wide, 2-2-input AND-XOR	3
Exclusive-NOR	F512	2-input XNOR	2
	F514	2-wide, 2-2-input AND-XNOR	3
Adder	F521	Full-adder	5
3-state buffer	F531	3-state buffer with EN	2
	F532	3-state buffer with EN-bar	2
Decoder	F561	2-to-4 decoder	4
	F981	2-to-4 decoder with EN-bar	6
	F982	3-to-8 decoder with EN-bar	10
	F983	1-to-2 decoder with EN	3
	F984	1-to-4 decoder with EN-bar	6
	F987	4-to-10 decoder with EN-bar	27
	F988	1-to-8 decoder with EN-bar	12
Multiplexer	F569	8-to-1 multiplexer with EN-bar	9
	F570	4-to-1 multiplexer with EN-bar	4
	F571	2-to-1 multiplexer with EN-bar	2
Latch	F595	R-S latch	2
	F601	D-latch	2
	F603	D-latch with R-bar	2
	F901	4-bit latch	8
Flip-flop	F635	D-F/F with R-bar	4
	F641	D-F/F	3
	F644	D-F/F with S- and R	5
	F645	D-F/F with R-bar	4
	F617	D-F/F with S- and R-bar	4
	F647	D-F/F with S- and R-bar	5
	F650	D-F/F with 2-to-1 data selector	4
	F744	Toggle F/F with S and R	5
	F765	Toggle F/F with R-bar	4
	F791	Toggle F/F with S, R, and EN	5
	F771	J-K F/F	5
	F778	J-K F/F with S and R	5
Miscellaneous	F091	High- and low-level generator	1
	S000	D-F/F for scan path tests	5
	F581	8-bit odd-parity generator	11
	F582	8-bit even-parity generator	11
	BUSA	Bus array	—

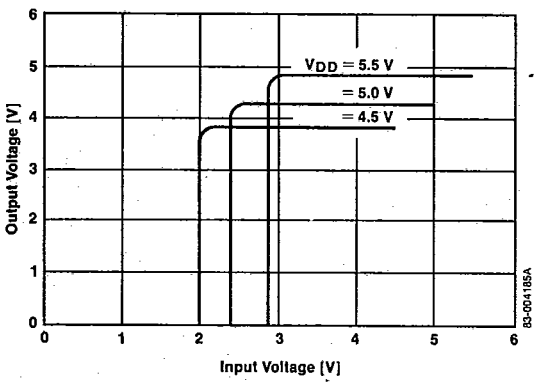
Operating Characteristics

Input Buffers; Output Voltage vs Input Voltage

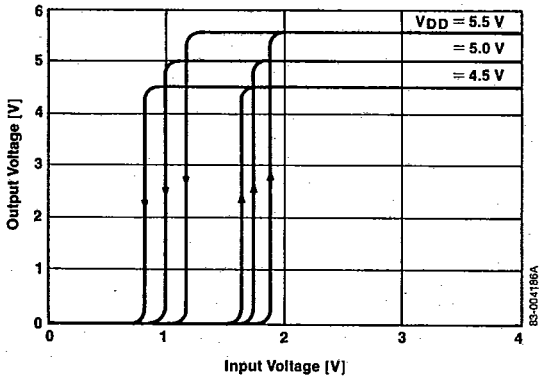
Normal TTL Level



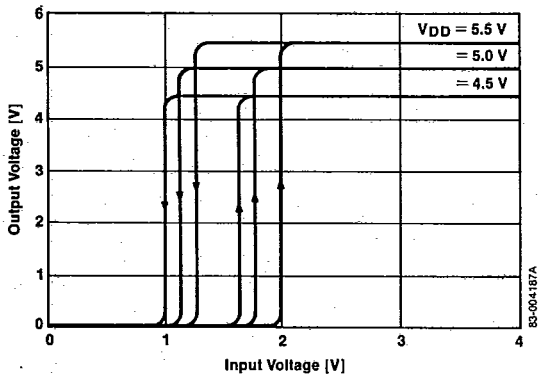
Normal CMOS Level



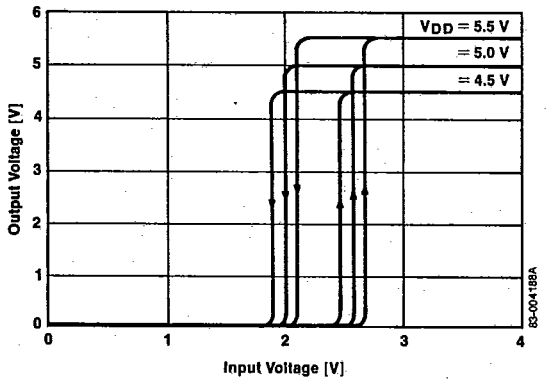
TTL-Level Schmitt Trigger; $T_A = 0°C$



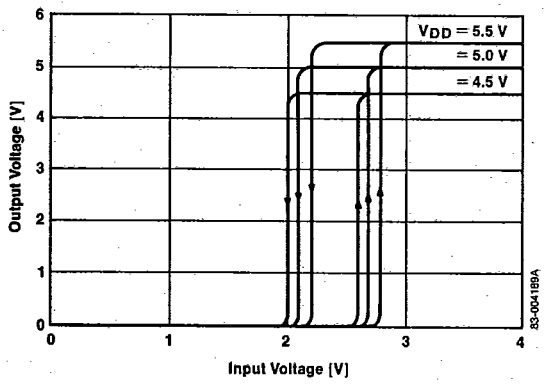
TTL-Level Schmitt Trigger; $T_A = +85°C$



CMOS-Level Schmitt Trigger; $T_A = 0°C$

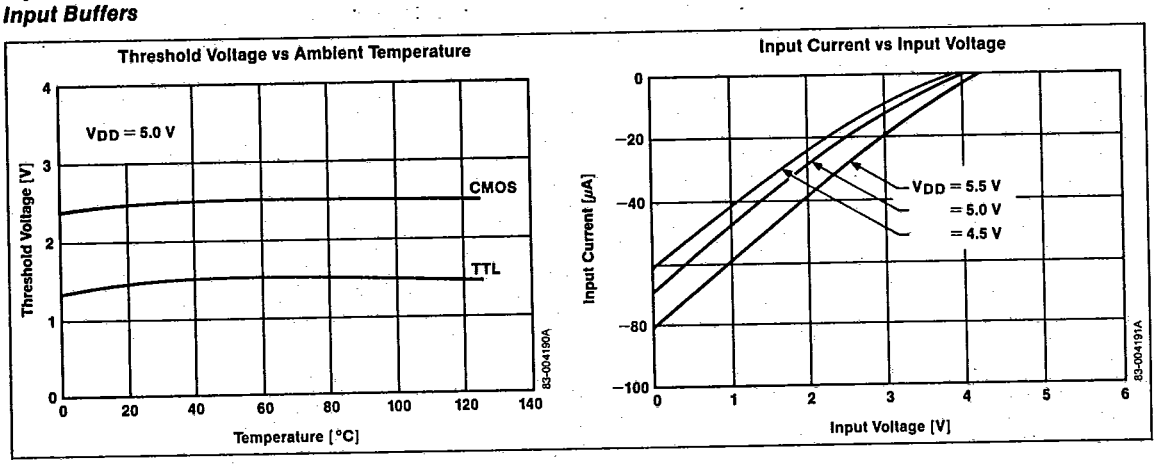


CMOS-Level Schmitt Trigger; $T_A = +85°C$

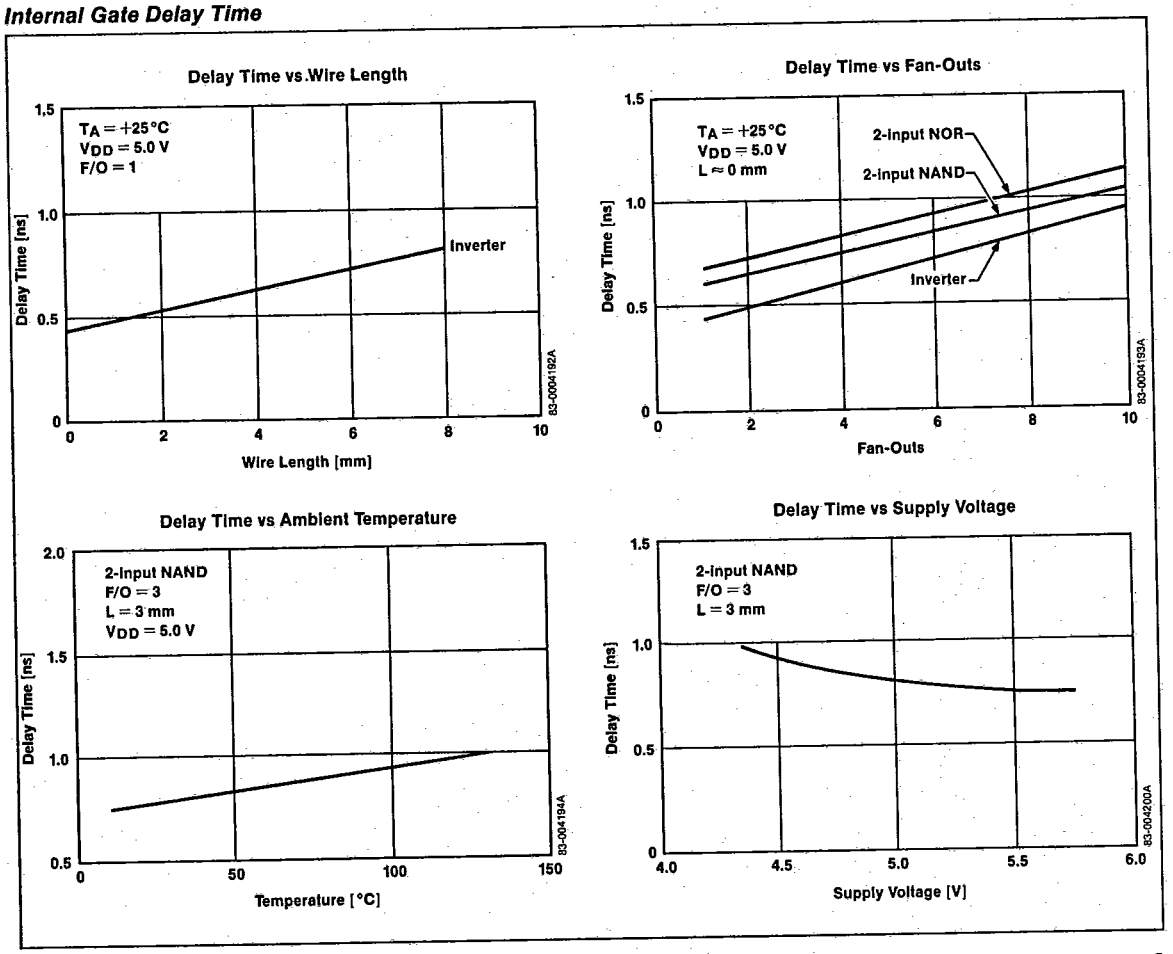


Operating Characteristics (cont)

Input Buffers

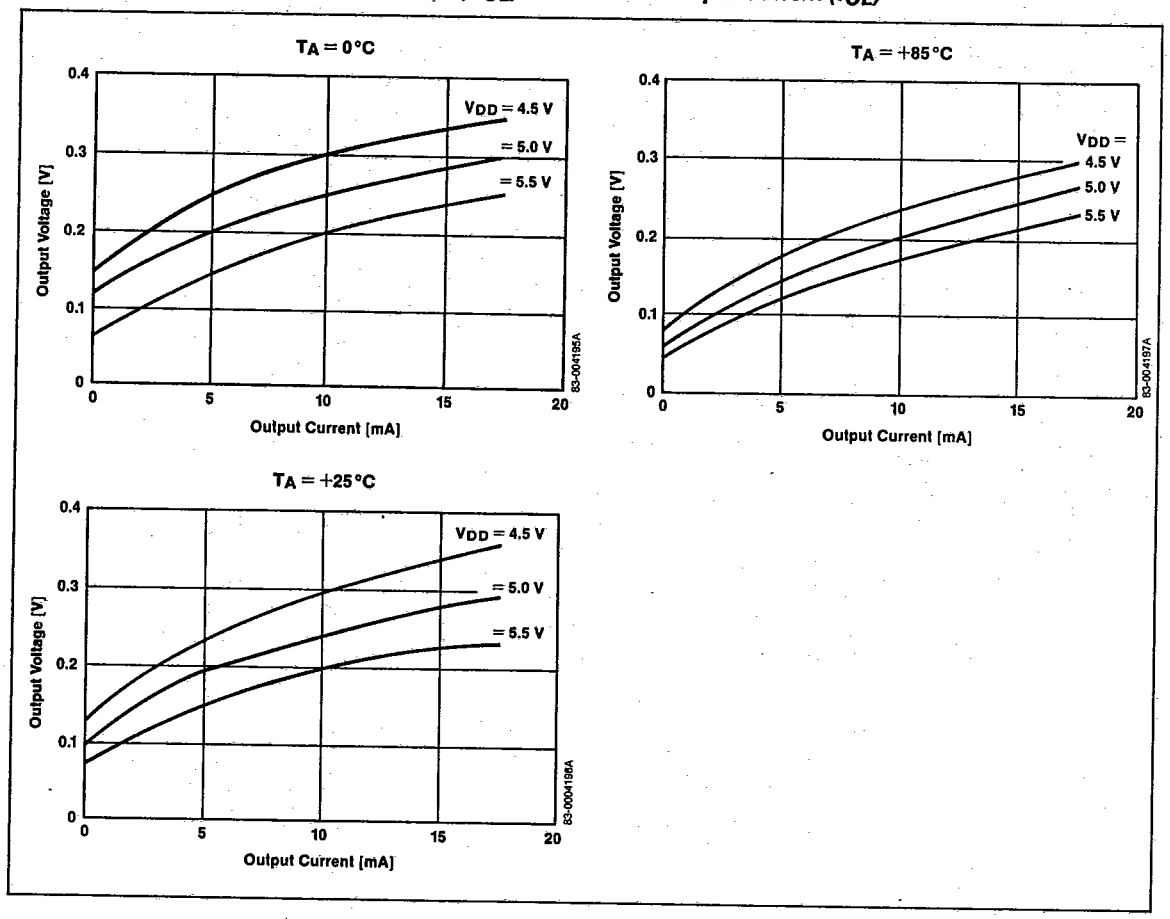


Internal Gate Delay Time



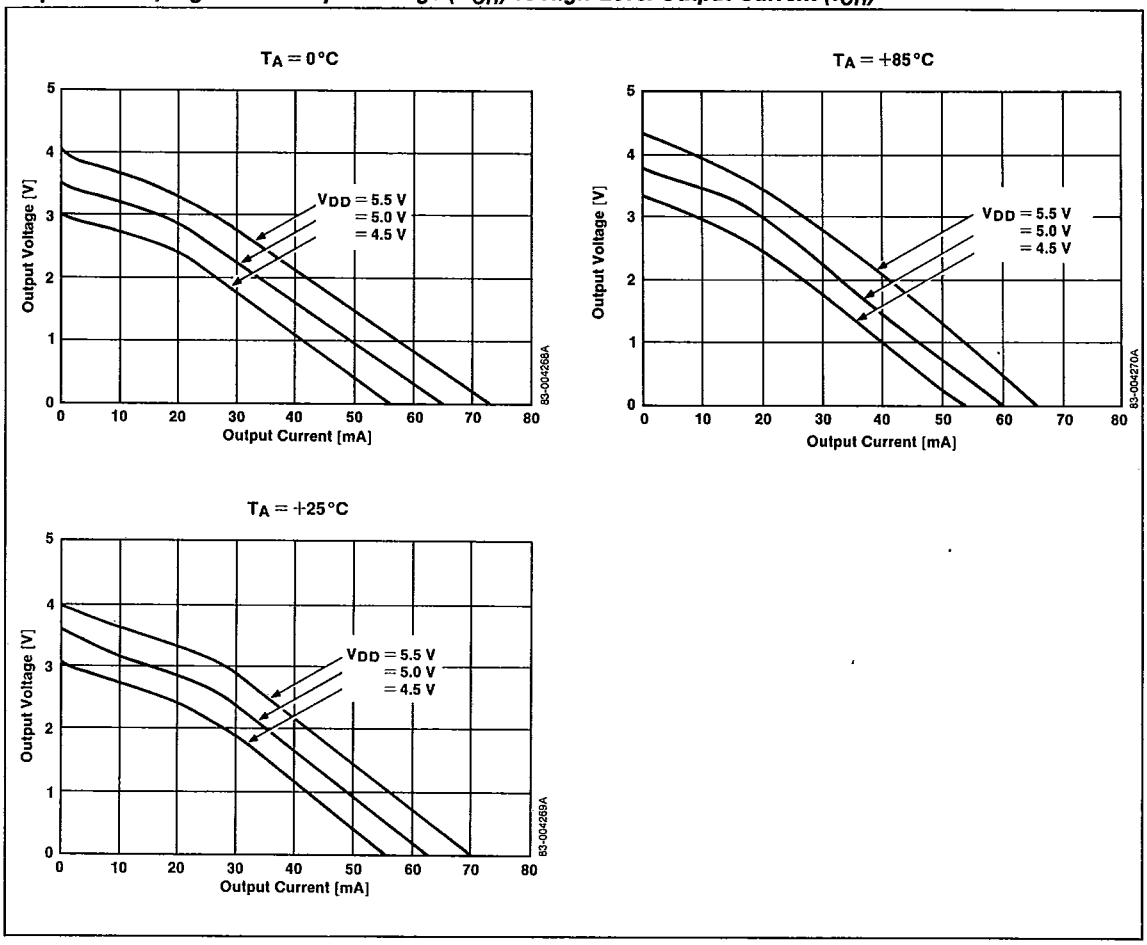
Operating Characteristics (cont)

Output Buffers; Low-Level Output Voltage (V_{OL}) vs Low-Level Output Current (I_{OL})



Operating Characteristics (cont)

Output Buffers; High-Level Output Voltage (V_{OH}) vs High-Level Output Current (I_{OH})



Output Buffers; Rise Time, Fall Time, and Delay Time