HIGH-VOLTAGE MIXED-SIGNAL IC

UC1602i

65x102 Matrix LCD Controller-Driver

Product Specifications
Revision 0.54

OCT 12, 2001

ULTRACHIP
The Coolest LCD Driver. Ever!!

UC1602i

Single-Chip, Ultra-Low Power
Passive Matrix LCD Controller-Driver

INTRODUCTION

UC1602i is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

In addition to low power column and row drivers, these ICs contain all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones or Smart Phones
- Pagers or other battery operated messaging devices
- Battery Powered Portable Instruments

FEATURE HIGHLIGHTS

- Supports I^2C 2-wire serial interface and 8-bit parallel bus interface.
- Ultra-low power LCD controller-driver with built-in display RAM and timing generator to support compact LCD module using as few as 5 pins.
- $V_{DD2/3}$ voltage range: 2.4V ~ 3.3V
  V_{DD1} voltage range: 1.8V ~ 3.3V
  LCD V_{OP} range: 4.5V ~ 10.5V
- 6x, built-in self-configuring, charge pump allows the use of low V_{DD} while produce high V_{LCD} for driving LCD.
- On-chip charge pump pumping capacitors requires only 3 external capacitors.
- Two multiplexing rates: 1/65, 1/49.
- Four temperature compensations.
- Support both high speed parallel interfaces and compact serial interfaces.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.

POWER CONSUMPTION

Symbol	Conditions				Typ.	Max.	Unit
	V_{DD} : V_{LCD}	Pump	Display pattern	LCD loading			
$I_{DD(tot)}$	2.7V : 8.5V	4x	Blank	65x102, 12nF Panel [$]	95		μA
	2.7V : 8.5V	4x	Checker		105		
	2.4V : 8.5V	5x	Blank		110		
	2.4V : 8.5V	5x	Checker		122		
	2.7V : 8.5V	4x	Blank/Checker	No load	65		
	2.4V : 8.5V	5x	Blank/Checker		70		
	Sleep Mode (Display Off)			N/A	0.2	1	

[$] LCD panel capacitance estimated when displaying checker pattern.

ORDERING INFORMATION

Nomenclature	Description
UC1602I-PP-M	PP: Packaging GU: Gold bumped, face up GD: Gold bumped, face down F*n*: Type *n* TCP film

Part Number	Memory	Drivers	Mux Rate Supported	Versions
UC1602I	65 x 102	65 COM x 102 SEG	1/65, 1/49	G

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

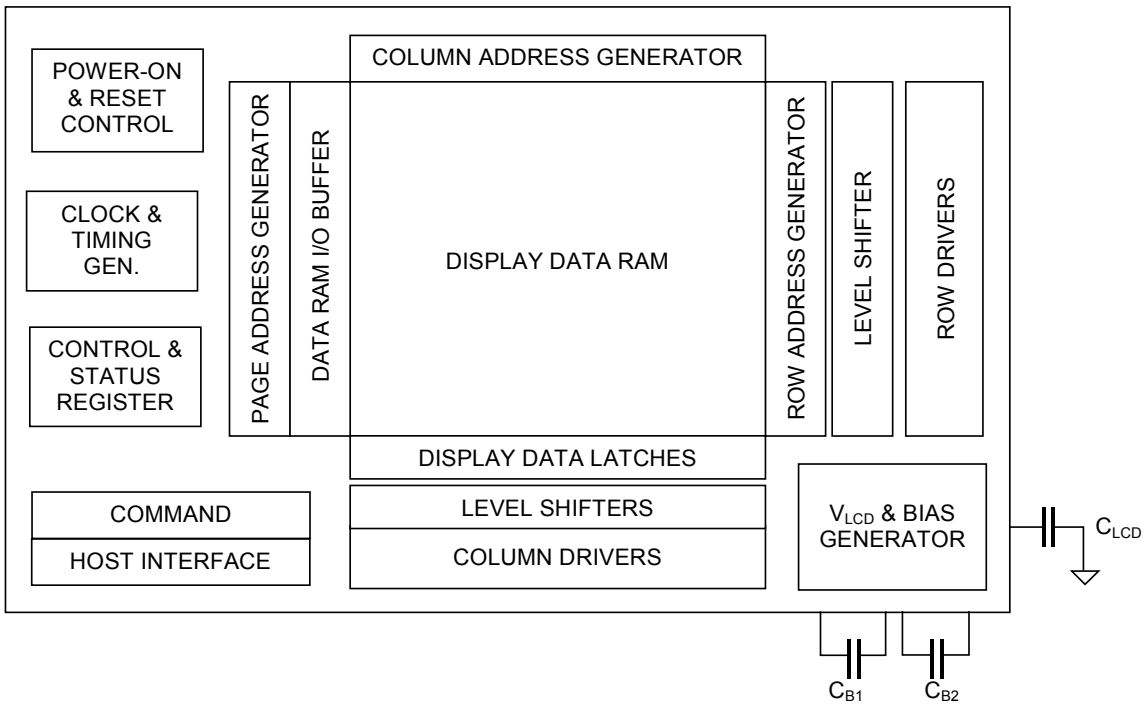
BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of UltraChip's delivery. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and quality their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	Pins	Description
			MAIN POWER SUPPLY
V_{DD1} V_{DD2} V_{DD3}	PWR		V_{DD1} supplies for display data RAM and digital logic, V_{DD2} supplies for V_{LCD}/V_B generator, V_{DD3} supplies for V_{REF} and other analog circuits. V_{DD2}/V_{DD3} should be connected to the same power source. But V_{DD1} can be connected to a source voltage no higher than V_{DD2}/V_{DD3}. In COG applications, always use separate ITO traces for V_{DD1}, V_{DD2} and V_{DD3} to reduce noise coupling.
V_{SS} V_{SS2}	GND		Ground. In COG applications, use separate ITO traces to connect V_{SS} and V_{SS2} to the separate GND pins or to the shared GND pin and minimize both ITO resistance.
			LCD POWER SUPPLY
V_{B1+} V_{B1-} V_{B0-} V_{B0+}	PWR		LCD Offset Voltages. Connect two C_B capacitors between V_{B+} to V_{B0+} and V_{B0-} to V_{B-}. For optimum operation result, minimize the ITO trace resistance of these nodes. Place C_{B1} and C_{B0} on the FPC or COF to reduce I/O pin count by 4.
V_{LCD-IN} $V_{LCD-OUT}$	PWR		Main LCD Power Supply. When internal V_{LCD} is used, connect these pins together. When external V_{LCD} source is used, connect external V_{LCD} source to V_{LCD-IN} pins and leave $V_{LCD-OUT}$ pins open. A by-pass capacitor C_L should be connected between V_{LCD} and V_{SS2}. Minimize the ITO trace resistance in COG applications.

NOTE

- Recommended capacitor values:
  C_B: 150~500x LCD load capacitance or 1.0uF (V_{BR} > 3V), whichever is higher.
  C_L: 20~50x LCD load capacitance or 0.2uF (V_{BR} > V_{LCD}+1V), whichever is higher.

Name	I/O	Pins	Description
			LCD DRIVE OUTPUT (UP TO 198 PINS)
C0, ~ C101	HV		LCD column driver outputs. Support up to 102 columns. Leave unused drivers open-circuit.
RIC	HV		LCD icon driver outputs. RIC has two pads. These two pads are used to drive icons. Leave unused drivers open-circuit.
R1, R3, ... R63 R2, R4, …	HV		LCD row driver outputs. Support up to 64 rows. Drivers for even and odd row are group into two separate groups along the two sides of the IC. Leave unused drivers open-circuit.

Name	I/O	Pins	Description
R64			

<table>
<tr><th>Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td colspan="4">CONFIGURATION PINS</td></tr>
<tr><td>PS[1:0]</td><td>C</td><td></td><td>Parallel/Serial.
Serial modes: “LL”: serial (S8) “LH”: 2-wire serial (I^2C)
Parallel modes: “HL”: 8080 “HH”: 6800</td></tr>
<tr><td>V_{DD1}</td><td>S</td><td></td><td>For configuration purpose</td></tr>
<tr><td colspan="4">TEST PINS</td></tr>
<tr><td>TP3</td><td>I</td><td></td><td>Test control. Connect to GND.</td></tr>
<tr><td>TP[2:0]</td><td>I</td><td></td><td>Test control. Leave these pins open during normal use.</td></tr>
<tr><td>TST[3:1]</td><td>I/O</td><td></td><td>Test I/O pins. Leave these pins open during normal use.</td></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>V_{DD1}</td><td>S</td><td></td><td>Use for configuration purpose.</td></tr>
<tr><td>CS0/A0
CS1/A1</td><td>I</td><td></td><td>Chip Select or Chip Address. In parallel mode and S8 mode, chip is selected when CS0=”L” and CS1=”H”.
In I^2C mode, A[1:0] specifies bit 3~2 of UC1602I’s device address.
When the chip is not selected, D[7:0] will be high impedance.</td></tr>
<tr><td>RST</td><td>I</td><td></td><td>When RST=”L”, all control registers are re-initialized by their default states and/or by their pin configurations if applicable.
When RST is not used, connect the pin to V_{DD1}.</td></tr>
<tr><td>CD</td><td>I</td><td></td><td>Select Control data or Display data for read/write operation. CD pin is not used in I^2C modes, connect it to V_{DD} or V_{SS}.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td></td><td>WR[1:0] controls the read/write operation of the host interface.
In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode.
In serial interface modes, these two pins are not used. Connect to V_{SS}.</td></tr>
<tr><td>D0~D7</td><td>I/O</td><td></td><td>Bi-directional bus for both serial and parallel host interfaces.
In S8 mode, connect unused pins to V_{DD} or V_{SS}. In I2C mode, connect D[1:0] to SCK, and D[5:2] to SDA, and D[7:6] to V_{DD} or V_{SS}.
<table>
<tr><th></th><th>PS=1x</th><th>PS=0x</th></tr>
<tr><td>D0</td><td>D0</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td></td></tr>
<tr><td>D2</td><td>D2</td><td></td></tr>
<tr><td>D3</td><td>D3</td><td>SDA</td></tr>
<tr><td>D4</td><td>D4</td><td></td></tr>
<tr><td>D5</td><td>D5</td><td></td></tr>
<tr><td>D6</td><td>D6</td><td>-</td></tr>
<tr><td>D7</td><td>D7</td><td>-</td></tr>
</table>
In I^2C mode, SDA and SCK are in open-drain mode. Pull up resistors are required on the bus. In COG applications, be careful to control ITO trace resistance, as it will affect effective output level of SDA.</td></tr>
</table>

NOTE

- Unless otherwise specified, connect all unused input pins and control pins to V_{SS}.

CONTROL REGISTERS

UC1602I contains registers which controls the chip operation. These registers can be modified by commands. The commands supported by UC1602I are described in the next section.

Name: The Symbolic reference of the register byte.
Note that, some symbol names refers to collection of bits (flags) within one register byte.

Default: Value after *Power-up-Reset* and *System-Reset*.
"PIN" means default value depends on the connection of associated configuration pin(s).

Name	Bits	Default	Description
MR	1	1H	Multiplexing Rate: Number of pixel rows plus icon row. 0: 49 1: 65
SL	6	0H	Start Line. Mapping from Row0 to Display Data RAM.
CR	8	0H	Return Column Address.
CA	8	0H	Display Data RAM Column Address (Used in Host to Display Data RAM access)
PA	4	0H	Display Data RAM Page Address (Used in Host to Display Data RAM access)
BR	2	2H	Bias Ratio. The ratio between V_{LCD} and V_D.
TC	2	0H	Temperature Compensation (per ^oC). 00: 0.0% 01: -0.05% 10: -0.1% 11: -0.2%
GN	2	3H	Gain = V_D / V_{PM}
PM	6	10H	Electronic Potential Meter to generate V_{PM} from V_{REF}
OM	2	0	Operating Modes 10: Sleep 11: Normal 01: (Not used) 00: Reset
BZ	1	–	Busy with internal processes (reset, changing mode, etc.) OK for Display RAM read/write access.
RS	1		Reset in progress, Host Interface not ready
PC	3	07H	Power Control. PC[0] 0: LCD load < 12nF 1: LCD load > 12nF PC[2:1] 00: External V_{LCD} 01: 4x Pump 10: 5x Pump 11: 6x Pump
APC0	8	6CH	Advanced Program Control. Default value should work fine.

Name	Bits	Default	Description
DC	3	0H	Display Control: DC[0]: PXV: Pixels Inverse DC[1]: APO: All Pixels ON DC[2]: DE, Display Enable
AC	4	0H	Address Control: AC[0]: WA: Automatic column/page Wrap Around AC[1]: Reserved (always set to 0) AC[2]: PID: PA (page address) auto increment direction (L:+1 H:-1) AC[3]: CUM: Cursor update mode, when CUM=1, CA increment on write only, wrap around suspended
LC	4	 0 0 0 0	LCD Layout Control: LC[0]: MSF: MSB First mapping Option LC[1]: Reserved (always set to 0) LC[2]: MX, Mirror X (Column sequence inversion) LC[3]: MY, Mirror Y (Row sequence inversion)

COMMANDS

The following is a list of host commands support by UC1062I.

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle

\# Useful Data bits
– Don't Care

Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action
Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte @ PA/CA
Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte @ PA/CA
Get Status	0	1	BZ	MX	DE	RS	0	0	0	0	Get Status Summary
Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]=D[3:0]
Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4] =D[3:0]
Set Mux rate & Temperature Compensation.	0	0	0	0	1	0	0	#	#	#	Set MR=D[2] Set TC[1:0]=D[1:0]
Set Power Control	0	0	0	0	1	0	1	#	#	#	Set PC[2:0]=D[2:0]
Set Adv. Program Control (double byte command)	0 0	0 0	0 #	0 #	1 #	1 #	0 #	0 #	RR #	 #	Set APC[R][7:0]=D[7:0], where RR = 00, or 01
Set Start Line	0	0	0	1	#	#	#	#	#	#	Set SL[5:0]=D[5:0]
Set V_{REF} potential meter (double-byte command)	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set PM[5:0]=D[5:0] Set GN[1:0]=D[7:6]
Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]=D[2:0]
Set Column Mirroring	0	0	1	0	1	0	0	0	0	#	Set LC[2]=D0
Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]=D0
Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]=D0
Set Display ON/OFF	0	0	1	0	1	0	1	1	1	#	Set DC[2]=D0
Set Page Address	0	0	1	0	1	1	#	#	#	#	Set PA[3:0]=D[3:0]
Set LCD to RAM Mapping	0	0	1	1	0	0	#	#	0	#	Set LC[3:0]=D[3:0]
Set Cursor Update Mode	0	0	1	1	1	0	0	0	0	0	Set AC[3]=1, CR=CA;
System Reset	0	0	1	1	1	0	0	0	1	0	System Reset sequence
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]= D[1:0]
Set/Reset Cursor-Update Mode	0	0	1	1	1	0	1	1	1	#	Set AC[3]=D0; if (D0) CR=CA else CA=CR;
Set Test Control (double byte command)	0 0	0 0	1 #	1 #	1 #	0 #	0 #	1 #	TT #	 #	For testing only. Do not use.

* Other than commands listed above, all other bit patterns result in NOP (No Operation).

LCD VOLTAGE SETTINGS

MULTIPLEX RATES

Two multiplex rates are supported in UC1602I: 65 or 49. The default is 65 and it can be changed by programming.

BIAS SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_D, i.e. $BR = V_{LCD}/V_D$, where V_D is the SEG data signal and its value is $| V_{B1+} - V_{B1-} |$

The optimum *Bias Ratio* can be calculated by:

$$\sqrt{Mux}+1$$

UC1602I supports four bias ratios as below.

BR	0	1	2	3
Bias Ratio	6	7	8	9

Table 2: BR vs. Mux rates

BR and MR can both be changed dynamically by software programming.

V_D GENERATION

V_D is generated internally by UC106. The value of V_D is determined by three control registers: *GN* (Gain), *PM* (Potential Meter), TC (Temperature Compensation) with the following relationship:

$$V_D = Gain \times V_{PM}$$

where V_{PM} is the output of an internal Electronic Potential Meter. The maximum value for V_D depends on the value of V_{DD2}. At V_{DD2} = 2.4V, V_D should be kept under 1.2V.

The value of V_{PM} is given by:

$$V_{PM} = \frac{600 + PM}{1200} \times V_{REF}$$

The value of *Gain* is controlled by GN[1:0]. Their relationship is shown below:

GN[1:0]	00	01	10	11
Gain	1.35	1.49	1.64	1.81

Table 3: Gain vs. GN value

V_{REF} TEMPERATURE COMPENSATION

V_{REF} is a temperature compensated reference voltage. V_{REF} increases automatically as ambient temperature cools down.

Four (4) different temperature compensated V_{REF} can be selected via pin wiring. The compensation coefficient is given by the following table:

TC[1:0]	0	1	2	3
% per °C	0.0	–0.05	–0.10	–0.20

Table 4: Temperature Compensation

For all TC values, V_{REF} are normalized to 1.2V at 25 °C.

V_{LCD} SELECTION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[2:1].

When V_{LCD} is generated internally its value has the following relationship with V_D:

$$V_{LCD} = BiasRatio \times V_D$$

Given V_{REF} = 1.2V at 25 °C, V_{LCD} becomes:

$$V_{LCD} \cong BiasRatio \times Gain \times \frac{600 + PM}{1200} \times 1.2 \quad (1)$$

When PM=0, then equation (1) becomes:

$$V_{LCD} \cong BiasRatio \times Gain \times 0.6 \quad (1b)$$

LOAD DRIVING STRENGTH

UC106's drivers and power supply circuits are designed to handle panel capacitance load of 25nF at V_{LCD}=9V when V_{DD2} >= 2.4V.

UC1602I load driving strength is sensitive to ITO impedance of power supply circuits (V_{DD2}, V_{SS2}, $V_{B0/B1}$, V_{LCD}.) Be sure to minimize the resistance of these ITO traces for COG applications.

POWER SUPPLY CONFIGURATION

UC1602I has built-in charge pump with on-chip pumping capacitors. The number of pump stages used can be programmed by setting PC[2:1] register. Make sure the chip is in Reset mode before changing the value of PC[2:0].

Given the same display quality, the lower the PC[2:1] setting the more efficient is UC1602I, but the weaker is the driving strength. In application, designer is recommended to verify the design with the highest setting first before trying lower settings to achieve better efficiency.

Due to the use of fully embedded power supply, built-in power ready detector, and drain circuit, there is no rigid power up or power down sequences for UC1602I controllers when using internal V_{LCD} generator.

On the other hand, caution must be exercised when external V_{LCD} source is used. The general rule of thumb is to make sure Display Enable is

OFF before connecting or disconnecting external V_{LCD} sources.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

The nominal frequency of UC1602I built-in system clock is 166kHz, the LCD refresh frequency is 80Hz. All required components for the clock oscillator are built-in. No external parts are required.

DRIVER MODES

Row and column drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When column drivers are in idle mode, their outputs are high-impedance (open circuit). When row drivers are in idle mode, their outputs are connected to V_{SS}.

DRIVER ARRANGEMENTS

The naming conventions are: R*x* (where x=1~64) refers to the row driver for the x-th row of pixels on the LCD panel; RIC refers to the icon driver.

Row drivers are clustered into “even row drivers” and “odd row drivers”, along the two sides of the chip to enhance the symmetry of ITO layout.

The mapping of Rx to LCD pixel rows is the same for all MR settings. When MR setting is not 11, leave unused row drivers open.

DISPLAY CONTROLS

There are three display control flags in the control register DC: Display Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DISPLAY ENABLE (DE)

Display Enable is controlled by the *Set Display ON* command. When DE is set to OFF (logic “0”), both column and row drivers will become idle and the chip will put itself into Sleep Mode to conserve power.

When the DE is set to ON, the chip will first exit from Sleep mode by restoring the power (V_{LCD}, V_D etc.). When the power is restored, column and row drivers will become active.

ALL PIXELS ON (APO)

When set, this flag will force all column drivers to output On signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag set to ON, column drivers will output the inverse of the value it received from the display buffer RAM. This flag has no impact on data stored in RAM.

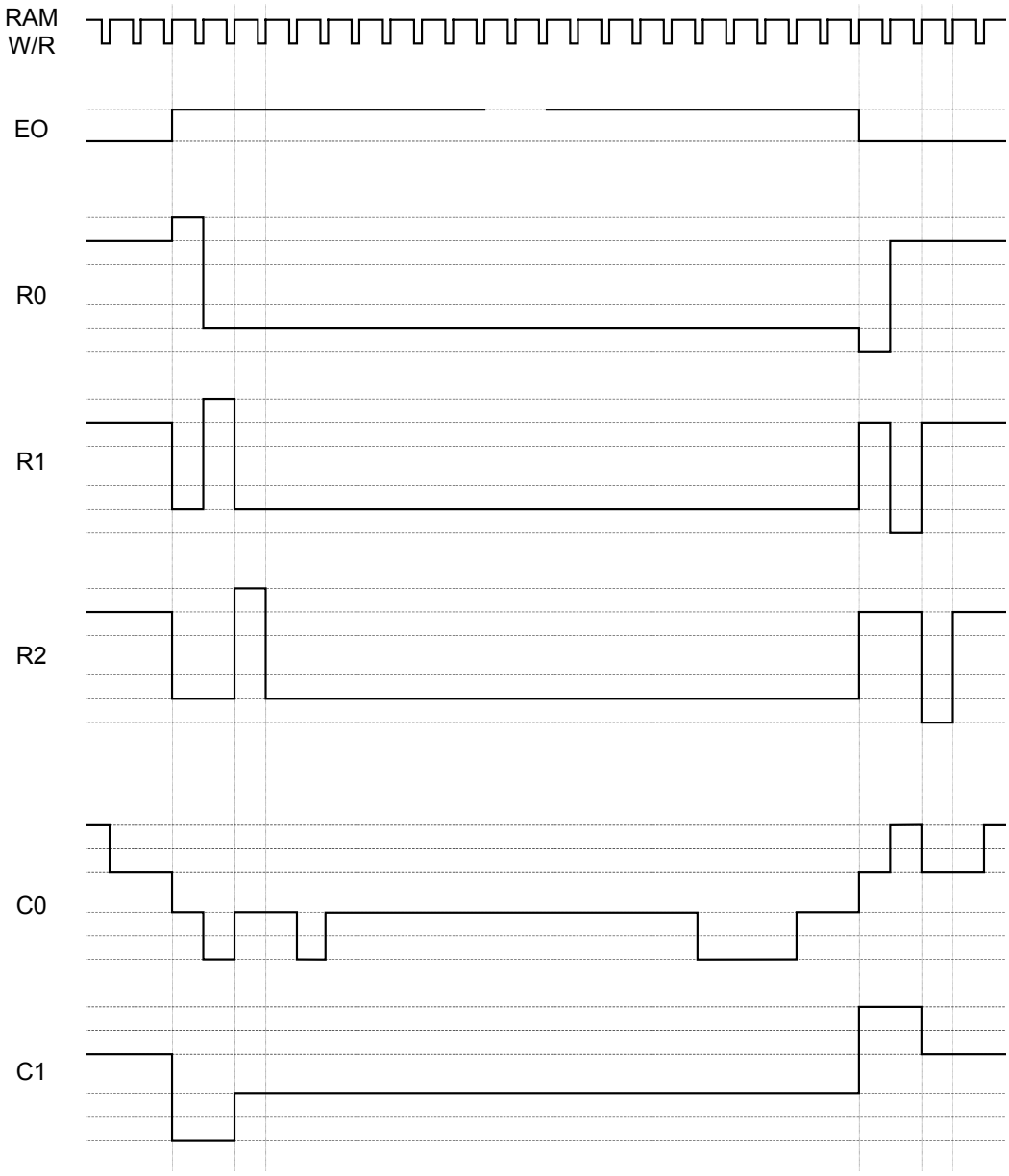


Fig. 4 Column and Row Driving Waveform

HOST INTERFACE

UC1602I series supports several parallel and serial host interface formats.

Bus	Bus Type	Access
Parallel	8080	R/W
	6800	R/W
Serial	4-wire (S8)	W
	2-wire (I^2C)	R/W

Table 5: Host interfaces Choices

System designers can use either the 8-bit parallel bus to achieve the high data transfer rate, or use serial bus to create LCD modules with as few as 9-pin connectors.

PARALLEL INTERFACE

It is possible to interface UC1602I controllers directly to either an 8080-style MPU bus or a 6800-style MCU bus with the following connection.

Bus Type	WR0	WR1
8080	$\overline{WR}$	$\overline{RD}$
6800	R/$\overline{W}$	E

Table 6: MPU bus control signal interface

The timing relationship between UC1602I internal control signal RD, WR and their associated bus actions are shown in the figure below. The generation of UC1602I internal bus control signals WR and RD is shown in the table below.

Bus Type	$\overline{WR}$	$\overline{RD}$
8080	WR0	WR1
6800	!(WR1 & !WR0)	!(WR1 & WR0)

Table 7: WR and RD signal generation

DISPLAY RAM DATA TRANSFER

UC1602I Display Data RAM (RAM) read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, either in parallel mode or serial mode, all three commands (*Set CA-LSB, Set CA-MSB, Set PA*) need to be issued, and a dummy read cycle need to be performed before the actual data can propagate through the pipe-line and be read from data port D[7:0].

There is no pipeline in write interface of RAM, and the data is transferred directly from data bus buffer to RAM.

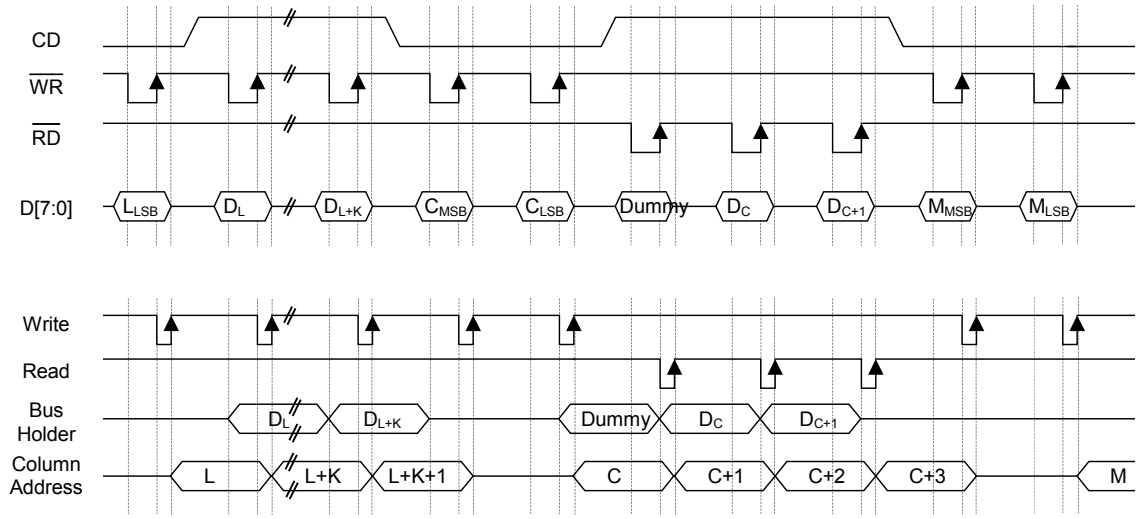


Figure 5: Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1602I supports two serial modes, 4-wire mode (PS=0), and 2-wire I^2C mode (PS=1). The mode of interface is determined during power-up process by the value of PS[1:0].

4-WIER SERIAL INTERFACE (S8)

Only write operations are supported in 4-wire serial mode. Pin CS[1-0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. On each write cycle, 8 bits of data, MSB first, are latched on eight (8) rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

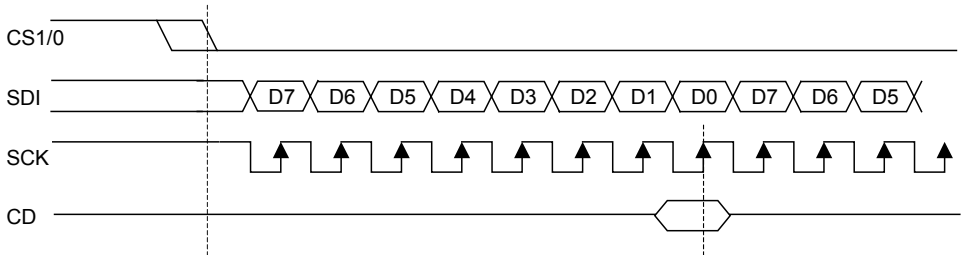


Figure 6: 4-wire Serial Interface (S8)

2-WIRE SERIAL INTERFACE (I^2C)

When PS[1-0] is set to "LH", UC1602I is configured as a slave receiver/transmitter, for industry standard I^2C serial interface.

Each UC1602I I^2C interface sequence starts with a START condition (S) from the bus master, followed by a sequence header, containing a device address, the direction of transfer (RW, 0:Write, 1:Read) and mode of transfer (CD, 0:Control, 1:Data).

In this mode, CS[1:0] become A[1:0] and are used to configure UC1602I's device address. WR[1:0] and CD are not used and may be connected to GND.

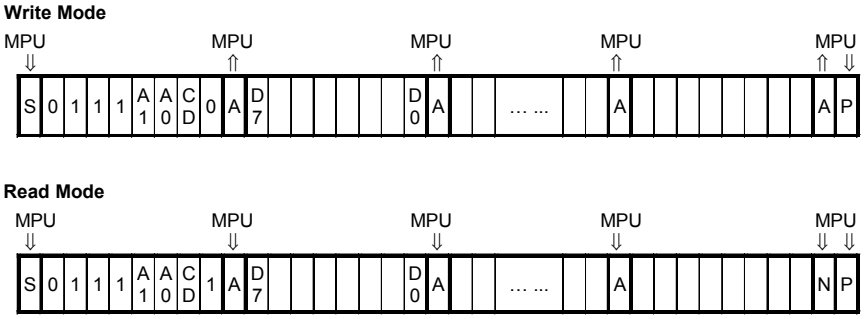


Figure 7: 2-wire interface protocol

The direction and content of the bytes following each header byte are fixed for the sequence. To change the direction (R⇔W) or the content type (C⇔D), start a new interface sequence with a new header.

After receiving the header, the UC1602I will send out an acknowledge signal (A). Then, depends on the setting of the header, the transmitting device (either the bus master or UC1602I) will start placing data bits on the serial bus, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE), or a Not Acknowledge (N, in READ mode) is sent by the bus master.

Note that, for data read (CD=1), the first byte of data is dummy.

2-WIRE INTERFACE TIMING

The 2-wire I^2C interface is a bidirectional interface. In order to properly communicate between all I^2C devices, certain timing protocols need to be satisfied.

There are always master and slave devices on an I^2C bus. The master device initiates an read or write action to the slave device with an address. The selected slave device to the action transimitting or receiving data. Without any action, the I^2C bus are pulled high by two pull-up resistors. A master or slave device initiates or responds to an action by pulling down the bus. UC1602I is a slave I^2C device.

In idle mode, the both wires, SDA and SCK are pulled high. When the SDA makes a HIGH to LOW transition while SCK remains high, this is the I^2C START condition. When the SDA makes a LOW to HIGH transition while SCK remain low, this is I^2C STOP condition. In between a START and STOP condition, I^2C transmits data bits by toggling SCK while SDA remains stable. These relations are shown in **Figure 8**.

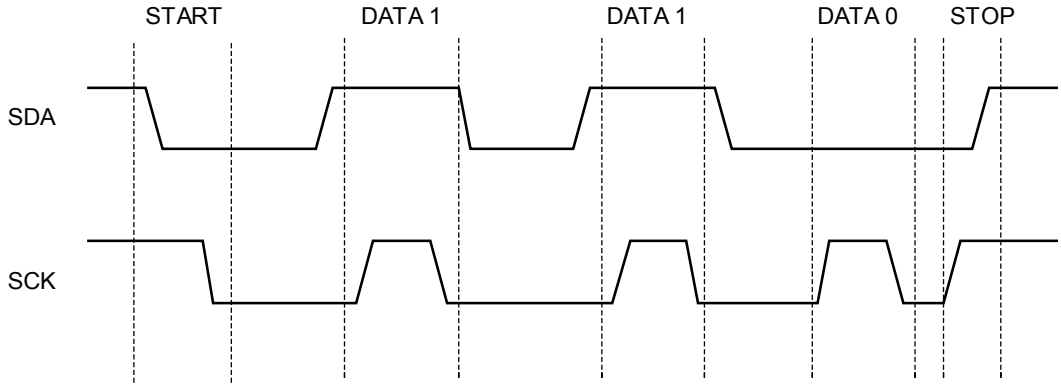


Figure 8. I^2C bus SDA and SCK timing relation.

Each eight-bit of data is followed by an acknowledge pulse from the receiver as shown in **Figure 9**. The master device will generate an extra pulse during this time. It is the receiving device's responsibility to generate this acknowledge pulse regardless of being a master or slave device. UC1602I generates an acknowledge pulse in the write mode. When the acknowledge pulse is HIGH, UC1602I has received write instruction or data correctly. When the acknowledge pulse is LOW, UC1602I has not correctly received instruction and the master device needs to resend.

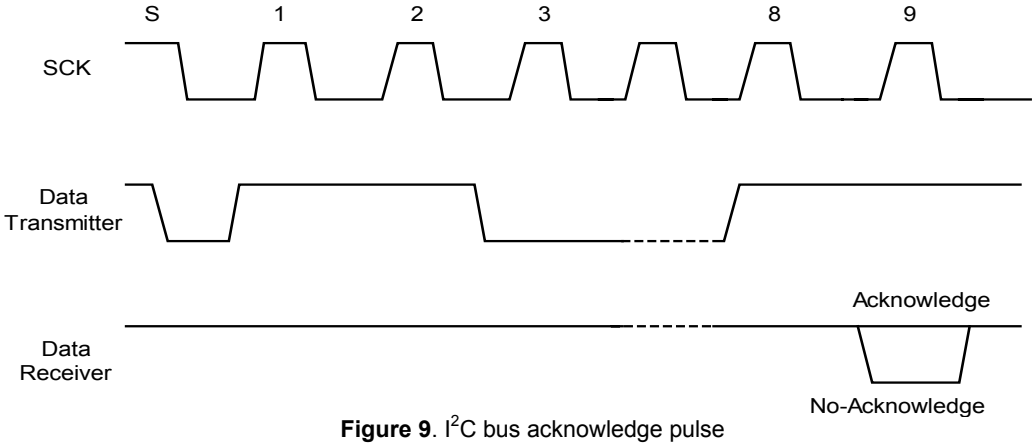


Figure 9. I^2C bus acknowledge pulse

SERIAL INTERFACE EXAMPLES

The table below shows an example of UC1602I to support a 9-pin (or 4-pin, if C_{LCD} and C_{Bx} are mounted on FPC or COF) interface using I^2C.

Hard wired	Comment
RST="H"	Use software Reset exclusively.
CA[1:0] ="XX"	Chip address
SP="01"	UC1602I will power up and reset to I^2C interface mode
on FPC/COF	**Comment**
V_{B0+}, V_{B0-} V_{B1+}, V_{B1-}	Connect to proper capacitors. These capacitors can be mounted on FPC as SMD.
Interface	**Comment**
SCK	Connect to clock
SDA	Serial I/O
V_{DD1}, V_{DD2}, V_{DD3}	Use three separate ITO traces to one common node.
V_{SS1} ,V_{SS2}	Use two separate ITO to one common node.
V_{LCD}	To V_{LCD} bypass capacitor

Table 9: I^2C Interface Example

The table below shows an example of UC1602I to support a 11-pin (or 6-pin, if C_{LCD} and C_{Bx} are mounted on FPC or COF), using S8, Write-only interface mode and CD pin for bus control.

Hard wired	Comment
RST="H"	Use software Reset exclusively.
SP="00"	UC1602I will power up and reset to S8 interface mode
SDO	Not used, Connect to GND
On FPC/COF	**Comment**
V_{B0+}, V_{B0-} V_{B1+}, V_{B1-}	Connect to two capacitors, mounted on FPC as SMD.
Interface	**Comment**
CS0 (or CS1)	Chip select
CD	Control or Display.
SCK	Connect to clock
SDA	Serial Data IN
V_{DD1}, V_{DD2}, V_{DD3}	Use three separate ITO traces to one common node.
V_{SS1} ,V_{SS2}	Use two separate ITO to one common node.
V_{LCD}	To V_{LCD} bypass capacitor

Table 10: S8 Interface Example

DISPLAY DATA RAM

DATA ORGANIZATION

The display data is one bit per pixel and stored in a dual port static RAM (RAM, for Display Data RAM). The RAM size is 65x102. This array of data bits are further organized into pages of 8 bit slices to facilitate parallel bus interface.

At the end of the graphics data, UC1602I contains an 1-bit wide page for icon data.

When Mirror X (MX, LC[2]) is OFF, the 1st column of LCD pixels will correspond to the bits of the first byte of each page, the 2nd column of LCD pixels correspond to the bits of the second byte of each page, etc.

MSB FIRST OR LSB FIRST

There are two options to map D[7:0] to RAM, MSB first (MSF=1), or LSB first (MSF=0), as illustrated below.

DISPLAY DATA RAM ACCESS

The memory used in UC1602I Display Data RAM (RAM) is a special purpose two port SRAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing *Set Page Address* and *Set Column Address* commands.

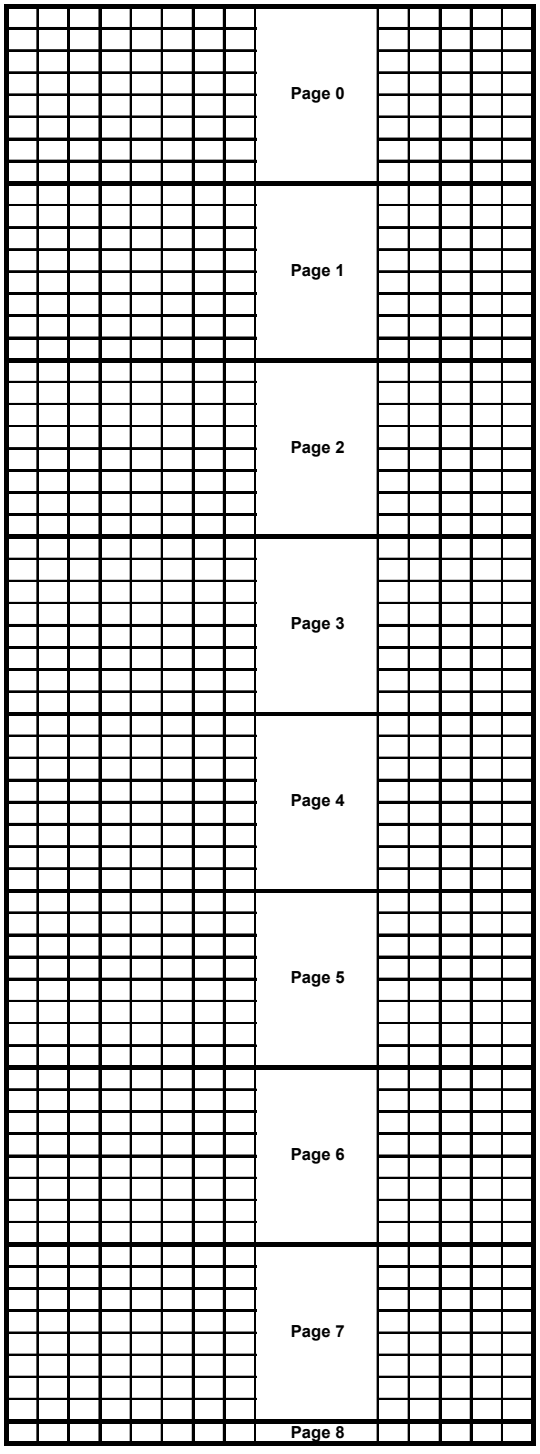
If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of page (102), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), after CA has reached the end of page (CA=101), CA will be rest to 0 and PA will increment or decrement, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 7), PA will be wrapped around to the other end of RAM and continue.

ICON DATA ADDRESSING

The Icon Page is addressed by explicitly setting PA to 8 (the 9th page). When addressing Icon page, auto wrap-around will be suspended and CA will stop when CA reaches 102.

PA[3:0]	MSF 0	MSF 1	Line Adderss
0000	D0	D7	00H
	D1	D6	01H
	D2	D5	02H
	D3	D4	03H
	D4	D3	04H
	D5	D2	05H
	D6	D1	06H
	D7	D0	07H
0001	D0	D7	08H
	D1	D6	09H
	D2	D5	0AH
	D3	D4	0BH
	D4	D3	0CH
	D5	D2	0DH
	D6	D1	0EH
	D7	D0	0FH
0010	D0	D7	10H
	D1	D6	11H
	D2	D5	12H
	D3	D4	13H
	D4	D3	14H
	D5	D2	15H
	D6	D1	16H
	D7	D0	17H
0011	D0	D7	18H
	D1	D6	19H
	D2	D5	1AH
	D3	D4	1BH
	D4	D3	1CH
	D5	D2	1DH
	D6	D1	1EH
	D7	D0	1FH
0100	D0	D7	20H
	D1	D6	21H
	D2	D5	22H
	D3	D4	23H
	D4	D3	24H
	D5	D2	25H
	D6	D1	26H
	D7	D0	27H
0101	D0	D7	28H
	D1	D6	29H
	D2	D5	2AH
	D3	D4	2BH
	D4	D3	2CH
	D5	D2	2DH
	D6	D1	2EH
	D7	D0	2FH
0110	D0	D7	30H
	D1	D6	31H
	D2	D5	32H
	D3	D4	33H
	D4	D3	34H
	D5	D2	35H
	D6	D1	36H
	D7	D0	37H
0111	D0	D7	38H
	D1	D6	39H
	D2	D5	3AH
	D3	D4	3BH
	D4	D3	3CH
	D5	D2	3DH
	D6	D1	3EH
	D7	D0	3FH
1000	D0	D7	40H



MX															
0	C0	C1	C2	C3	C4	C5	C6	C7		C97	C98	C99	C100	C101
1	C101	C100	C99	C98	C97	C96	C95	C94		C4	C3	C2	C1	C0

MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=0	MY=1 SL=25	MY=1 SL=25
R1	R49	R64	R48	R25	R9
R2	R50	R63	R47	R24	R8
R3	R51	R62	R46	R23	R7
R4	R52	R61	R45	R22	R6
R5	R53	R60	R44	R21	R5
R6	R54	R59	R43	R20	R4
R7	R55	R58	R42	R19	R3
R8	R56	R57	R41	R18	R2
R9	R57	R56	R40	R17	R1
R10	R58	R55	R39	R16	---
R11	R59	R54	R38	R15	---
R12	R60	R53	R37	R14	---
R13	R61	R52	R36	R13	---
R14	R62	R51	R35	R12	---
R15	R63	R50	R34	R11	---
R16	R64	R49	R33	R10	---
R17	R1	R48	R32	R9	---
R18	R2	R47	R31	R8	---
R19	R3	R46	R30	R7	---
R20	R4	R45	R29	R6	---
R21	R5	R44	R28	R5	---
R22	R6	R43	R27	R4	---
R23	R7	R42	R26	R3	---
R24	R8	R41	R25	R2	---
R25	R9	R40	R24	R1	---
R26	R10	R39	R23	R64	R48*
R27	R11	R38	R22	R63	R47
R28	R12	R37	R21	R62	R46
R29	R13	R36	R20	R61	R45
R30	R14	R35	R19	R60	R44
R31	R15	R34	R18	R59	R43
R32	R16	R33	R17	R58	R42
R33	R17	R32	R16	R57	R41
R34	R18	R31	R15	R56	R40
R35	R19	R30	R14	R55	R39
R36	R20	R29	R13	R54	R38
R37	R21	R28	R12	R53	R37
R38	R22	R27	R11	R52	R36
R39	R23	R26	R10	R51	R35
R40	R24	R25	R9	R50	R34
R41	R25	R24	R8	R49	R33
R42	R26	R23	R7	R48	R32
R43	R27	R22	R6	R47	R31
R44	R28	R21	R5	R46	R30
R45	R29	R20	R4	R45	R29
R46	R30	R19	R3	R44	R28
R47	R31	R18	R2	R43	R27
R48	R32	R17	R1	R42	R26
R49	R33	R16	---	R41	R25
R50	R34	R15	---	R40	R24
R51	R35	R14	---	R39	R23
R52	R36	R13	---	R38	R22
R53	R37	R12	---	R37	R21
R54	R38	R11	---	R36	R20
R55	R39	R10	---	R35	R19
R56	R40	R9	---	R34	R18
R57	R41	R8	---	R33	R17
R58	R42	R7	---	R32	R16
R59	R43	R6	---	R31	R15
R60	R44	R5	---	R30	R14
R61	R45	R4	---	R29	R13
R62	R46	R3	---	R28	R12
R63	R47	R2	---	R27	R11
R64	R48	R1	---	R26	R10
RIC	RIC	RIC	RIC	RIC	RIC
		65	49	65	49

MUX

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (101–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

DISPLAY SCANNING

During each field of display, depends on the setting of MR, row electrodes will be scanned in a fixed pattern at a rate of

(80 x Mux Rate) rows/second.

During each row period, the signal at the column drivers determine the ON/OFF status of the row of pixels being scanned.

ROW SCANNING

Icon data is always outputted via RIC electrodes before the 1st row of each field. It is then followed by scanning R1 through R*m*, where *m* may be 64, or 48 depends on the setting of MR.

Row electrode scanning orders are not affected by Start Line (SL) or Mirror Y (MY, LC[3]). When MY is 0, the effect of SL having a value *K* is to change the mapping of R0 to the *K*-th bit slice of data stored in display RAM. Visually, SL having a non-zero value is equivalent to scrolling LCD display up by SL rows.

RAM ADDRESS GENERATION

The mapping of the data store in the display SRAM and the scanning electrodes can be obtained by combining the fixed R*m* scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *Icon Line (40H)*

For the 2nd line period of each field
Line = *SL*

Otherwise
Line = Mod(*Line*+1, *64*)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to column drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produce the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches *64*.

Effects such as page scrolling, page swapping can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between row electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = *Icon Line (40H)*

For the 2nd line period of each field
Line = Mod(*SL* + *MUX-2*, *64*)
where MUX = 65 or 49

Otherwise
Line = Mod(*Line-1* , *64*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1602I has two different types of Reset: *Power-ON-Reset* and *System-Reset*.

Power-ON-Reset is performed right after V_{DD1} is connected to power. *Power-On-Reset* will first wait for about 12mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1602I enters RESET sequence:

- All non-pin configurable control registers will be reset to their default values.
- All pin configurable control registers will be reset according to their configuration pins.
- Operation mode will be "Reset"
- System Status bits RS and BZ will stay as "1" until the Reset process is completed (for a duration of 3~5uS).

Refer to Control Registers for details of control flags and their default values. Refer to Pin Description for configuration pin definitions.

When RS=1, only status read command is processed by UC106. All other commands are ignored.

Once entered Reset mode, all control registers will be reset to their default values and capacitors will be discharged. In general it is necessary to set up control registers before transition out of the Reset mode.

OPERATION MODES

UC1602I has three operating modes (OM): Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	OFF	OFF

Table 11: Operating Modes

CHANGING OPERATION MODE

Two commands will initiate OM transitions: *Set Display Enable*, and *System Reset*.

Action	Mode	OM
Set Display Enable "ON"	Normal	11
Set Display Enable "OFF"	Sleep	10
Reset command RST_ pin pulled "L" Power ON reset	Reset	00

Table 12: OM changes

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter power saving mode.

For maximum energy utilization, Sleep mode is designed to retain charges stored in external capacitors C_{B0}, C_{B1} and C_{LCD}. To drain these capacitors, use Reset command to activate the on-chip draining circuit.

OM changes are synchronized with the edges of UC1602I internal clock. To ensure consistent system states, wait at least 10uS after *System Reset* or *Set Display Enable* command.

EXITING POWER SAVE MODES

UC1602I contains internal logic to check whether V_{LCD} and V_D is ready before releasing row and column drivers from their OFF states. When exiting Sleep Mode and Reset Mode, column and row drivers will not be activated until UC1602I internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1602I power-up sequence is simplified by built-in "Power Ready" flags and by the automatic invocation of *System-Reset* command after *Power-ON-Reset*. System programmer are only required to wait 4~6 ms before starting to issue commands to UC106. No additional commands or waits are required between enabling of the charge pump, turning on the display drivers, writing to RAM or any other commands.

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{B+}, C_{B-}, and C_{LCD} from damaging the LCD when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

UC1602I draining resistance is 1K for both V_{LCD} and V_{B+}. It is recommended to wait *3* x *RC* for

V_{LCD} and *1.5 x RC* for V_{B+} before allowing V_{DD} to drop below 2V. For example, if C_{LCD} is 1uF, then the draining time required for V_{LCD} is 3~5mS.

UC1602I will *not* drain V_{LCD} when internal V_{LCD} is not used. System designer should take care to make sure external V_{LCD} source is properly drained off before turning off VDD.

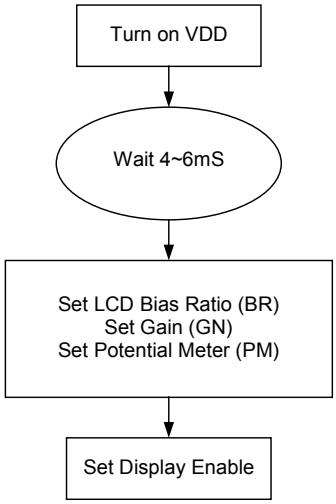


Figure 12: Reference Power-up Sequence

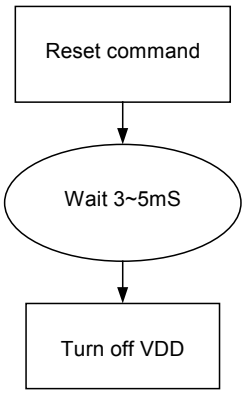


Figure 13: Reference Power-Down Sequence

SAMPLE COMMAND SEQUENCES

The following table are host interface examples for various UC1602I operations.

Step sequences starting with the same number (such as 2a, 2b, 2c, …) can be rearranged without affecting the result. Some optional steps have mutual dependencies. Such mutually-dependent optional steps need to be elected or skipped together as a group.

C/D The type of the interface cycle. Depending on the interface type (parallel or serial). This may be external pin (parallel and serial 8-bit), part of the bit stream (serial 9-bit write) or the internal flag (serial 9-bit read).

W/R The direction of data flow of the cycle. It can be either Write (0) or Read (1).

BZ, OM The status of these flags "*during*" the operation of the command.

(Opt.) Optional item.

POWER-UP SEQUENCE

The only "*required*" command to initialize UC1602I is *Set Display ON*. However, many other commands (such as *Set APO* = 0/1, *Set LCD Mapping*) and any of the NOP bit patterns can be used for maximum software compatibility with other industry leading LCD controller-drivers.

The following command sequence can be performed in parallel 8-bit, I^2C or S8 modes.

Example 1: Use System Reset command.

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
	–	–	–	–	–	–	–	–	–	–	Power-On reset. V_{DD} powering up. Wait ~15mS for V_{DD} to become steady.	—	1	(Recommended) Use "Read Status" to make sure BZ flag is 0 before issuing any other command.
	–	–	–	–	–	–	–	–	–	–	Automatic System Reset.	—	1	
	0	1	D	D	D	D	–	–	–	–	(Opt.) Read Status	00	0	
	0	0	1	0	1	0	1	0	0	0	(Opt.) System Reset	00	0	Recommended.
	0	0	1	1	1	0	1	0	#	#	(Opt.) Set Bias Ratio	00	0	
	0	0	0	0	1	0	0	#	#	#	(Opt.) Set Gain	00	0	
	0 –	0 –	1 –	0 –	0 #	0 #	0 #	0 #	0 #	1 #	(Opt.) Set PM	00	0	
	0	0	0	0	1	0	1	#	#	#	(Opt.) Set Power Control	00	0	If external V_{LCD} is selected, activate the source here.
	0	0	1	0	1	0	1	1	1	1	Set Display ON	11	0	

Note: Example 1 does not require the use of RST pin and therefore is more appropriate for applications where compact connector size is critical.

Example 2: Use RST pin.

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
	–	–	–	–	–	–	–	–	–	–	Hold RST pin to “L” until the external power is stable.	—	1	
	0	1	D	D	D	D	–	–	–	–	(Opt.) Read Status	00	0	Recommended
	0	0	1	1	1	0	0	0	1	0	(Opt.) System Reset	00	0	Recommended
	0	0	1	1	1	0	1	0	#	#	(Opt.) Set Bias Ratio	00	0	
	0	0	0	0	1	0	0	#	#	#	(Opt.) Set Gain	00	0	
	0 –	0 –	1 –	0 –	0 #	0 #	0 #	0 #	0 #	1 #	(Opt.) Set PM	00	0	
	0	0	0	0	1	0	1	#	#	#	(Opt.) Set Power Control	00	0	If external V_{LCD} is selected, activate the source here.
	0	0	1	0	1	0	1	1	1	1	Set Display ON	11	0	

POWER-DOWN SEQUENCES

The following two command sequences can be performed in parallel, I^2C or S8 modes.

Option 1: Use System Reset command.

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
	0	0	1	1	1	0	0	0	1	0	System Reset	00	1	
	–	–	–	–	–	–	–	–	–	–	(Wait ~3mS)	00	0	Draining C_{LCD}, C_B
	–	–	–	–	–	–	–	–	–	–	Turn off V_{DD}	00	0	

Note: Option 1 does not require the use of RST pin and therefore is more appropriate for applications where compact connector size is critical.

Option 2: Use RST pin.

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
	–	–	–	–	–	–	–	–	–	–	Hold RST to “L”, wait ~3mS	00	1	Draining C_{LCD}, C_B
	–	–	–	–	–	–	–	–	–	–	Turn off V_{DD}	00	0	

PREPARE TO ACCESS DATA RAM

Address control (register AC) flags and some LCD to SRAM mapping (register LC) flags affect how data is stored into the display buffer SRAM => Make proper adjustment to these two registers before writing data to UC1602I display buffer SRAM.

These sequence can be performed in parallel 8-bit, I^2C or S8 modes. These commands can be performed under any operating mode (OM).

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
	0	0	1	0	0	0	1	#	#	#	(Opt.) Set Address Control	–	0	
	0	0	1	1	0	0	#	#	0	#	(Opt.) Set/clear LCD Mapping control flags.	–	0	

DATA RAM ACCESS: WRITE

These sequence can be performed in parallel 8-bit, I^2C or S8. These commands can be performed under any operating mode (OM).

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
1	0	0	1	0	1	1	#	#	#	#	Set Page Address	–	0	
2	0	0	0	0	0	1	#	#	#	#	Set Column Address MSB	–	0	
3	0	0	0	0	0	0	#	#	#	#	Set Column Address LSB	–	0	
4	1	0	#	#	#	#	#	#	#	#	Write Display Data (repeat as appropriate)	–	0	
5											(Return to 1 as necessary, repeat until complete)	–	0	

DATA RAM ACCESS: READ

For parallel interface and I^2C modes, a dummy Read cycle is required when a Read Data command follows immediately after a Write cycle (either Write Data or Write Control).

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
1	X	0	1	0	1	1	#	#	#	#	Write cycle (either data or control)	–	0	For example: Commands setting PA and/or CA.
2	1	1	–	–	–	–	–	–	–	–	Dummy Read cycle	–	0	
3	1	1	#	#	#	#	#	#	#	#	Read Display Data (repeat as appropriate)	–	0	

DATA RAM ACCESS: CURSOR UPDATE

Cursor can be used to support many flexible user interface designs. Blinking cursor requires frequent update to a limited set of pixels. UC1602I Cursor update mode is designed to facilitate such frequent data RAM updates.

Under Cursor Update mode, both the wrap around (CA reset to 0, PA increment or decrement) and CA increment on Read are temporary disabled. These two features allow system designer to minimize the need to update CA and PA registers and allows on-chip RAM to be used in Read-Modify-Write style operations.

EXAMPLE 1: CURSOR UPDATE WITH READ-MODIFY-WRITE, PARALLEL INTERFACE OR I^2C MODE

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
1	0	0	1	1	1	0	0	0	0	0	Set Cursor-Update mode and set CR=CA	–	0	CR tracks where CA should be restored later
2	1	1	–	–	–	–	–	–	–	–	Dummy Read cycle	–	0	CA unchanged
	1	1	#	#	#	#	#	#	#	#	Read Display Data			
3	1	0	#	#	#	#	#	#	#	#	Write Display Data	–	0	CA will increment, but will not wrap around
											(Return to 2 and repeat until the cursor is updated)	–	0	
4	0	0	1	1	1	0	1	1	1	0	Clear Cursor Update Mode	–	0	Set CA=CR
											Return to 1 for next cursor update cycle or continue	–	0	

EXAMPLE 2: CURSOR UPDATE WITHOUT READ, ALL INTERFACE MODES

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
1	0	0	1	1	1	0	1	1	1	1	Set Cursor-Update mode and set CR=CA	–	0	CR remembers where CA should be restored later
2	1	0	#	#	#	#	#	#	#	#	Write Display Data	–	0	CA will increment but will not wrap around
3											(Return to 2 and repeat until the cursor is updated)	–	0	
4	0	0	1	1	1	0	1	1	1	0	Clear Cursor Update Mode	–	0	Set CA=CR
											Return to 1 for next cursor update cycle or continue	–	0	

ENABLE DISPLAY

The following command sequence can be performed in all interface modes.

#	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Operation	OM	BZ	Comments
	0	0	0	1	#	#	#	#	#	#	(Opt.) Set Start Line	–	0	
	0	0	1	0	1	0	0	1	0	#	(Opt.) Set All-Pixel-ON	–	0	
	0	0	1	0	1	0	0	1	1	#	(Opt.) Set Inverse Mode.	–	0	
	0	0	1	0	1	0	1	1	1	1	Set Display ON	11	0	

Note: The order of these steps are not critical. However, for the smoothness of display effect, the above sequence is recommended.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD1}	Logic Supply voltage	-0.3	+4	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4	V
V_{LCD}	LCD Generated voltage	-0.3	+12	V
V_{IN} / V_{OUT}	Any input/output	-0.3	V_{DD} + 0.3	V
T_{OPR}	Operating temperature range	-25	+85	^{o}C
T_{STR}	Storage temperature	-50	+100	^{o}C
T_J	Junction temperature		+150	^{o}C
P_{IC}	Total power dissipation		250	mW

Notes

1. V_{DD1} based on V_{SS1} = 0V. V_{LCD} based on V_{SS2} = 0V.
2. Stress outside values listed may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD1}	Digital Supply voltage		2.4		3.7	V
V_{DD2}	Supply for V_{LCD} generation		2.4		3.7	V
V_{LCD}	LCD Driving Voltage		4.5		10.5	V
V_{B0}	LCD Bias Voltage					V
V_{IL}	Input logic LOW			0.2Vdd		V
V_{IH}	Input logic HIGH			0.8Vdd		V
V_{OL}	Output logic LOW			0.2Vdd		V
V_{OH}	Output logic HIGH			0.8Vdd		V
I_{IL}	Input leakage current			1		μA
I_{OZ}	Output leakage current					μA
$R_{0(col.)}$	Column output impedance	V_{LCD} = 9.0V		2.4	4.0	kΩ
$R_{0(row)}$	Row output impedance	V_{LCD} = 9.0V		2.4	4.0	kΩ
f_{CLK}	Internal clock frequency		133	166	200	kHz

AC CHARACTERISTICS

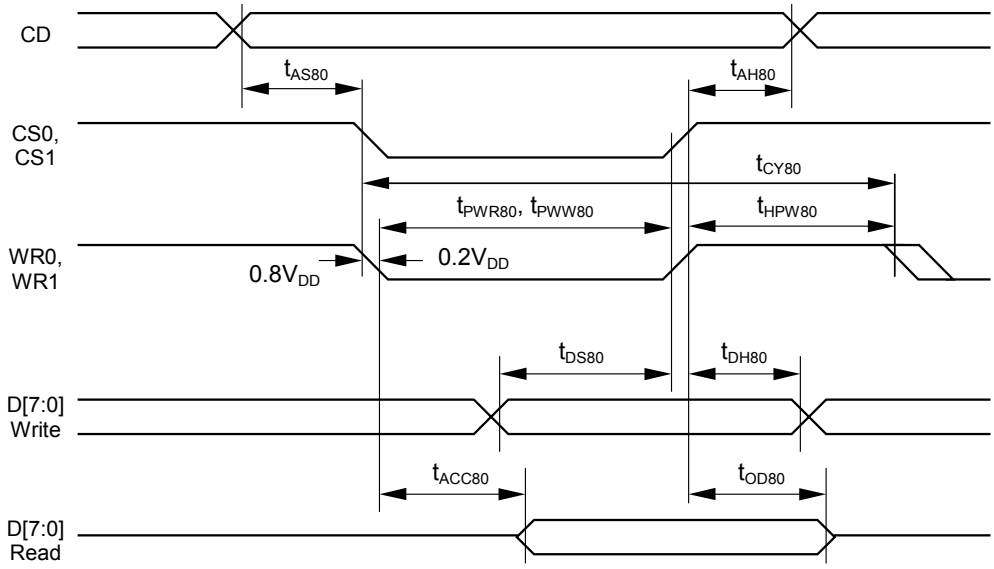


Figure 21: Parallel Bus Timing Characteristics (for 8080 MCU)

(VDD=2.4V to 3.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		25 50	–	ns
t_{CY80}		System cycle time		300	–	ns
t_{PWR80}	WR1	Pulse width (read)		120	–	ns
t_{PWW80}	WR0	Pulse width (write)		60	–	ns
t_{HPW80}	WR0, WR1	High pulse width		60	–	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		40 15	–	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	140 100	ns

(VDD=3.0V to 4.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		20 45	–	ns
T_{CY80}		System cycle time		166	–	ns
t_{PWR80}	WR1	Pulse width (read)		75	–	ns
t_{PWW80}	WR0	Pulse width (write)		30	–	ns
t_{HPW80}	WR0, WR1	High pulse width		30	–	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	65 45	ns

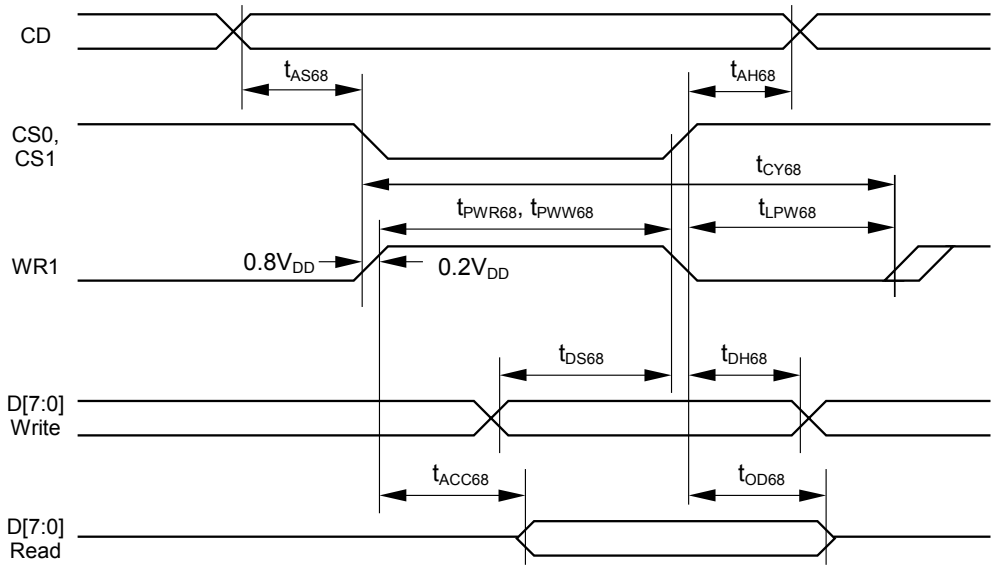


Figure 22: Parallel Bus Timing Characteristics (for 6800 MCU)

(VDD=2.4V to 3.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		25 50	–	ns
T_{CY68}		System cycle time		300	–	ns
t_{PWR68}	WR1	Pulse width (read)		120	–	ns
t_{PWW68}		Pulse width (write)		60	–	ns
t_{LPW68}		Low pulse width		60	–	ns
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		40 15	–	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 10	140 100	ns

(VDD=3.0V to 4.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		20 45	–	ns
T_{CY68}		System cycle time		166	–	ns
t_{PWR68}	WR1	Pulse width (read)		75	–	ns
t_{PWW68}		Pulse width (write)		30	–	ns
t_{LPW68}		Low pulse width		30	–	ns
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 10	70 50	ns

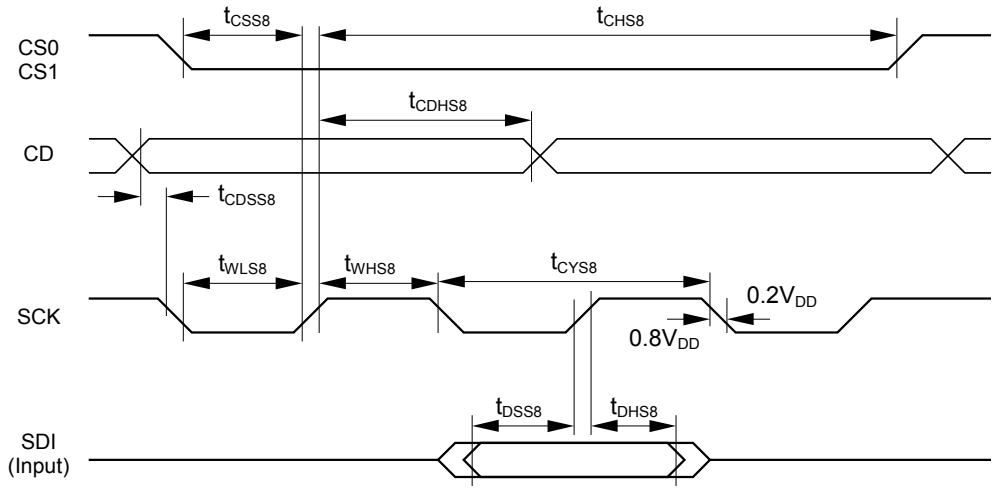


Figure 23: Serial Bus (S8 mode) Timing Characteristics

(VDD=2.4V to 3.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CSS8} t_{CHS8}	CS	CS setup time CS hold time		150 150	–	ns
T_{CDSS8} t_{CDHS8}	CD	CD setup time CD hold time		15 10	–	ns
t_{CYS8} t_{WHS8} t_{WLS8}	SCK	SCK clock cycle SCK high width SCK low width		250 100 100	–	ns
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		90 90	–	ns

(VDD=3.0V to 4.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CSS8} t_{CHS8}	CS	CS setup time CS hold time		100 100	–	ns
t_{CDSS8} t_{CDHS8}	CD	CD setup time CD hold time		10 5	–	ns
t_{CYS8} t_{WHS8} t_{WLS8}	SCK	SCK clock cycle SCK high width SCK low width		200 75 75	–	ns
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		50 50	–	ns

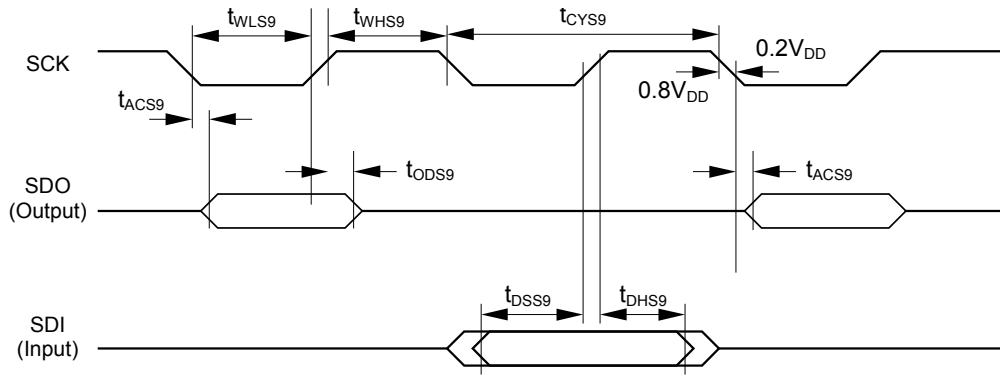


Figure 24: Serial Bus (I^2C mode) Timing Characteristics

(VDD=2.4V to 3.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9} t_{WHS9} t_{WLS9}	SCK	Serial I/O clock cycle SCK high width SCK low width				ns
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time				ns
t_{ACS9} t_{ODS9}	SDA	Read access time Output disable time	C_L = 100pF			ns

(VDD=3.0V to 4.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9} t_{WHS9} t_{WLS9}	SCK	Serial I/O clock cycle SCK high width SCK low width				ns
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time				ns
t_{ACS9} t_{ODS9}	SDA	Read access time Output disable time	C_L = 100pF			ns

Figure 25: Reset Characteristics

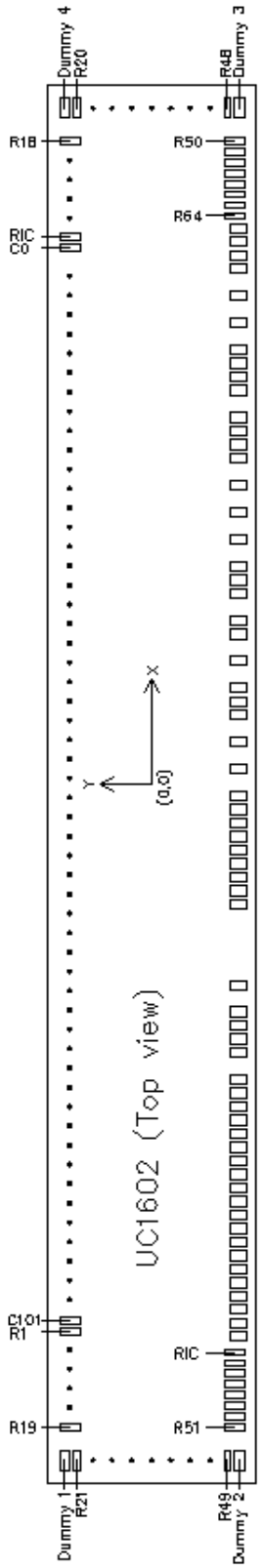
(VDD=2.4V to 3.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		1000	–	ns

(VDD=3.0V to 4.0V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		500	–	ns

PHYSICAL DIMENSIONS



Die size : 7.234 x 1.065 x 0.5 mm
Bump height : 18µm

#	Pin	X	Y	BX	BY
1	DUMMY1	-3500.7	447.0	100	51
2	R21	-3500.7	385.0	100	35
3	R23	-3500.7	330.0	100	35
4	R25	-3500.7	275.0	100	35
5	R27	-3500.7	220.0	100	35
6	R29	-3500.7	165.0	100	35
7	R31	-3500.7	110.0	100	35
8	R33	-3500.7	55.0	100	35
9	R35	-3500.7	0.0	100	35
10	R37	-3500.7	-55.0	100	35
11	R39	-3500.7	-110.0	100	35
12	R41	-3500.7	-165.0	100	35
13	R43	-3500.7	-220.0	100	35
14	R45	-3500.7	-275.0	100	35
15	R47	-3500.7	-330.0	100	35
16	R49	-3500.7	-385.0	100	35
17	DUMMY2	-3500.7	-447.0	100	51
18	R51	-3327.6	-420.5	35	100
19	R53	-3272.6	-420.5	35	100
20	R55	-3217.6	-420.5	35	100
21	R57	-3162.6	-420.5	35	100
22	R59	-3107.6	-420.5	35	100
23	R61	-3052.6	-420.5	35	100
24	R63	-2997.6	-420.5	35	100
25	RIC	-2942.6	-420.5	35	100
26	CS0	-2859.9	-440.5	50	80
27	CS1	-2789.9	-440.5	50	80
28	VDD1	-2719.9	-440.5	50	80
29	TP3	-2649.9	-440.5	50	80
30	RST	-2579.9	-440.5	50	80
31	CD	-2509.9	-440.5	50	80
32	WR0	-2439.9	-440.5	50	80
33	WR1	-2369.9	-440.5	50	80
34	VDD1	-2299.9	-440.5	50	80
35	D0	-2229.9	-440.5	50	80
36	D1	-2159.9	-440.5	50	80
37	D2	-2089.9	-440.5	50	80
38	D3	-2019.9	-440.5	50	80
39	D4	-1949.9	-440.5	50	80
40	D5	-1879.9	-440.5	50	80
41	D6	-1809.9	-440.5	50	80
42	D7	-1739.9	-440.5	50	80
43	VDD1	-1669.8	-440.5	50	80
44	VDD1	-1599.8	-440.5	50	80
45	VDD1	-1529.9	-440.5	50	80

#	Pin	X	Y	BX	BY
46	VDD2	-1389.8	-440.5	50	80
47	VDD2	-1319.8	-440.5	50	80
48	VDD2	-1249.8	-440.5	50	80
49	VDD2	-1179.9	-440.5	50	80
50	VDD3	-1039.9	-440.5	50	80
51	VSS2	-622.6	-440.5	50	80
52	VSS2	-552.6	-440.5	50	80
53	VSS2	-482.6	-440.5	50	80
54	VSS2	-412.6	-440.5	50	80
55	VSS	-342.6	-440.5	50	80
56	VSS	-272.6	-440.5	50	80
57	VSS	-202.6	-440.5	50	80
58	VSS	-132.6	-440.5	50	80
59	TST3	-62.6	-440.5	50	80
60	TST2	77.4	-440.5	50	80
61	TST1	217.4	-440.5	50	80
62	VB1+	357.6	-440.5	50	80
63	VB1+	427.6	-440.5	50	80
64	VB1+	497.6	-440.5	50	80
65	PS0	637.6	-440.5	50	80
66	VDD1	777.6	-440.5	50	80
67	PS1	847.6	-440.5	50	80
68	VB1-	987.6	-440.5	50	80
69	VB1-	1057.6	-440.5	50	80
70	VB1-	1127.6	-440.5	50	80
71	TP2	1267.6	-440.5	50	80
72	TP1	1407.6	-440.5	50	80
73	TP0	1547.6	-440.5	50	80
74	VB0-	1688.6	-440.5	50	80
75	VB0-	1758.6	-440.5	50	80
76	VB0-	1828.6	-440.5	50	80
77	VB0-	1898.6	-440.5	50	80
78	VB0+	2038.6	-440.5	50	80
79	VB0+	2108.6	-440.5	50	80
80	VB0+	2178.6	-440.5	50	80
81	VB0+	2248.6	-440.5	50	80
82	VLCDOUT	2388.6	-440.5	50	80
83	VLCDIN	2528.6	-440.5	50	80
84	VLCDOUT	2668.6	-440.5	50	80
85	VLCDIN	2738.6	-440.5	50	80
86	VDD2	2808.6	-440.5	50	80
87	VDD2	2878.5	-440.5	50	80
88	R64	2942.6	-420.5	35	100
89	R62	2997.6	-420.5	35	100
90	R60	3052.6	-420.5	35	100

#	Pin	X	Y	BX	BY
91	R58	3107.6	-420.5	35	100
92	R56	3162.6	-420.5	35	100
93	R54	3217.6	-420.5	35	100
94	R52	3272.6	-420.5	35	100
95	R50	3327.6	-420.5	35	100
96	DUMMY3	3500.7	-447.0	100	51
97	R48	3500.7	-385.0	100	35
98	R46	3500.7	-330.0	100	35
99	R44	3500.7	-275.0	100	35
100	R42	3500.7	-220.0	100	35
101	R40	3500.7	-165.0	100	35
102	R38	3500.7	-110.0	100	35
103	R36	3500.7	-55.0	100	35
104	R34	3500.7	0.0	100	35
105	R32	3500.7	55.0	100	35
106	R30	3500.7	110.0	100	35
107	R28	3500.7	165.0	100	35
108	R26	3500.7	220.0	100	35
109	R24	3500.7	275.0	100	35
110	R22	3500.7	330.0	100	35
111	R20	3500.7	385.0	100	35
112	DUMMY4	3500.7	447.0	100	51
113	R18	3327.4	420.5	35	100
114	R16	3272.4	420.5	35	100
115	R14	3217.4	420.5	35	100
116	R12	3162.4	420.5	35	100
117	R10	3107.4	420.5	35	100
118	R8	3052.4	420.5	35	100
119	R6	2997.4	420.5	35	100
120	R4	2942.4	420.5	35	100
121	R2	2887.4	420.5	35	100
122	RIC	2832.4	420.5	35	100
123	C0	2777.4	420.5	35	100
124	C1	2722.4	420.5	35	100
125	C2	2667.4	420.5	35	100
126	C3	2612.4	420.5	35	100
127	C4	2557.4	420.5	35	100
128	C5	2502.4	420.5	35	100
129	C6	2447.4	420.5	35	100
130	C7	2392.4	420.5	35	100
131	C8	2337.4	420.5	35	100
132	C9	2282.4	420.5	35	100
133	C10	2227.4	420.5	35	100
134	C11	2172.4	420.5	35	100
135	C12	2117.4	420.5	35	100

#	Pin	X	Y	BX	BY
136	C13	2062.4	420.5	35	100
137	C14	2007.4	420.5	35	100
138	C15	1952.4	420.5	35	100
139	C16	1897.4	420.5	35	100
140	C17	1842.4	420.5	35	100
141	C18	1787.4	420.5	35	100
142	C19	1732.4	420.5	35	100
143	C20	1677.4	420.5	35	100
144	C21	1622.4	420.5	35	100
145	C22	1567.4	420.5	35	100
146	C23	1512.4	420.5	35	100
147	C24	1457.4	420.5	35	100
148	C25	1402.4	420.5	35	100
149	C26	1347.4	420.5	35	100
150	C27	1292.4	420.5	35	100
151	C28	1237.4	420.5	35	100
152	C29	1182.4	420.5	35	100
153	C30	1127.4	420.5	35	100
154	C31	1072.4	420.5	35	100
155	C32	1017.4	420.5	35	100
156	C33	962.4	420.5	35	100
157	C34	907.4	420.5	35	100
158	C35	852.4	420.5	35	100
159	C36	797.4	420.5	35	100
160	C37	742.4	420.5	35	100
161	C38	687.4	420.5	35	100
162	C39	632.4	420.5	35	100
163	C40	577.4	420.5	35	100
164	C41	522.4	420.5	35	100
165	C42	467.4	420.5	35	100
166	C43	412.4	420.5	35	100
167	C44	357.4	420.5	35	100
168	C45	302.4	420.5	35	100
169	C46	247.4	420.5	35	100
170	C47	192.4	420.5	35	100
171	C48	137.4	420.5	35	100
172	C49	82.4	420.5	35	100
173	C50	27.4	420.5	35	100
174	C51	-27.6	420.5	35	100
175	C52	-82.6	420.5	35	100
176	C53	-137.6	420.5	35	100
177	C54	-192.6	420.5	35	100
178	C55	-247.6	420.5	35	100
179	C56	-302.6	420.5	35	100
180	C57	-357.6	420.5	35	100

#	Pin	X	Y	BX	BY
181	C58	-412.6	420.5	35	100
182	C59	-467.6	420.5	35	100
183	C60	-522.6	420.5	35	100
184	C61	-577.6	420.5	35	100
185	C62	-632.6	420.5	35	100
186	C63	-687.6	420.5	35	100
187	C64	-742.6	420.5	35	100
188	C65	-797.6	420.5	35	100
189	C66	-852.6	420.5	35	100
190	C67	-907.6	420.5	35	100
191	C68	-962.6	420.5	35	100
192	C69	-1017.6	420.5	35	100
193	C70	-1072.6	420.5	35	100
194	C71	-1127.6	420.5	35	100
195	C72	-1182.6	420.5	35	100
196	C73	-1237.6	420.5	35	100
197	C74	-1292.6	420.5	35	100
198	C75	-1347.6	420.5	35	100
199	C76	-1402.6	420.5	35	100
200	C77	-1457.6	420.5	35	100
201	C78	-1512.6	420.5	35	100
202	C79	-1567.6	420.5	35	100
203	C80	-1622.6	420.5	35	100
204	C81	-1677.6	420.5	35	100
205	C82	-1732.6	420.5	35	100
206	C83	-1787.6	420.5	35	100
207	C84	-1842.6	420.5	35	100
208	C85	-1897.6	420.5	35	100
209	C86	-1952.6	420.5	35	100
210	C87	-2007.6	420.5	35	100
211	C88	-2062.6	420.5	35	100
212	C89	-2117.6	420.5	35	100
213	C90	-2172.6	420.5	35	100
214	C91	-2227.6	420.5	35	100
215	C92	-2282.6	420.5	35	100
216	C93	-2337.6	420.5	35	100
217	C94	-2392.6	420.5	35	100
218	C95	-2447.6	420.5	35	100
219	C96	-2502.6	420.5	35	100
220	C97	-2557.6	420.5	35	100
221	C98	-2612.6	420.5	35	100
222	C99	-2667.6	420.5	35	100
223	C100	-2722.6	420.5	35	100
224	C101	-2777.6	420.5	35	100
225	R1	-2832.6	420.5	35	100
226	R3	-2887.6	420.5	35	100
227	R5	-2942.6	420.5	35	100
228	R7	-2997.6	420.5	35	100
229	R9	-3052.6	420.5	35	100
230	R11	-3107.6	420.5	35	100
231	R13	-3162.6	420.5	35	100
232	R15	-3217.6	420.5	35	100
233	R17	-3272.6	420.5	35	100
234	R19	-3327.6	420.5	35	100

GOLD BUMP SUMMARY

Type	W	L	Spacing
HV	35	100	20
LV/PWR	50	80	20

* *W* refers to the side along the edge of chip.
* All numbers in uM.

ALIGNMENT MARKS

Shape	X	Y	Size
Circle	196	43	45
Circle	6975	43	45