



PESD18VF1BL

Ultra low capacitance bidirectional ESD protection diode

Rev. 1— 2 September 2013

Product data sheet

1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a DFN1006-2 (SOD882) leadless ultra small Surface-Mounted Device (SMD) plastic package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Ultra low diode capacitance $C_d = 0.35$ pF
- High reverse standoff voltage $V_{RWM} = 18$ V
- Very small voltage dependency of the capacitance
- ESD protection up to ± 10 kV according to IEC 61000-4-2, level 4

3. Applications

- NFC antenna protection
- Protection of high-speed data lines

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_d	diode capacitance	$f = 1$ MHz; $V_R = 0$ V	0.28	0.35	0.5	pF
V_{RWM}	reverse standoff voltage		-	-	18	V

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	<p>Transparent top view</p>	<p>sym045</p>
2	K2	cathode (diode 2)		

DFN1006-2 (SOD882)



6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PESD18VF1BL	DFN1006-2	leadless ultra small plastic package; 2 terminals	SOD882

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD18VF1BL	WM

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	peak pulse current	$t_p = 8/20 \mu s$; IEC 61000-4-5; IEC 61643-321	[1]	-	1	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[1][2]	-	10	kV
		IEC 61000-4-2; air discharge	[1][2]	-	15	kV
		MIL-STD-883; human body model; HBM	[1]	-	10	kV
		machine model; MM	[1]	-	400	V

[1] Measured from pin 1 to pin 2.

[2] Device stressed with ten non-repetitive ESD pulses.

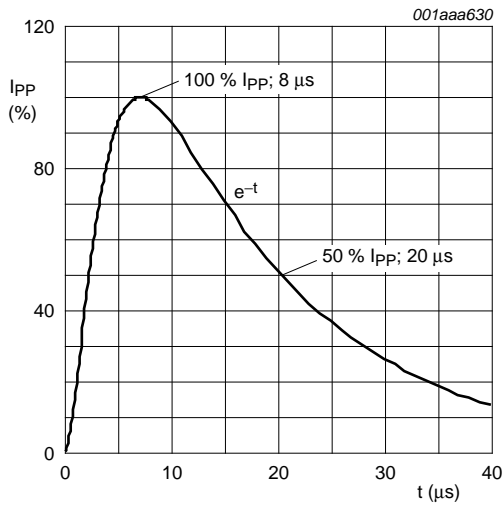


Fig 1. 8/20 μs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

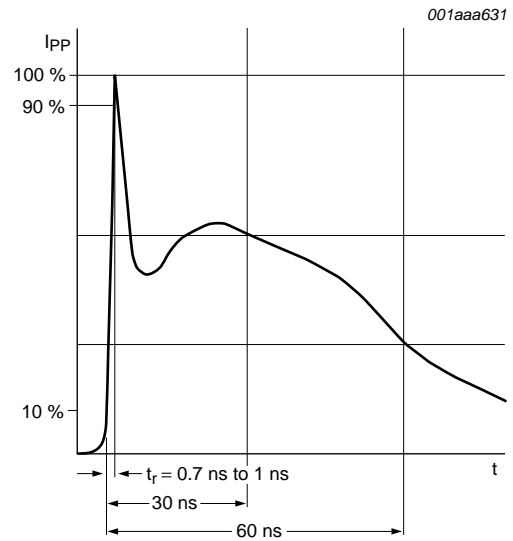


Fig 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{RWM}	reverse standoff voltage		-	-	18	V
I _{RM}	reverse leakage current	V _R = 18 V	-	1	30	nA
V _{CL}	clamping voltage	I _{PP} = 1 A; t _p = 8/20 μs; IEC 61000-4-5; IEC 61643-321	-	-	17	V
V _{BR}	breakdown voltage	I _R = 10 mA	19	22	24	V
C _d	diode capacitance	f = 1 MHz; V _R = 0 V	0.28	0.35	0.5	pF
R _{dyn}	dynamic resistance	I _R = 10 A	-	0.8	-	Ω

[1] Measured from pin 1 to pin 2.

[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANSI / ESD STM5.1-2008.

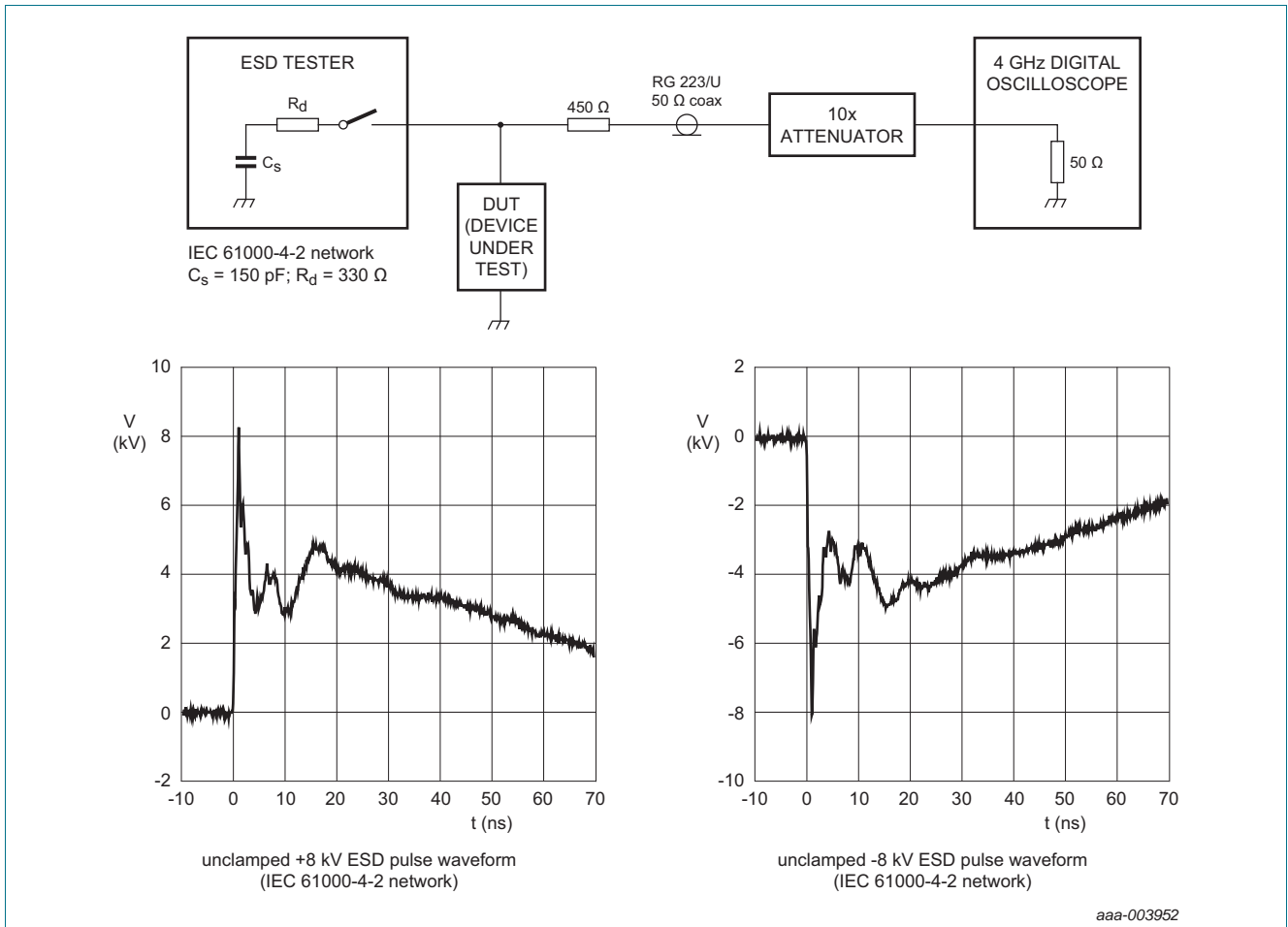


Fig 3. ESD clamping test setup and waveforms

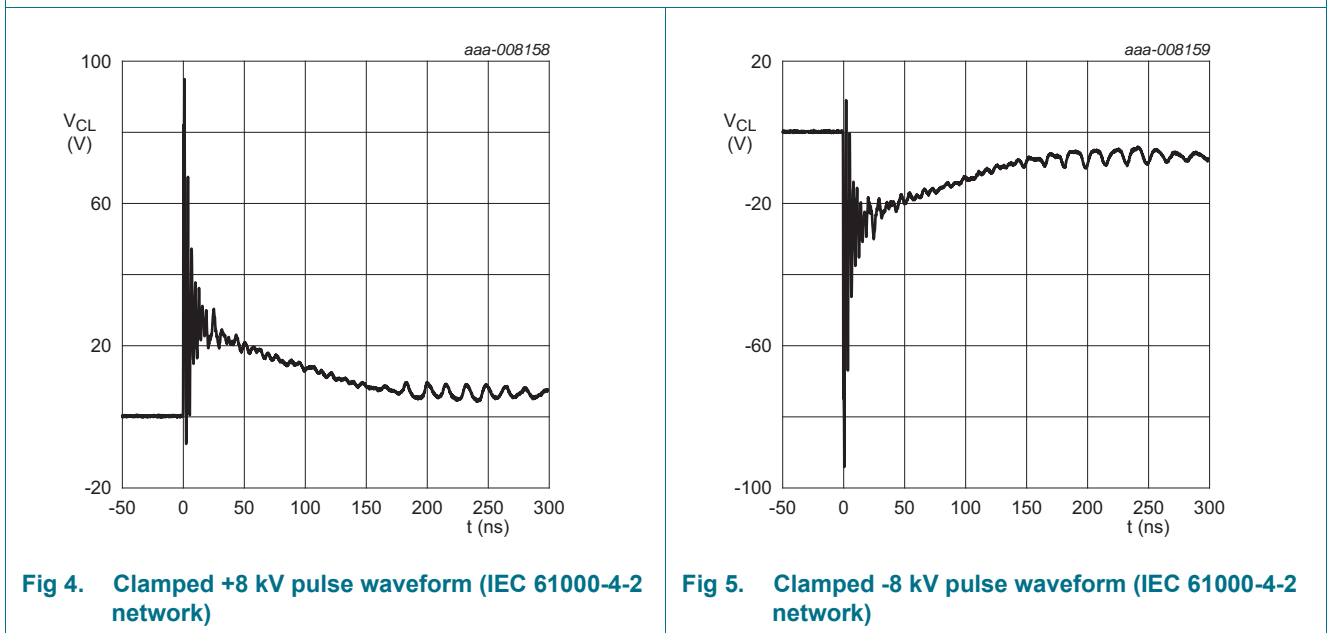
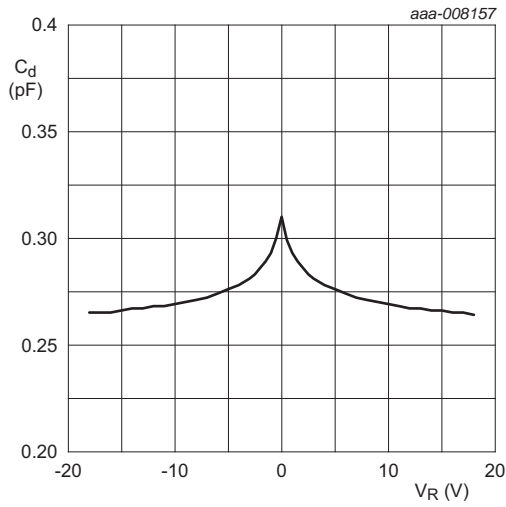


Fig 4. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

Fig 5. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)



$f = 1 \text{ MHz}; V_R = 0 \text{ V}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$

Fig 6. Diode capacitance as a function of reverse voltage; typical values

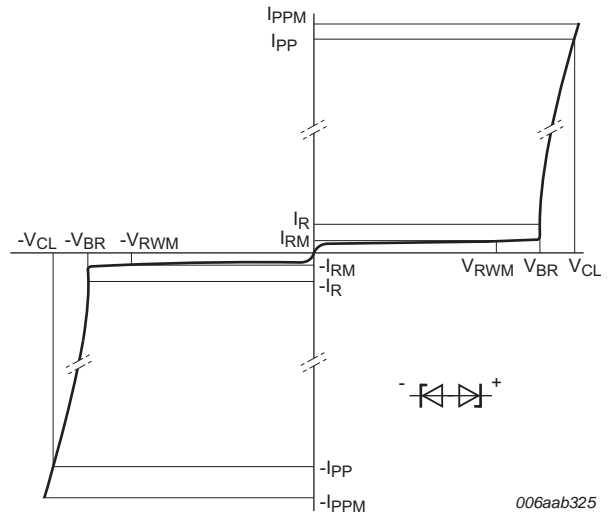
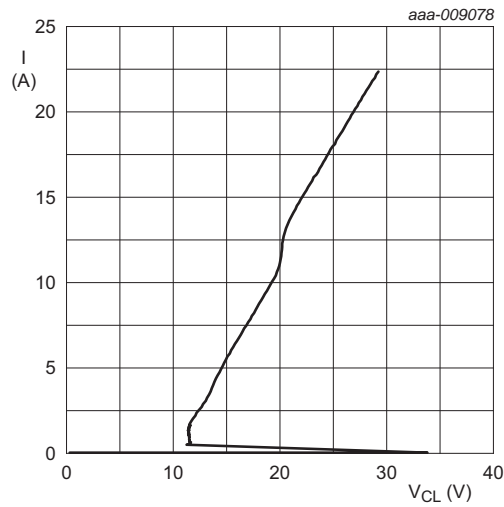


Fig 7. V-I characteristics for a bidirectional ESD protection diode



$t_p = 100 \text{ ns}; \text{Transmission Line Pulse (TLP)}$

Fig 8. Dynamic resistance

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

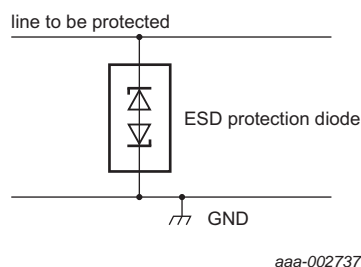


Fig 9. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

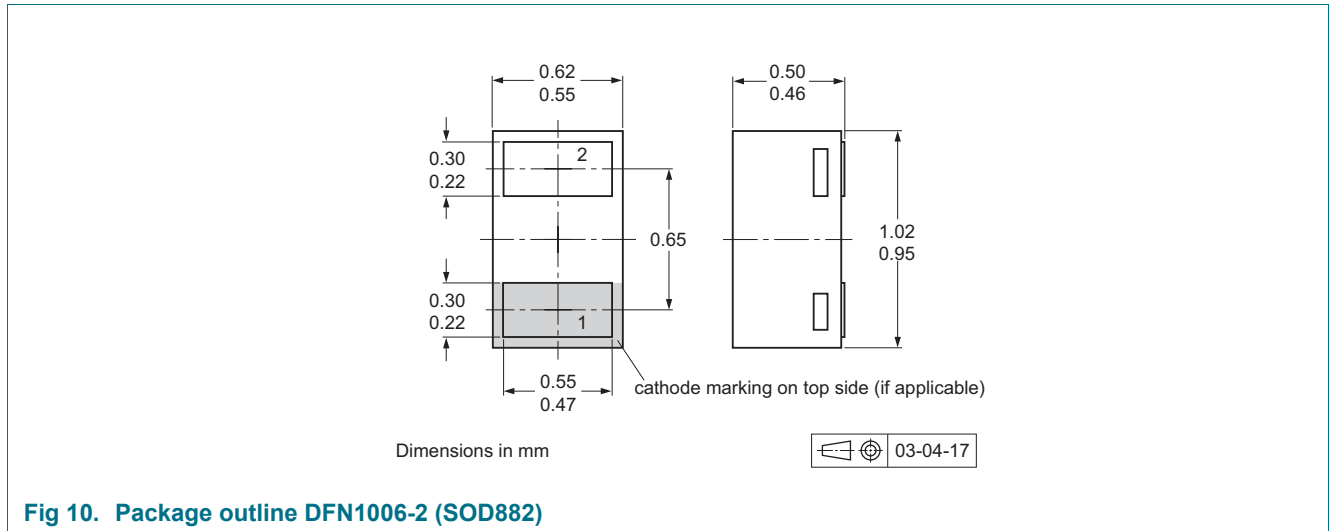


Fig 10. Package outline DFN1006-2 (SOD882)

12. Soldering

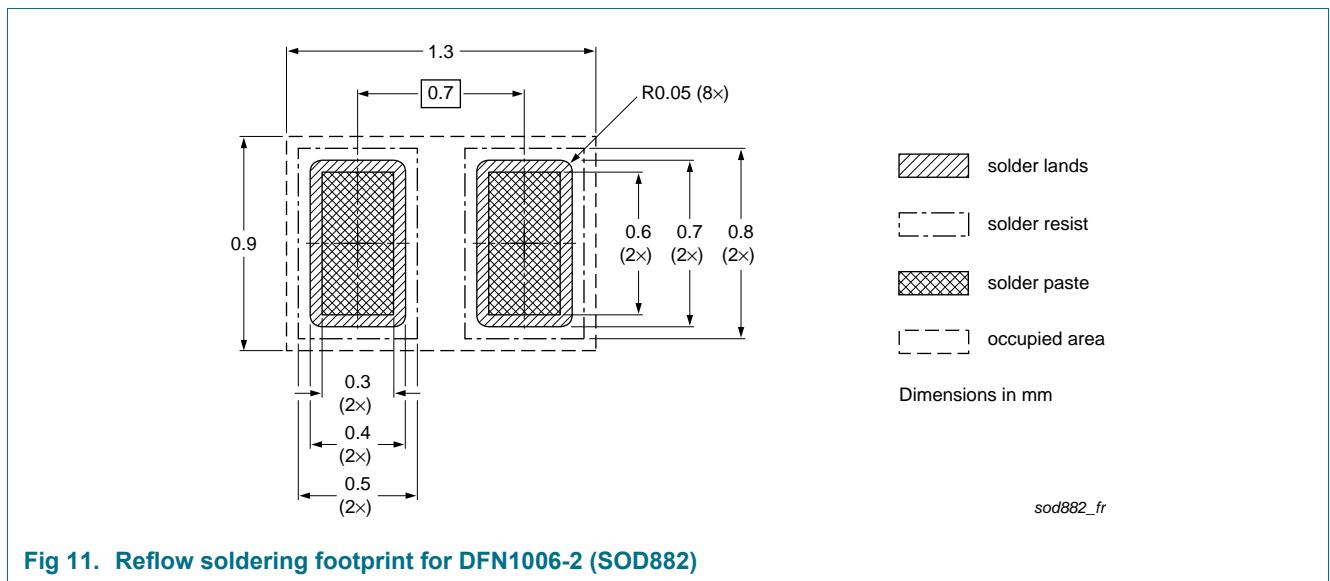


Fig 11. Reflow soldering footprint for DFN1006-2 (SOD882)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD18VF1BL v.1	20130902	Product data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status ^[1] [2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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16. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	1
6	Ordering information	2
7	Marking	2
8	Limiting values	2
9	Characteristics	3
10	Application information	6
11	Package outline	7
12	Soldering	7
13	Revision history	8
14	Legal information	9
14.1	Data sheet status	9
14.2	Definitions	9
14.3	Disclaimers	9
14.4	Trademarks	10
15	Contact information	10

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