Ordering number : ENA0646

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA73033M — I²C bus control (excluding standby control and RGB through control)

Overview

This LA73033M is DVD recorder video signal input SW & output driver.

Functions

[SW side]

- Composite signal five-input SW and S signal three-input SW
- Keyed clamp
- Component signal or RGB signal 1 input
- 0dB/ 6dB amplifier
- AGC amplifier (composite and Y signal only)
- LPF for removal of 13.5MHz clock
- Composite output/ Y output changeover switch
- Compatible with standby (two types)
- C.SYNC & V.SYNC output

[Driver side]

- Six-channel input & six-channel output of composite signal & S signal & component or RGB signal
- Clamp (keyed clamp for Cb and Cr)
- 6dB/ 9dB amplifier amplifier
- LPF for removal of 27MHz/ 54MHz clock
- Output mute (three types)
- 75Ω driver (two drives possible)
- Through changeover of RGB signal from the SW side
- Y/ C-MIX
- DC output for S1/ S2
- SCART-RGB/ YC changeover SW

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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Allowable power dissipation	Pd max	Ta ≤ 75°C * Mounted on a board	1200	mW
Operating temperature	Topg		-20 to +75	°C
Storage temperature	Tstg		-40 to +150	°C

* Mounted on a board : 114.3×76.1×1.6mm^3, glass epoxy board.

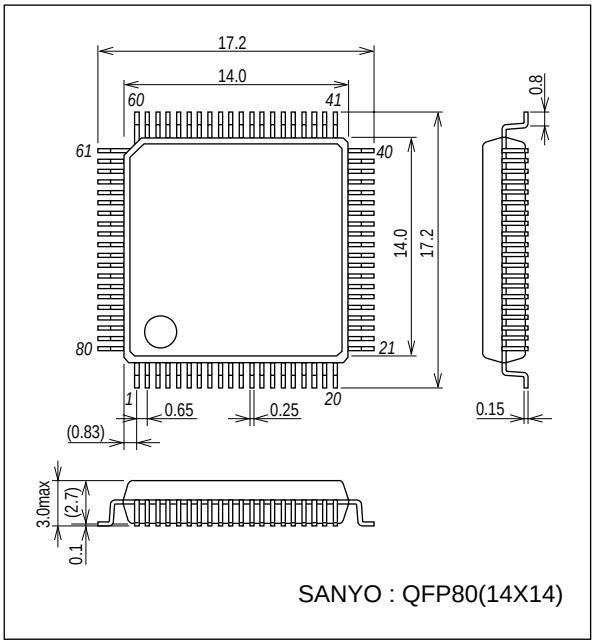
Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5.0	V
Operating supply voltage range	V_{CC} opg		4.75 to 5.25	V
Input pin voltage application range	V_{IN}	V_{CC} opg +0.3 ≤ 7V	-0.3 to V_{CC} opg +0.3	V

Package Dimensions

unit : mm (typ)

3255



Electrical Characteristics at Ta = 25°C, V_{CC} = 5.0V

Parameter	Symbol	Input signal				Out	Test Condition	Spec			unit		Control voltage			I^2C bus data (MSB-LSB)	
		Point	Signal	Freq	Mag	Point		min	typ	max		R1	V18	V38	V30, V35	SW1	SW2
Current drain 1	$I_{CC}11$					$V_{CC}1$	Current flowing through $V_{CC}1$ at no signal	58	73	88	mA	330	0	0	3.5	01000010	00000000
Current drain at standby	$I_{CC}12$					$V_{CC}1$	Current flowing through $V_{CC}1$ at standby control	9	11	13	mA	330	3	0			
Current drain 1 at RGB standby	$I_{CC}13$					$V_{CC}1$	Current flowing through $V_{CC}1$ at EXT-RGB control	11	14	17	mA	330	3	3			
Composite output clamp voltage	C23	$V_{IN}13$ $V_{IN}15$ $V_{IN}17$ $V_{IN}19$ $V_{IN}21$	SG3		1Vp-p	T27	Measure the output clamp voltage (sink chip voltage)	0.7	0.8	0.9	V	330	0	0	3.5	01001010 01101010 10001010 10101010 11001010	00000000 00000000 00000000 00000000 00000000
Chroma output center voltage	C25	$V_{IN}7$ $V_{IN}5$ $V_{IN}3$	SG2		714mVp-p	T25	Measure the output DC voltage (center voltage)	2.2	2.4	2.7	V	330	0	0	3.5	01000100 01100100 10000100	00000000 00000000 00000000
Y output clamp voltage	C27	$V_{IN}79$ $V_{IN}77$ $V_{IN}75$	SG1		1Vp-p	T27	Measure the output clamp voltage (sink chip voltage)	0.7	0.8	0.9	V	330	0	0	3.5	01000100 01100100 10000100	00000000 00000000 00000000
Component output pedestal voltage	 PC23 PC25	$V_{IN}1$ $V_{IN}11$ $V_{IN}9$	SG5 SG6 SG6		1Vp-p 1Vp-p 1Vp-p	 T23 T25	Measure the output pedestal clamp voltage	2.4	2.5	2.6	V	330	0	0	3.5	00000100	00000000
RGB output clmap voltage	RC23 RC25 RC29	$V_{IN}11$ $V_{IN}9$ $V_{IN}1$ $V_{IN}73$	SG8 SG8 SG5 SG8		700mVp-p 700mVp-p 1Vp-p 700mVp-p	T23 T25 T29	Measure the output pedestal clamp voltage	1.15	1.25	1.35	V	330	0	0	3.5	00100100	00000000
Gain at 6dB	G23H G25H G27H	$V_{IN}13$ $V_{IN}7$ $V_{IN}79$	SG5 SG6 SG5		1Vp-p 714mVp-p 1Vp-p	T27 T25 T27	Measure GAIN for input of each output	5.5	6	6.5	dB	330	0	0	3.5	01001010 01000100 01001000	00000000 00000000 00000000
	G23H G25H G27H G29H	$V_{IN}11$ $V_{IN}9$ $V_{IN}1$ $V_{IN}73$	SG8 SG8 SG5 SG8		700mVp-p 700mVp-p 1Vp-p 700mVp-p	T23 T25 T27 T29							0	0	3.5	00101100	00000000

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Parameter	Symbol	Input signal				Out	Test Condition	Spec			unit		Control voltage			I^2C bus data (MSB-LSB)	
		Point	Signal	Freq	Mag	Point		min	typ	max		R1	V18	V38	V30, V35	SW1	SW2
Gain at 0dB	G23L	$V_{IN}13$	SG5		2Vp-p	T27	Measure GAIN for input of each output	-0.5	0	0.5	dB	330	0	0	3.5	01000010	00000000
	G25L	$V_{IN}7$	SG6		1.428Vp-p	T25										01000000	00000000
	G27L	$V_{IN}79$	SG5		2Vp-p	T27										01000000	00000000
	G23H	$V_{IN}11$	SG8		1.4Vp-p	T23										00100000	00000000
	G25H	$V_{IN}9$	SG8		1.4Vp-p	T25											
	G27H	$V_{IN}1$	SG5		2Vp-p	T27											
	G29H	$V_{IN}73$	SG8		1.4Vp-p	T29											
AGC-AMP control voltage	VA23M	$V_{IN}13$	SG5		1Vp-p	T27	Measure V30 and V35 where the output gain changeable.	2	3.5	5	V	330	0	0	VA23M	01001010	10000000
	VA27M	$V_{IN}79$	SG5		1Vp-p	T27									VA27M	01001000	10000000
10MHz change rate for f characteristics of gain	F23	$V_{IN}13$	SG3	10MHz	1Vp-p	T27	Measure gain for input of each output and calculates the change rate for gain at 100kHz.	-0.5	-0.1	0.5	dB	330	0	0	3.5	01001010	00000000
	F25	$V_{IN}7$	SG2	10MHz	714mVp-p	T25										01000100	00000000
	F27	$V_{IN}79$	SG1	10MHz	1Vp-p	T27										01001000	00000000
	F23	$V_{IN}11$	SG9	10MHz	700mVp-p	T23										00101100	00000000
	F25	$V_{IN}9$	SG9	10MHz	700mVp-p	T25											
	F27	$V_{IN}1$	SG1	10MHz	1Vp-p	T27											
	F29	$V_{IN}73$	SG9	10MHz	700mVp-p	T29											
4.5MHz change rate of f characterics of gain (with LPF)	F23L1	$V_{IN}13$	SG3	4.5MHz	1Vp-p	T27	Measure gain for input of each output and calculates the change rate for gain at 100kHz.	-0.5	-0.2	0.5	dB	1k	0	0	3.5	01011010	00000000
	F25L1	$V_{IN}7$	SG2	4.5MHz	714mVp-p	T25										01010100	00000000
	F27L1	$V_{IN}79$	SG1	4.5MHz	1Vp-p	T27										01011000	00000000
	F23L1	$V_{IN}11$	SG9	4.5MHz	700mVp-p	T23										00111100	00000000
	F25L1	$V_{IN}9$	SG9	4.5MHz	700mVp-p	T25											
	F27L1	$V_{IN}1$	SG1	4.5MHz	1Vp-p	T27											
	F29L1	$V_{IN}73$	SG9	4.5MHz	700mVp-p	T29											
5MHz change rate of f characterics of gain (with LPF)	F23L2	$V_{IN}13$	SG3	5MHz	1Vp-p	T27	Measure gain for input of each output and calculates the change rate for gain at 100kHz.	-1	-0.3	0.5	dB	1k	0	0	3.5	01011010	00000000
	F25L2	$V_{IN}7$	SG2	5MHz	714mVp-p	T25										01010100	00000000
	F27L2	$V_{IN}79$	SG1	5MHz	1Vp-p	T27										01011000	00000000
	F23L2	$V_{IN}11$	SG9	5MHz	700mVp-p	T23										00111100	00000000
	F25L2	$V_{IN}9$	SG9	5MHz	700mVp-p	T25											
	F27L2	$V_{IN}1$	SG1	5MHz	1Vp-p	T27											
	F29L2	$V_{IN}73$	SG9	5MHz	700mVp-p	T29											

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Parameter	Symbol	Input signal				Out	Test Condition	Spec			unit		Control voltage			I^2C bus data (MSB-LSB)	
		Point	Signal	Freq	Mag	Point		min	typ	max		R1	V18	V38	V30, V35	SW1	SW2
13.5 MHz change rate of f characteristics of gain (with LPF)	F23L3	$V_{IN}13$	SG3	13.5MHz	1Vp-p	T27	Measure gain for input of each output and calculates the change rate for gain at 100kHz.		-41	-30	dB	1k	0	0	3.5	01011010	00000000
	F25L3	$V_{IN}7$	SG2	13.5MHz	714mVp-p	T25										01010100	00000000
	F27L3	$V_{IN}79$	SG1	13.5MHz	1Vp-p	T27										01011000	00000000
	F23L3	$V_{IN}11$	SG9	13.5MHz	700mVp-p	T23										00111100	00000000
	F25L3	$V_{IN}9$	SG9	13.5MHz	700mVp-p	T25											
	F27L3	$V_{IN}1$	SG1	13.5MHz	1Vp-p	T27											
	F29L3	$V_{IN}73$	SG9	13.5MHz	700mVp-p	T29											
Output drive capacity 1 (secondary distortion)	H23	$V_{IN}13$	SG3	5MHz	1Vp-p	T27	Connect the load of 330Ω to the output via C connection and measure the secondary distortion of output.		-45	-35	dB	330	0	0	3.5	01001010	00000000
	H25	$V_{IN}7$	SG2	5MHz	714mVp-p	T25										01000100	00000000
	H27	$V_{IN}79$	SG1	5MHz	1Vp-p	T27										01001000	00000000
	H23	$V_{IN}11$	SG9	5MHz	700mVp-p	T23										00101100	00000000
	H25	$V_{IN}9$	SG9	5MHz	700mVp-p	T25											
	H27	$V_{IN}1$	SG1	5MHz	1Vp-p	T27											
	H29	$V_{IN}73$	SG9	5MHz	700mVp-p	T29											
Output drive capacity 1 (secondary distortion) (with LPF)	H23	$V_{IN}13$	SG3	5MHz	1Vp-p	T27	Connect the load of 1kΩ to the output via C connection and measure the secondary distortion of output.		-45	-35	dB	330	0	0	3.5	01011010	00000000
	H25	$V_{IN}7$	SG2	5MHz	714mVp-p	T25										01010100	00000000
	H27	$V_{IN}79$	SG1	5MHz	1Vp-p	T27										01011000	00000000
	H23	$V_{IN}11$	SG9	5MHz	700mVp-p	T23										00111100	00000000
	H25	$V_{IN}9$	SG9	5MHz	700mVp-p	T25											
	H27	$V_{IN}1$	SG1	5MHz	1Vp-p	T27											
	H29	$V_{IN}73$	SG9	5MHz	700mVp-p	T29											
C.SYNC output H voltage	V36H	$V_{IN}13$	SG5		1Vp-p	T36	Connect 10kΩ between this output and V_{CC}.	4.75	5	5.25	V		0	0	3.5	01001010	00000000
		$V_{IN}79$	SG5		1Vp-p											01001000	00000000
C.SYNC output L voltage	V36L	$V_{IN}13$	SG5		1Vp-p	T36	Connect 10kΩ between this output and V_{CC}.	0	0.3	0.6	V		0	0	3.5	01001010	00000000
		$V_{IN}79$	SG5		1Vp-p											01001000	00000000
C.SYNC2 output H voltage	V37H	$V_{IN}13$	SG5		1Vp-p	T37	Connect 10kΩ between this output and V_{CC}.	4.75	5	5.25	V		0	0	3.5	01001010	00000000
		$V_{IN}79$	SG5		1Vp-p											01001000	00000000
C.SYNC2 output L voltage	V37L	$V_{IN}13$	SG5		1Vp-p	T37	Connect 10kΩ between this output and V_{CC}.	0	0.3	0.6	V		0	0	3.5	01001010	00000000
		$V_{IN}79$	SG5		1Vp-p											01001000	00000000

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Parameter	Symbol	Input signal				Out	Test Condition	Spec			unit		Control voltage			I^2C bus data (MSB-LSB)	
		Point	Signal	Freq	Mag	Point		min	typ	max		R1	V18	V38	V30, V35	SW1	SW2
C.SYNC output pulse width	W36	$V_{IN}13$	SG5		1Vp-p	T36	Output pulse width	3.2	4.2	5.2	µs		0	0	3.5	01001010	00000000
		$V_{IN}79$	SG5		1Vp-p											01001000	00000000
C.SYNC threshold level	W36V	$V_{IN}13$	SG5		1Vp-p	T36	The value of input SYNC at which the output pulse width becomes 1.3-folds or more as the input SYNC is reduced.	7.5	11.5	15.5	IRE		0	0	3.5	01001010	00000000
		$V_{IN}79$	SG5		1Vp-p											01001000	00000000

(Note) The C. SYNC2 threshold level is 12 IRE at 6dB and 12.8 IRE at 0dB .

Design guarantee items

Parameter	Symbol	Input signal				Out	Test Condition	Spec			unit		Control voltage			I^2C bus data (MSB-LSB)	
		Point	Signal	Freq	Mag	Point		min	typ	max		R1	V18	V38	V30, V35	SW1	SW2
DG	DG23	$V_{IN}13$	SG7	3.58MHz	1Vp-p	T27	Ratio of the amplitude on the white level relative to that on the black level.	-2	1	2	%	1k	0	0	3.5	01011010	00000000
	DG27	$V_{IN}79$	SG7	3.58MHz	1Vp-p	T27										01011000	00000000
	ADG23	$V_{IN}13$	SG7	3.58MHz	1Vp-p	T27	When AGC amplifier is used	-2	1	2	%				VA23M	01011010	10000000
	ADG27	$V_{IN}79$	SG7	3.58MHz	1Vp-p	T27									VA27M	01011000	10000000
DP	DP23	$V_{IN}13$	SG7	3.58MHz	1Vp-p	T27	Difference of the phase on the white level relative to that on the black level	-1	1	1.5	deg	1k	0	0	3.5	01011010	00000000
	DP27	$V_{IN}79$	SG7	3.58MHz	1Vp-p	T27										01011000	00000000
	ADP23	$V_{IN}13$	SG7	3.58MHz	1Vp-p	T27	When AGC amplifier is used	-1	1.2	2	deg				VA23M	01011010	10000000
	ADP27	$V_{IN}79$	SG7	3.58MHz	1Vp-p	T27									VA27M	01011000	10000000
Crosstalk	CT23	$V_{IN}13$	SG5		1Vp-p	T27	The magnitude of crosstalk in which the non-selected input signal is carried on the selected signal output is specified by the value of selected signal output.		-60	-55	dB	330	0	0	3.5	01001010	00000000
		$V_{IN}15$	SG5		1Vp-p												
	CT25	$V_{IN}7$	SG2	4MHz	714mVp-p	T25			-60	-55	dB	330	0	0	3.5	01000100	00000000
		$V_{IN}5$	SG2	4MHz	714mVp-p												
	CT27	$V_{IN}79$	SG5		1Vp-p	T27			-60	-55	dB	330	0	0	3.5	01001000	00000000
		$V_{IN}77$	SG5		1Vp-p												
Video S/ N ratio	SN23	$V_{IN}13$	SG5		1Vp-p	T27	S/ N in the HPF100kHz and LPF 10MHz bands is expressed in dB.		-70	-65	dB	330	0	0	3.5	01001010	00000000
	SN27	$V_{IN}79$	SG5		1Vp-p	T27										01001000	00000000
Video S/ N ratio (with LPF)	SN23	$V_{IN}13$	SG5		1Vp-p	T27	S/ N in the HPF100kHz and LPF 10MHz bands is expressed in dB.		-65	-60	dB	1k	0	0	3.5	01011010	00000000
	SN27	$V_{IN}79$	SG5		1Vp-p	T27										01011000	00000000

Electrical characteristics at Ta=25°C, unless otherwise specified V_{CC} = 5.0V

Parameter	Symbol	Input signal				Out	Test Condition	Spec			unit	Control voltage		SW		I^2C bus data (MSB-LSB)	
		Point	Signal	Freq	Mag	Point		min	typ	max		V18	V38	S68, S65, S63	S60, S58, S56	DV1	DV2
Current drain 2	$I_{CC}21$					$V_{CC}2$	Current flowing through $V_{CC}2$ at no signal	64	80	96	mA	0	0	ON	ON	00000000	00110000
Current drain at RGB standby 2	$I_{CC}23$					$V_{CC}2$	Current flowing through $V_{CC}2$ at EXT-RGB control	18	22	26	mA	3	3	ON	ON		
Gain at 6dB for two drives	G68L	$V_{IN}39$	SG3		1Vp-p	T68	Measure gain of each output relative to input	5.6	5.9	6.4	dB	0	0	ON	ON	00000000	00110000
	G65L	$V_{IN}41$	SG2		714mVp-p	T65											
	G63L	$V_{IN}43$	SG1		1Vp-p	T63											
	G60L	$V_{IN}45$	SG5		1Vp-p	T60											
	G58L	$V_{IN}51$	SG6		1Vp-p	T58											
	G56L	$V_{IN}53$	SG6		1Vp-p	T56											
Gain at 9dB for two drives	G68H	$V_{IN}39$	SG3		709mVp-p	T68	Measure gain of each output relative to input	8.55	8.9	9.45	dB	0	0	ON	ON	00000000	11110000
	G65H	$V_{IN}41$	SG2		507mVp-p	T65											
	G63H	$V_{IN}43$	SG1		709mVp-p	T63											
	G60H	$V_{IN}45$	SG5		709mVp-p	T60											
	G58H	$V_{IN}51$	SG6		709mVp-p	T58											
	G56H	$V_{IN}53$	SG6		709mVp-p	T56											
Gain at 6dB for one drive in two-drive mode	G68L	$V_{IN}39$	SG3		1Vp-p	T68	Measure gain of each output relative to input	5.6	6.1	6.4	dB	0	0	OFF	ON	00000000	00110000
	G65L	$V_{IN}41$	SG2		714mVp-p	T65											
	G63L	$V_{IN}43$	SG1		1Vp-p	T63											
	G60L	$V_{IN}45$	SG5		1Vp-p	T60											
	G58L	$V_{IN}51$	SG6		1Vp-p	T58											
	G56L	$V_{IN}53$	SG6		1Vp-p	T56											
Gain at 9dB for one drive in two-drive mode	G68H	$V_{IN}39$	SG3		709mVp-p	T68	Measure gain of each output relative to input	8.55	9.1	9.45	dB	0	0	ON	OFF	00000000	11110000
	G65H	$V_{IN}41$	SG2		507mVp-p	T65											
	G63H	$V_{IN}43$	SG1		709mVp-p	T63											
	G60H	$V_{IN}45$	SG5		709mVp-p	T60											
	G58H	$V_{IN}51$	SG6		709mVp-p	T58											
	G56H	$V_{IN}53$	SG6		709mVp-p	T56											
Output gain ratio (composite/ S)	Δ68/65	$V_{IN}39$	SG3		709mVp-p	T68	Calculate the gain ratio of two outputs.	-5	0	5	%	0	0	ON	ON	00000000	11110000
	Δ68/63	$V_{IN}41$	SG2		507mVp-p	T65											
	Δ65/63	$V_{IN}43$	SG1		709mVp-p	T63											

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Parameter	Symbol	Input signal				Out	Test Condition	Spec			unit	Control voltage		SW		I^2C bus data (MSB-LSB)	
		Point	Signal	Freq	Mag	Point		min	typ	max		V18	V38	S68, S65, S63	S60, S58, S56	DV1	DV2
Output gain ratio (component)	Δ60/58 Δ60/56 Δ58/56	$V_{IN}45$ $V_{IN}51$ $V_{IN}53$	SG5 SG6 SG6		709mVp-p 709mVp-p 709mVp-p	T60 T58 T56	Calculate the gain ratio of two outputs.	-5	0	5	%	0	0	ON	ON	00000000	11110000
7MHz change rate for f characteristics of GAIN	F68L F65L F63L	$V_{IN}39$ $V_{IN}41$ $V_{IN}43$	SG3 SG2 SG1	7MHz 7MHz 7MHz	1Vp-p 714mVp-p 1Vp-p	T68 T65 T63	Measure gain of each output relative to input and calculate the change rate for gain at 100kHz.	-2	-0.8	0.4	dB	0	0	ON	ON	00000000	00110000
	F60L1 F58L1 F56L1	$V_{IN}45$ $V_{IN}51$ $V_{IN}53$	SG1 SG4 SG4	7MHz 7MHz 7MHz	1Vp-p 1Vp-p 1Vp-p	T60 T58 T56											
27MHz change rate of f characteristics of GAIN	F68H F65H F63H	$V_{IN}39$ $V_{IN}41$ $V_{IN}43$	SG3 SG2 SG1	27MHz 27MHz 27MHz	1Vp-p 714mVp-p 1Vp-p	T68 T65 T63	Measure gain of each output relative to input and calculate the change rate for gain at 100kHz.		-33	-25	dB	0	0	ON	ON	00000000	00110000
	F60H1 F58H1 F56H1	$V_{IN}45$ $V_{IN}51$ $V_{IN}53$	SG1 SG4 SG4	27MHz 27MHz 27MHz	1Vp-p 1Vp-p 1Vp-p	T60 T58 T56											
14MHz change rate for f characteristics of GAIN	F60L2 F58L2 F56L2	$V_{IN}45$ $V_{IN}51$ $V_{IN}53$	SG1 SG4 SG4	14MHz 14MHz 14MHz	1Vp-p 1Vp-p 1Vp-p	T60 T58 T56	Measure gain of each output relative to input and calculate the change rate for gain at 100kHz.	-2.3	-1.1	0.1	dB	0	0	ON	ON	00001000	00110000
54MHz change rate for f characteristics of GAIN	F60H2 F58H2 F56H2	$V_{IN}45$ $V_{IN}51$ $V_{IN}53$	SG1 SG4 SG4	54MHz 54MHz 54MHz	1Vp-p 1Vp-p 1Vp-p	T60 T58 T56			-37	-30	dB					00001000	00110000
Gain at RGB through One drive	G60E G58E G56E	$V_{IN}9$ $V_{IN}11$ $V_{IN}73$	SG8 SG8 SG8		700mVp-p 700mVp-p 700mVp-p	T60 T58 T56	Measure gain of each output relative to input. Two-drive mode.	5.6	6.1	6.4	dB	0	3	ON	OFF	10000000	00100000
10MHz change rate for f characteristics of GAIN at RGB through	F60E F58E F56E	$V_{IN}9$ $V_{IN}11$ $V_{IN}73$	SG9 SG9 SG9	10MHz 10MHz 10MHz	700mVp-p 700mVp-p 700mVp-p	T60 T58 T56	Measure gain of each output relative to input and calculate the change rate for gain at 100kHz.	-0.5	-0.1	0.5	dB	0	3	ON	OFF	10000000	00100000
Gain at RGB standby One drive	G60E G58E G56E	$V_{IN}9$ $V_{IN}11$ $V_{IN}73$	SG8 SG8 SG8		700mVp-p 700mVp-p 700mVp-p	T60 T58 T56	Measure gain of each output relative to input.	5.6	5.9	6.4	dB	3	3	ON	OFF		

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Parameter	Symbol	Input signal				Out	Test Condition	Spec			unit	Control voltage		SW		I^2C bus data (MSB-LSB)	
		Point	Signal	Freq	Mag	Point		min	typ	max		V18	V38	S68, S65, S63	S60, S58, S56	DV1	DV2
MUTE voltage	V65MD V63MD					T65 T63	Measure the pin voltage.	2.1	2.5	2.9	V	0	0	ON	ON	00000010	00110000
	V60MD V58MD V56MD					T60 T58 T56										00000001 00000100	00110000 00110000
DC for SQ	VSQ					T66	Measure the pin voltage with V_{CC} = 4.75 to 5.25V	4.1	4.4	4.7	V	0	0	ON	ON	00100000	00110000
DC for LB	VLB					T66		2.05	2.2	2.35	V	0	0	ON	ON	00010000	00110000
DC for 4 : 3	V43					T66		0	0	0.35	V	0	0	ON	ON	00000000	00110000

Design guarantee items

Parameter	Symbol	Input signal				Out	Test Condition	Spec			unit	Control voltage		SW		I^2C bus data (MSB-LSB)	
		Point	Signal	Freq	Mag	Point		min	typ	max		V18	V38	S68, S65, S63	S60, S58, S56	DV1	DV2
f characteristcs of group delay at 7MHz (interlace)	GD68 GD65 GD63	V_{IN}39 V_{IN}41 V_{IN}43	SG3 SG2 SG1	7MHz 7MHz 7MHz	1Vp-p 714mVp-p 1Vp-p	T68 T65 T63	Difference in group delay of 7MHz relative to 100kHz of each output	-20	10	20	ns	0	0	ON	ON	00000000	00110000
	GD60-1 GD58-1 GD56-1	V_{IN}45 V_{IN}51 V_{IN}53	SG1 SG4 SG4	7MHz 7MHz 7MHz	1Vp-p 714mVp-p 714mVp-p	T60 T58 T56											
f characteristics of group delay at 14MHz (progressive)	GD60-2 GD58-2 GD56-2	V_{IN}45 V_{IN}51 V_{IN}53	SG1 SG4 SG4	14MHz 14MHz 14MHz	1Vp-p 714mVp-p 714mVp-p	T60 T58 T56	Difference in group delay of 14MHz from 100kHz of each output	-15	5	15	ns	0	0	ON	ON	00001000	00110000
DG	DG68 DG63 DG60	V_{IN}39 V_{IN}43 V_{IN}45	SG7 SG7 SG7	3.58MHz 3.58MHz 3.58MHz	1Vp-p 1Vp-p 1Vp-p	T68 T63 T60	Calculate the ratio in percentage of the amplitude of SIN wave on the white level relative to that of SIN wave on the black level of each output signal.		1	2	%	0	0	ON	ON	00000000	00110000
	DGMIX	V_{IN}41 V_{IN}43	SG2 SG7	3.58MHz Y only component	286mVp-p 1Vp-p	T68										01000000	00110000

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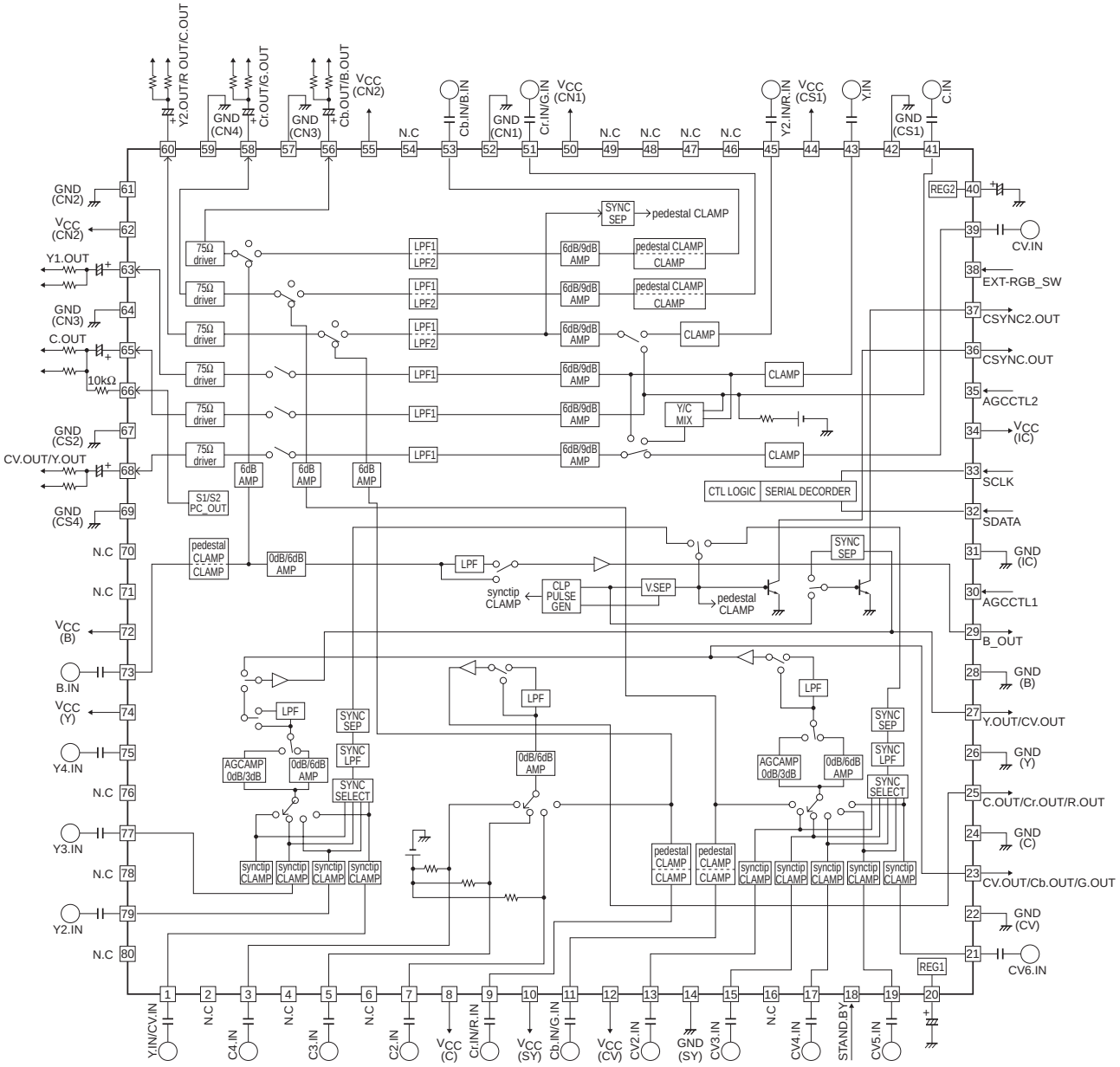
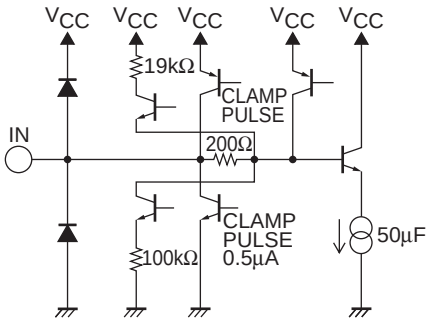
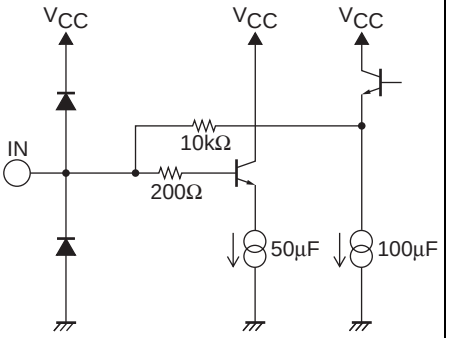
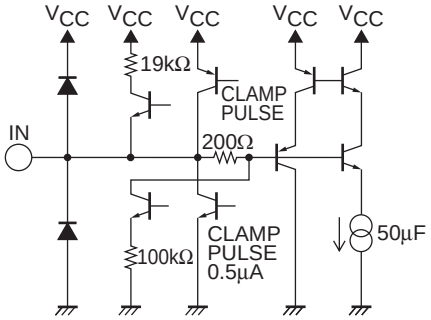
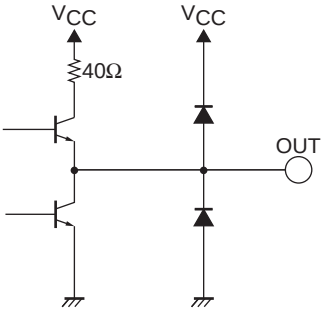
Parameter	Symbol	Input signal				Out	Test Condition	Spec			unit	Control voltage		SW		I^2C bus data (MSB-LSB)	
		Point	Signal	Freq	Mag	Point		min	typ	max		V18	V38	S68, S65, S63	S60, S58, S56	DV1	DV2
DP	DP68	$V_{IN}39$	SG7	3.58MHz	1Vp-p	T68	Measure the difference in phase of the SIN wave on the black level of each output signal relative to that of SIN wave on the white level.	-1	0.5	1	deg	0	0	ON	ON	00000000	00110000
	DP63	$V_{IN}43$	SG7	3.58MHz	1Vp-p	T63											
	DP60	$V_{IN}45$	SG7	3.58MHz	1Vp-p	T60											
	DPMIX	$V_{IN}41$	SG2	3.58MHz	286mVp-p	T68										01000000	00110000
		$V_{IN}43$	SG7	Y only component	1Vp-p												
Crosstalk	CT68	$V_{IN}39$	SG3	4MHz	1Vp-p	T68	Measure the 4MHz component of the otput of non-input route and calculate its ratio relative to the 4MHz amplitude of other outputs.		-60	-55	dB	0	0	ON	ON	00000000	00110000
	CT65	$V_{IN}41$	SG2	4MHz	714mVp-p	T65											
	CT63	$V_{IN}43$	SG1	4MHz	1Vp-p	T63											
	CT60	$V_{IN}45$	SG1	4MHz	1Vp-p	T60											
	CT58	$V_{IN}51$	SG4	4MHz	714mVp-p	T58											
	CT56	$V_{IN}53$	SG4	4MHz	714mVp-p	T56											
Video S/ N ratio	SN68	$V_{IN}39$	SG5		1Vp-p	T68	Measure the S/ N ratio of output signal with a noise meter (LPF 10MHz, HPF 100kHz) and express it in dB.		-79	-77	dB	0	0	ON	ON	00000000	00110000
	SN63	$V_{IN}43$	SG5		1Vp-p	T63											
	SN60	$V_{IN}45$	SG5		1Vp-p	T60											
	SNMIX	$V_{IN}43$	SG5		1Vp-p	T68			-73	-71	dB	0	0	ON	ON	01000000	00110000

Block Diagram and Test Circuits



Pin Functions

Pin No.	Pin name	I/0	Impedance	DC voltage	Pin Explanation	Input/Output form
13 15 17 19 21 1 79 77 75	CV2.IN CV3.IN CV4.IN CV5.IN CV6.IN Y1.IN / CV.IN Y2.IN Y3.IN Y4.IN	I	Clamp Form	1.5V at 0dB 2.1V at 6dB 1.5V at AGC 1.5V at no selection 1.5V at no signal CS-REC : 1.5V	Recommended clamp capacitor = 0.1µF. For the selected pin, keyed clamp is applied to the input so that the clamp voltage of the output signal becomes constant when the signal is provided. Diode clamp is applied to the input when there is no signal. When no pin is selected and at CS-REC, diode clamp is applied to the input regardless of whether or not the signal is provided.	
7 5 3	C2.IN C3.IN C4.IN	I	10kΩ	2.9V	Recommended capacitor = 0.1µF. DC is overlapped over the signal through external C connection regardless of whether there is a signal or the pin is selected or AMP-GAIN in the mode other than CS-REC.	
11 9 73	Cb.IN G.IN Cr.IN R.IN B.IN	I	Clamp Form	For component 3.2V at 0dB 3.0V at 6dB For RGB 2.2V at 0dB 2.5V at 6dB For RGB through 2.3V 1.2V at no selection 1.2V at no signal to pin 1	Recommended clamp capacitor = 0.1µF. For the selected signal, keyed clamp is applied to the input so that the clamp voltage of output signal becomes constant when there is a signal to pin 1. Diode clamp is applied to the input when there is no signal at pin 1 or when the pin is not selected. For RGB through, feedback clamp is applied from the output to the input.	
23 25 27 29	CV.OUT Cb.OUT G.OUT C.OUT Cr.OUT R.OUT Y.OUT CV.OUT B.OUT	O	4.5Ω	0.8V for CV/ Y 2.5V for component 1.25V for RGB For chroma output 2.2V at 0dB 2.4V at 6dB	The signal that has been selected and keyed clamped (excluding chroma) is amplified and output from the emitter follower. The constant current of emitter follower is 2.5mA when the built-in LPF is selected and 7.5mA when it is not selected.	

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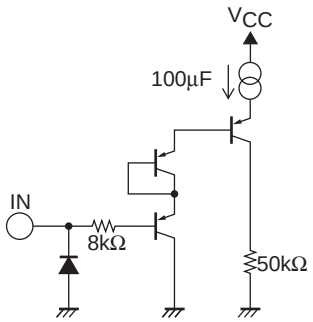
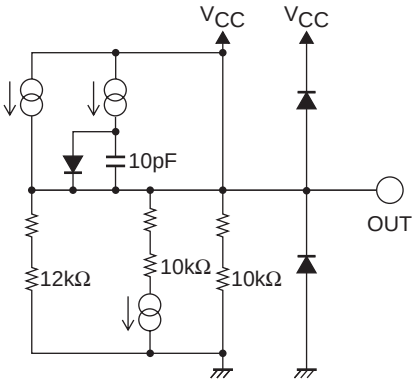
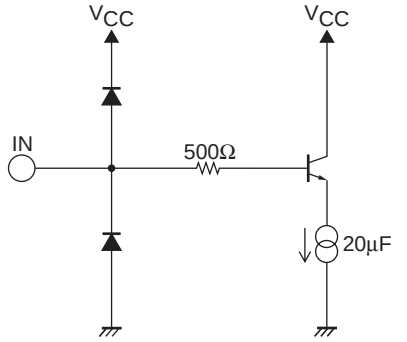
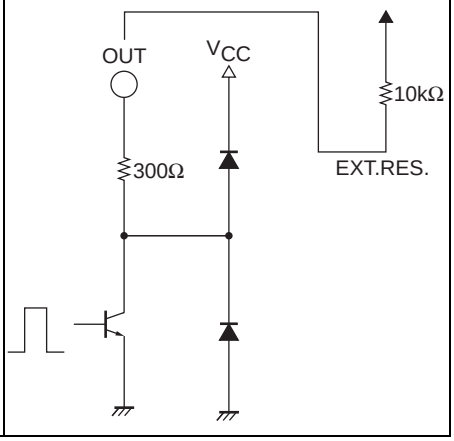
Pin No.	Pin name	I/0	Impedance	DC voltage	Pin Explanation	Input/Output form
18	STAND-BY-SW	I	17GΩ	Hi : 3.3V Lo : 0V	Normal mode when pins 18 and 38 are “L.” RGB through mode when pin 18 is “L” and pin 38 is “H.” RGB standby mode when pins 18 and 38 are “H.” CS-REC mode when pin 18 is “H” and pin 38 is “L.”	
38	EXT-RGB-SW					
20	SW-REG-FILT	O	880Ω	With pin 18 = L, Pin 20 : 2.5V Pin 40 : 2.0V 1With pin 18 = H, Pin 20 : 0V Pin 40 : 0V	Output pin for regulator voltage in IC. S/ N improvement measures recommended by inserting a capacitor of about 470µF between this pin and GND. The amplifier reference voltage on the SW side is based on the regulator voltage of pin 20 and that on the driver side is based on the regulator voltage of pin 40.	
40	DV-REG-FILT					
30	AGCCTL1 (CV)	I	128MΩ	Hi : 5V Lo : 2V Center : 3.3V	Pin to control gain of composite and Y signals when AGC-AMP is used. To suppress crosstalk, it is recommended to insert a noise suppressing capacitor near the pin between the pin and GND.	
35	AGCCTL2 (Y)					
36	C.SYNC OUT	I	480Ω	Hi : 5V Lo : 0.3V	Composite sink output pin Lo (sink) at SYNC Pin 36 can be used for detection of no-signal because LPF is applied. Pin 37 is for detection of the weak electric field. Pin 37 can be changed to V.SYNC-OUT.	
37	C.SYNC OUT2					

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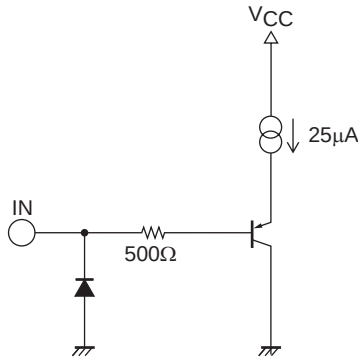
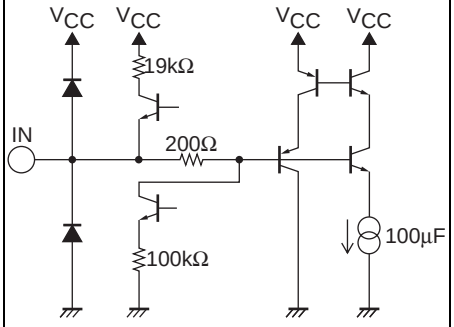
Pin No.	Pin name	I/0	Impedance	DC voltage		Pin Explanation	Input/Output form
72	V_{CC} (B)	P		5V	Description of each pin	V_{CC} on the input SW. To avoid crosstalk, it is recommended to insert a capacitor between each V_{CC} and GND. Keep V_{CC} always ON.	V_{CC} for pin 73 input
74	V_{CC} (Y)						V_{CC} for input of pins 1, 79, 77, and 75
8	V_{CC} (C)						V_{CC} for input of pins 9, 7, 5, and 3
10	V_{CC} (SY)						V_{CC} for input of pins 11, 13, 15, 17, 19, and 21
12	V_{CC} (CV)						V_{CC} for SYNC-SEP, clamp pulse
14	GND (SY)	P		0V	Description of each pin	GND on the input SW side	GND for pin 73 input
22	GND (CV)						GND for input of pins 1, 79, 77, and 75
24	GND (C)						GND for input of pins 9, 7, 5, and 3
26	GND (Y)						GND for pins 11, 13, 15, 17, 19, and 21
28	GND (B)						GND for SYNC-SEP, clamp pulse
76	NC			0V		NC pins on the input SW side. It is recommended to connect this to GND on the substrate to avoid interference between input signals.	
78	NC						
80	NC						
2	NC						
4	NC						
6	NC						
16	NC						
32	SDATA	I	734MΩ	Hi : 5V Lo : V		Pin to enter the serial data and its clock for IIC bus. For the input waveform, refer to the SDA & SCL standard.	
33	SCLK						
39	CV.IN	I	Clamp Form	2.2V at 6dB 2.3V at 9dB 1.85V at no signal		Recommended capacitor = 0.1μF. For the signal with input, feedback clamp is applied to the input so that the clamp voltage becomes constant. For signal without input, diode clamp is applied to the input. Pins 39 and 45 drop to 0 to 1V when not selected.	
43	Y1.IN						
45	Y2.IN R.IN						

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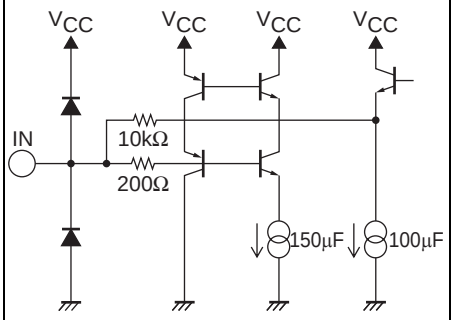
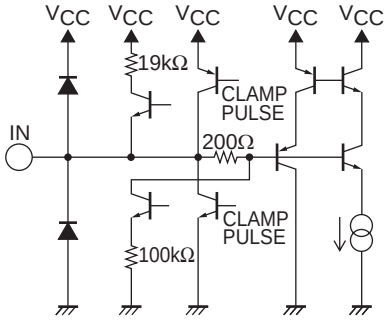
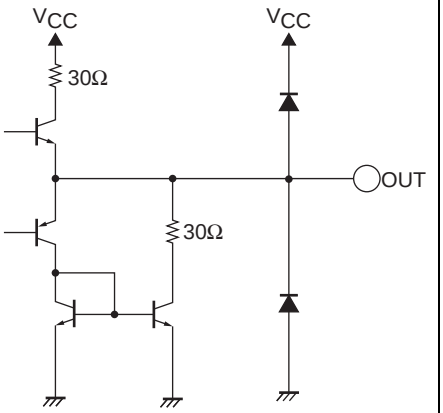
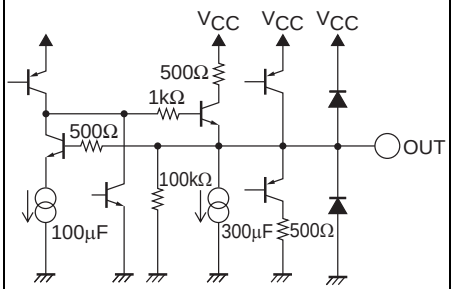
Pin No.	Pin name	I/0	Impedance	DC voltage	Pin Explanation	Input/Output form
41	C.IN	I	10kΩ	2.7V	Recommended capacitor = 0.1µF. DC is overlapped over the signal with external C connected, regardless of the signal or no-signal and AMP-GAIN.	
51	Cr.IN G.IN	I	Clamp Form	For component 2.8V at 6dB 2.7V at 9dB For RGB 2.2V at 6dB 2.3 at 9dB 1.85V at no signal	Recommended capacitor = 0.1µF. In the component mode, keyed clamp is applied to the input so that the pedestal of output signal becomes constant when there is a signal at pin 45. In the RGB mode, feedback clamp is applied to the input so that the output signal clamp voltage becomes constant. Diode clamp is applied to the input when there is no signal.	
53	Cb.IN B.IN					
68	CV.OUT Y1.OUT	O	4Ω	1.3V for CV/ Y/ RGB 2.5V for component For chroma output 2.4V at 0dB 2.6V at 6dB	Recommended coupling capacitor = 470µF (0.1µF for chroma). The signal that has passed AMP & LPF is output from the 75Ω driver. Two drives possible. It is recommended to provide this capacitor as near as possible to the pin to avoid interference.	
65	C.OUT					
63	Y1.OUT					
60	Y2.OUT R.OUT C.OUT					
58	Cr.OUT G.OUT					
56	Cb.OUT B.OUT					
66	C_DC OUT	O	11Ω	Hi : 4.4V Mid : 2.2V Lo : 0V	Circuit to output the DC voltage of S1 and S2 standards. When using this pin, insert a resistor (driving with about 10 kΩ per drive) between the output chroma signal after coupling and this pin, so that the DC voltage of S1 and S2 standard can be overlapped.	
34	V_{CC} (IC)	P		5V	Description of each pin: V_{CC} on the output driver side. It is recommended to insert a capacitor between each V_{CC} and GND to avoid crosstalk. Keep V_{CC} normally ON.	V_{CC} for input of pins 32 and 33
44	V_{CC} (CS1)					V_{CC} for input of pins 39, 41, and 43
50	V_{CC} (CN1)					V_{CC} for input of pins 45, 51, and 53
55	V_{CC} (CN2)					V_{CC} for output of pins 60, 58, and 56
62	V_{CC} (CS2)					V_{CC} for output of pins 68, 65, and 63

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Pin No.	Pin name	I/0	Impedance	DC voltage		Pin Explanation	Input/Output form
31	GND (IC)	P		0V	Description of each pin	GND on the output driver side	GND for input of pins 32 and 33
42	GND (CS1)						GND for input of pins 39, 41, and 43
52	GND (CN1)						GND for input of 45, 51, and 53
57	GND (CN3)						GND for output of pin 56
59	GND (CN4)						GND for output of pin 58
61	GND (CN2)						GND for output of pins 60
64	GND (CS3)						GND for output of pins 63
67	GND (CS2)						GND for output of pin 65
69	GND (CS4)						GND for output of pin 68
46	NC			0V		NC pins on the output driver side. It is recommended to connect this pin to GND on the substrate to avoid interference with the input SW side.	
47	NC						
48	NC						
49	NC						
54	NC						
70	NC						
71	NC						

Device address

	Gr address	bit7 (MSB)	bit6	bit5	bit4	bit3	bit2	bit1	bit0 (LSB)
SW1	00000001	INSEL3	INSEL2	INSEL1	LPF	SWGAIN1	SWGAIN2	YOUT SEL	*Res
SW2	00000010	AGC	V.SYNC	*Res	*Res	CLPOFF1	CLPIUP	TEST2	TEST1
DR1	00000011	SCART	YC MIX	CDC2	CDC1	PROG	GB MUTE	YC MUTE	CP MUTE
DR2	00000100	CV/ S GAIN	CP GAIN	CV/ S DRIVE	CP DRIVE	SCART YC	*Res	*Res	CLPOFF2

* Res means a reserved bit.

Initial state

SW block

INSEL3 INSEL2 INSEL1	SW block input selection/mode changeover	INSEL3	INSEL2	INSEL1	Input selection	Mode
		0	0	0	IN1	Component
		0	0	1	IN1	RGB
		0	1	0	IN2	Composite/ S
		0	1	1	IN3	Composite/ S
		1	0	0	IN4	Composite/ S
		1	0	1	IN5	Composite/ S
		1	1	0	IN6	Composite/ S
		1	1	1	Prohibition	
LPF	SW block LPF	1 : LPF on			0 : LPF off	
SWGAIN1	SW block amplifier gain changeover 1 (for composite/ Y signal)	1 : +6dB (AGC used+3dB)			0 : 0dB	
SWGAIN2	SW block amplifier gain changeover 2 (C/ component/ RGB signal)	1 : +6dB (AGC used+3dB)			0 : 0dB	
YOUT SEL	SW block YOUT output selection	1 : Composite			0 : Y	
AGC	SW block AGC ON/OFF	1 : ON			0 : OFF	
V.SYNC	SYNC output changeover	1 : V-SYNC output			0 : C- SYNC output (for detection of weak field)	
CLPOFF1	Test mode (SW block input clamp OFF)	1 : Clamp OFF			0 : Clamp ON	
CLPIUP	Increase in SW block clamp current	1 : Increase in the clamp current			0 : Clamp current normal	
TEST2	C-SYNC output (TEST mode)	00 : C-SYNC (Normal)			01 : Clamp pulse	
TEST1		10 : Prohibition			11 : Macro vision gate	

Driver block

SCART	Driver block component mode changeover	1 : SCART (RGB)	0 : Y/ Cb/ Cr
YC MIX	Driver block composite output selection	1 : Y/ C MIX	0 : Composite (Y/ C MIX OFF)
CDC2	Driver block C_DC output voltage	00 : Low (0V) 4 : 3mode	01 : Middle (2.2V) letter box
CDC1		10 : High (5V) squeeze	11 : Prohibition
PROG	Driver block LPF changeover	1 : Progressive	0 : Interlace
GB MUTE	Driver block G/B MUTE	1 : MUTE ON	0 : MUTE OFF
YC MUTE	Driver block YC MUTE	1 : MUTE ON	0 : MUTE OFF
CP MUTE	Driver block component MUTE	1 : MUTE ON	0 : MUTE OFF
CV/ S GAIN	Driver block composite/ S amplifier gain	1 : +9dB	0 : +6dB
CP GAIN	Driver block component amplifier gain	1 : +9dB	0 : +6dB
CV/ S DRIVE	Driver block composite/ S output drive capacity	1 : Two-system drive	0 : One-system drive
CP DRIVE	Driver block component output drive capacity	1 : Two-system drive	0 : One-system drive
SCART YC	Driver block SCART YC mode changeover	1 : YC	0 : RGB
CLPOFF2	Test mode (driver block input clamp OFF)	1 : Clamp OFF	0 : Clamp ON

*Initial setting at power ON

	Gr address	data
SW1	00000001	01100010
SW2	00000010	00000000
DR1	00000011	01000000
DR2	00000100	00110000

Control pin function table (1)

*For the serial control pin, enter 3.5 to 5V for H and 0 to 1.5V for L.
*For the parallel control pin, enter 2.6 to 5V for H and 0 to 0.7V for L.
*For all control pins, do not apply the voltage higher than the one applied to V_{CC} or lower than the one applied to GND.
*No control pin must be used in the OPEN state.
*Values in the table are standard values. For SPEC, refer to the electrical characteristics.

[Selection of the SW side input signal]

Control	Gr address 00000001	Gr address 00000010	Pin 18 Standby	Pin 38 RGB through	Input pin to be selected	Signal to be output			
						Pin 23	Pin 25	Pin 27	Pin 29
CV (rear 1)	010***1*	****0*00	L	H/ L	13 (CV) , 7 (C)	(CV)	C	CV	DC
S (rear 1)	010***0*	****0*00	L	H/ L	7 (C) , 79 (Y)	-	C	Y	DC
CV (rear 2)	011***1*	****0*00	L	H/ L	15 (CV) , 5 (C)	(CV)	C	CV	DC
S (rear 2)	011***0*	****0*00	L	H/ L	5 (C) , 77 (Y)	-	C	Y	DC
CV (front)	100***1*	****0*00	L	H/ L	17 (CV) , 3 (C)	(CV)	C	CV	DC
S (front)	100***0*	****0*00	L	H/ L	3 (C) , 75 (Y)	-	C	Y	DC
CV (tuner)	101***1*	****0*00	L	H/ L	19 (CV)	(CV)	DC	CV	DC
	101***0*	****0*00	L	H/ L	None	-	DC	DC	DC
CV (tuner)	110***1*	****0*00	L	H/ L	21 (CV)	(CV)	DC	CV	DC
	110***0*	****0*00	L	H/ L	None	-	DC	DC	DC
component	000*****	****0*00	L	L	1 1(Cb) , 9 (Cr) , 1 (Y)	Cb	Cr	Y	DC
	000*****	****0*00	L	H	1 (Y)	-	-	Y	-
RGB	001*****	****0*00	L	L	11 (G) , 9 (R) , 1 (CV) , 73 (B)	G	R	CV	B
	001*****	****0*00	L	H	1 (CV)	-	-	CV	-
CS-REC	********	********	H	L	Pin 15 input→15 (CV)	-	-	-	-
	********	********	H	L	Pins 15+77 input→77 (Y)	-	-	-	-
	********	********	H	L	Pin 77 input→77 (Y)	-	-	-	-

(Note 1) (CV) : Though a signal is output, its use is not recommended.
(Note 2) DC : The DC voltage differing depending on the AMP-GAIN setting is output.
(Note 3) - : Either the signal is not output or should not be used because the DC voltage is abnormal if output.

[Selection of the input signal for C.SYNC OUT]

Control	Gr address 00000001	Gr address 00000010	Pin 18 Standby	Pin 38 RGB through	Input pin to be selected	Signal to be output	
						C.SYNC	C.SYNC2
CV (rear 1)	010***1*	*0**0*00	L	H/ L	13 (CV)	C.SYNC	C.SYNC2
S (rear 1)	010***0*	*0**0*00	L	H/ L	79 (Y)	C.SYNC	C.SYNC2
CV (rear 2)	011***1*	*0**0*00	L	H/ L	15 (CV)	C.SYNC	C.SYNC2
S (rear 2)	011***0*	*0**0*00	L	H/ L	77 (Y)	C.SYNC	C.SYNC2
CV (front)	100***1*	*0**0*00	L	H/ L	17 (CV)	C.SYNC	C.SYNC2
S (front)	100***0*	*0**0*00	L	H/ L	75 (Y)	C.SYNC	C.SYNC2
CV (tuner)	101***1*	*0**0*00	L	H/ L	19 (CV)	C.SYNC	C.SYNC2
	101***0*	*0**0*00	L	H/ L	None	×	×
CV (tuner)	110***1*	*0**0*00	L	H/ L	21 (CV)	C.SYNC	C.SYNC2
	110***0*	*0**0*00	L	H/ L	None	×	×
component	000*****	*0**0*00	L	H/ L	1 (Y)	C.SYNC	C.SYNC2
RGB	001*****	*0**0*00	L	H/ L	1 (CV)	C.SYNC	C.SYNC2
V.SYNC	********	*1**0*00	L	H/ L	Same as above	C.SYNC	V.SYNC
Monitor	********	*0**0*01	L	H/ L	Same as above	Clamp pulse	C.SYNC2
	********	*0**0*11	L	H/L	Same as above	Macro gate pulse	C.SYNC2
CS-REC	********	********	H	L	Pin 15 input→15 (CV)	C.SYNC	×
	********	********	H	L	Pins 15 + 77 input→77 (Y)	C.SYNC	×
	********	********	H	L	Pin 77 input→77 (Y)	C.SYNC	×
RGB standby	********	********	H	H	1 (CV)	C.SYNC	×

Control pin function table (2)

[SW side AMP-GAIN selection]

Control	Gr address 00000001	Gr address 00000010	Pin 18 Standby	Pin 38 RGB through	AMP-GAIN			
					Pin 23	Pin 25	Pin 27	Pin 29
CV/ S	****00**	0***0*00	L	H/ L	(Fixed at 0dB)	Fixed at 0dB	Fixed at 0dB	DC
	****10**	0***0*00	L	H/ L	(Fixed at 6dB)	Fixed at 0dB	Fixed at 6dB	DC
	****01**	0***0*00	L	H/ L	(Fixed at 0dB)	Fixed at 6dB	Fixed at 0dB	DC
	****11**	0***0*00	L	H/ L	(Fixed at 6dB)	Fixed at 6dB	Fixed at 6dB	DC
	****00**	1***0*00	L	H/ L	(AGC0dB)	Fixed at 0dB	AGC0dB	DC
	****10**	1***0*00	L	H/ L	(AGC3dB)	Fixed at 0dB	AGC3dB	DC
	****01**	1***0*00	L	H/ L	(AGC0dB)	Fixed at 6dB	AGC0dB	DC
	****11**	1***0*00	L	H/ L	(AGC3dB)	Fixed at 6dB	AGC3dB	DC
component	000*00**	0***0*00	L	H/ L	Fixed at 0dB	Fixed at 0dB	Fixed at 0dB	DC
	000*10**	0***0*00	L	H/ L	Fixed at 0dB	Fixed at 0dB	Fixed at 6dB	DC
	000*01**	0***0*00	L	H/ L	Fixed at 6dB	Fixed at 6dB	Fixed at 0dB	DC
	000*11**	0***0*00	L	H/ L	Fixed at 6dB	Fixed at 6dB	Fixed at 6dB	DC
	000*00**	1***0*00	L	H/ L	Fixed at 0dB	Fixed at 0dB	AGC0dB	DC
	000*10**	1***0*00	L	H/ L	Fixed at 0dB	Fixed at 0dB	AGC3dB	DC
	000*01**	1***0*00	L	H/ L	Fixed at 6dB	Fixed at 6dB	AGC0dB	DC
	000*11**	1***0*00	L	H/ L	Fixed at 6dB	Fixed at 6dB	AGC3dB	DC
RGB	001*00**	0***0*00	L	H/ L	Fixed at 0dB	Fixed at 0dB	Fixed at 0dB	Fixed at 0dB
	001*10**	0***0*00	L	H/ L	Fixed at 0dB	Fixed at 0dB	Fixed at 6dB	Fixed at 0dB
	001*01**	0***0*00	L	H/ L	Fixed at 6dB	Fixed at 6dB	Fixed at 0dB	Fixed at 6dB
	001*11**	0***0*00	L	H/ L	Fixed at 6dB	Fixed at 6dB	Fixed at 6dB	Fixed at 6dB
	001*00**	1***0*00	L	H/ L	Fixed at 0dB	Fixed at 0dB	AGC0dB	Fixed at 0dB
	001*10**	1***0*00	L	H/ L	Fixed at 0dB	Fixed at 0dB	AGC3dB	Fixed at 0dB
	001*01**	1***0*00	L	H/ L	Fixed at 6dB	Fixed at 6dB	AGC0dB	Fixed at 6dB
	001*11**	1***0*00	L	H/ L	Fixed at 6dB	Fixed at 6dB	AGC3dB	Fixed at 6dB

(Note 1) Though a signal is output, its use is not recommended.

(Note 2) At the Gr address = 0000 0001 of CV/S, *** ~ does not contain 00* ~ .

[SW side LPF selection]

Control	Gr address 00000001	Gr address 00000010	Pin 18 Standby	Pin 38 RGB through	LPF route of each output	Load corresponding to each output
					Pins 23, 25, 27, 29	Pins 23, 25, 27, 29
LPF-ON	***1****	****0*00	L	H/ L	Pass	1kΩ
LPF-OFF	***0****	****0*00	L	H/ L	Through	330Ω

Control pin function table (3)

[Driver side input signal selection]

Control	Gr address 00000011	Gr address 00000100	Pin 18 Standby	Pin 38 RGB through	Input pin to be selected						Signal to be output					
											Pin 68	Pin 65	Pin 63	Pin 60	Pin 58	Pin 56
CV/ S component	00***000	****0**0	L	L	39 (CV)	41 (C)	43 (Y1)	45 (Y2)	51 (Cr)	53 (Cb)	CV	C	Y1	Y2	Cr	Cb
	00***010	****0**0	L	L	39 (CV)			45 (Y2)	51 (Cr)	53 (Cb)	CV	DC	DC	Y2	Cr	Cb
	00***001	****0**0	L	L	39 (CV)	41 (C)	43 (Y1)				CV	C	Y1	DC	DC	DC
Y/ C-MIX component	01***000	****0**0	L	L		41 (C)	43 (Y1)	45 (Y2)	51 (Cr)	53 (Cb)	CV	C	Y1	Y2	Cr	Cb
	01***010	****0**0	L	L		41 (C)	43 (Y1)	45 (Y2)	51 (Cr)	53 (Cb)	CV	DC	DC	Y2	Cr	Cb
	01***001	****0**0	L	L	39 (CV)	41 (C)	43 (Y1)				CV	C	Y1	DC	DC	DC
CV/ S RGB	10***000	****0**0	L	L	39 (CV)	41 (C)	43 (Y1)	45 (R)	51 (G)	53 (B)	CV	C	Y1	R	G	B
	10***010	****0**0	L	L	39 (CV)			45 (R)	51 (G)	53 (B)	CV	DC	DC	R	G	B
	10***001	****0**0	L	L	39 (CV)	41 (C)	43 (Y1)				CV	C	Y1	DC	DC	DC
YC/ MIX RGB	11***000	****0**0	L	L		41 (C)	43 (Y1)	45 (R)	51 (G)	53 (B)	CV	C	Y1	R	G	B
	11***010	****0**0	L	L		41 (C)	43 (Y1)	45 (R)	51 (G)	53 (B)	CV	DC	DC	R	G	B
	11***001	****0**0	L	L	39 (CV)	41 (C)	43 (Y1)				CV	C	Y1	DC	DC	DC
SCART Y/ C	10***000	****1**0	L	L		41 (C)	43 (Y1)		51 (G)	53 (B)	Y1	C	Y1	C	G	R
	10***010	****1**0	L	L		41 (C)	43 (Y1)		51 (G)	53 (B)	Y1	DC	DC	C	G	R
	10***100	****1**0	L	L		41 (C)	43 (Y1)				Y1	C	Y1	C	DC	DC
SCART Y/ C-MIX	11***000	****1**0	L	L		41 (C)	43 (Y1)		51 (G)	53 (B)	CV	C	Y1	C	G	R
	11***010	****1**0	L	L		41 (C)	43 (Y1)		51 (G)	53 (B)	CV	DC	DC	C	G	R
	11***100	****1**0	L	L		41 (C)	43 (Y1)				CV	C	Y1	C	DC	DC
CV/ S RGB through	*0****0*	****0**0	L	H	39 (CV)	41 (C)	43 (Y1)	9 (R)	11 (G)	73 (B)	CV	C	Y1	R	G	B
	*0****1*	****0**0	L	H	39 (CV)			9 (R)	11 (G)	73 (B)	CV	DC	DC	R	G	B
SCART Y/ C RGB through	*0****0*	****1**0	L	H		41 (C)	43 (Y1)	9 (R)	11 (G)	73 (B)	Y1	C	Y1	R	G	B
	*0****1*	****1**0	L	H			43 (Y1)	9 (R)	11 (G)	73 (B)	Y1	DC	DC	R	G	B
Y/ C-MIX RGB through	*1****0*	*******0	L	H		41 (C)	43 (Y1)	9 (R)	11 (G)	73 (B)	CV	C	Y1	R	G	B
	*1****1*	*******0	L	H		41 (C)	43 (Y1)	9 (R)	11 (G)	73 (B)	CV	DC	DC	R	G	B
RGB standby	********	********	H	H				9 (R)	11 (G)	73 (B)	-	-	-	R	G	B
CS-REC	********	********	H	L							-	-	-	-	-	-

(Note 1) Y1 is a Y signal for S and Y2 is a Y signal for component.

(Note 2) The mute voltage described in the table of electrical characteristics is output.

(Note 3) -: Either the signal is not output or should not be used because the DC voltage is abnormal if output.

Control pin function table (4)

[Driver side AMP-GAIN selection]

Control	Gr address 00000011	Gr address 00000100	Pin 18 Standby	Pin 38 RGB through	AMP-GAIN					
					Pin 68	Pin 65	Pin 63	Pin 60	Pin 58	Pin 56
DAC signal	*****000	00****00	L	L	6dB	6dB	6dB	6dB	6dB	6dB
	*****000	10****00	L	L	9dB	9dB	9dB	6dB	6dB	6dB
	*****000	01****00	L	L	6dB	6dB	6dB	9dB	9dB	9dB
	*****000	11****00	L	L	9dB	9dB	9dB	9dB	9dB	9dB
DAC signal RGB through	*****000	0*****00	L	H	6dB	6dB	6dB	6dB	6dB	6dB
	*****000	1*****00	L	H	9dB	9dB	9dB	6dB	6dB	6dB
RGB standby	********	********	H	H	-	-	-	6dB	6dB	6dB

(Note 1) At SCART-YC, the gain control of chroma output is different between pin 65 and pin 60.
(Note 2) -: Either the signal is not output or should not be used because the DC voltage is abnormal if output.

[Driver side LPF selection]

Control	Gr address 0000001	Gr address 00000100	Pin 18 Standby	Pin 38 RGB through	LPF cut-off frequency (MHz)					
					Pin 68	Pin 65	Pin 63	Pin 60	Pin 58	Pin 56
Interlace	***1****	******00	L	L	9	9	9	9	9	9
Progressive	***0****	******00	L	L	9	9	9	18	18	18
RGB through	********	******00	L	H	9	9	9	Through	Through	Through
RGB standby	********	********	H	H	-	-	-	Through	Through	Through

[Selection of the number of channels that can be driven by 75Ω driver]

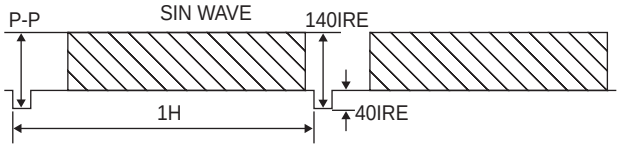
Control	Gr address 0000001	Gr address 00000100	Pin 18 Standby	Pin 38 RGB through	Number of channels that can be driven of each output					
					Pin 68	Pin 65	Pin 63	Pin 60	Pin 58	Pin 56
DAC signal	*****000	**00***0	L	L	1	1	1	1	1	1
	*****000	**10***0	L	L	2	2	2	1	1	1
	*****000	**01***0	L	L	1	1	1	2	2	2
	*****000	**11***0	L	L	2	2	2	2	2	2
DAC signal RGB through	******0*	**00***0	L	H	1	1	1	1	1	1
	******0*	**10***0	L	H	2	2	2	1	1	1
	******0*	**01***0	L	H	1	1	1	2	2	2
	******0*	**11***0	L	H	2	2	2	2	2	2
RGB standby	********	********	H	H	-	-	-	1	1	1

[Selection of S1 and S2 overlapping DC]

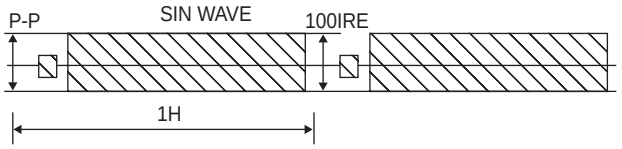
Control	Gr address 0000001	Gr address 00000100	Pin 18 Standby	Pin 38 RGB through	Pin 66	
					Application	Output voltage (V)
For S1 and S2 control	**00****	*******0	L	H/ L	For 4 : 3	0
	01**	*******0	L	H/ L	For letter box	2.2
	10**	*******0	L	H/ L	For squeeze	4.4
	11**	*******0	L	H/ L	Prohibited	-

Test Input Signal

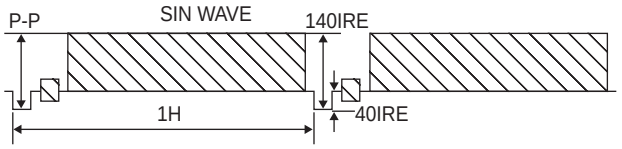
SG.1



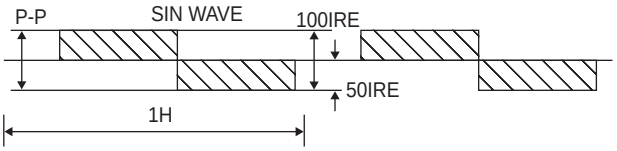
SG.2



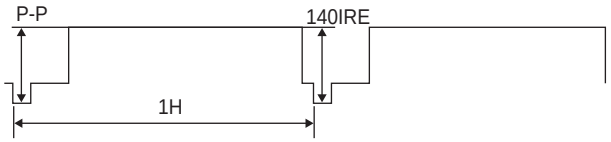
SG.3



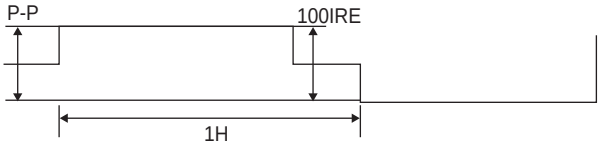
SG.4



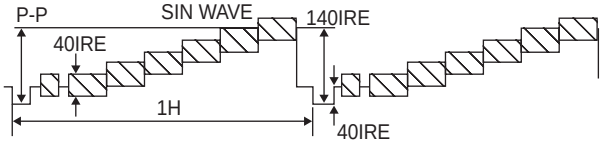
SG.5



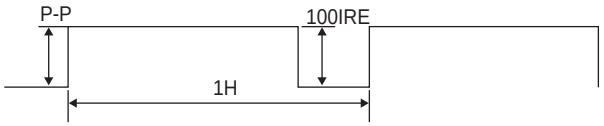
SG.6



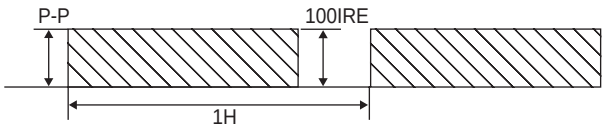
SG.7



SG.8



SG.9



Sample Application