Description

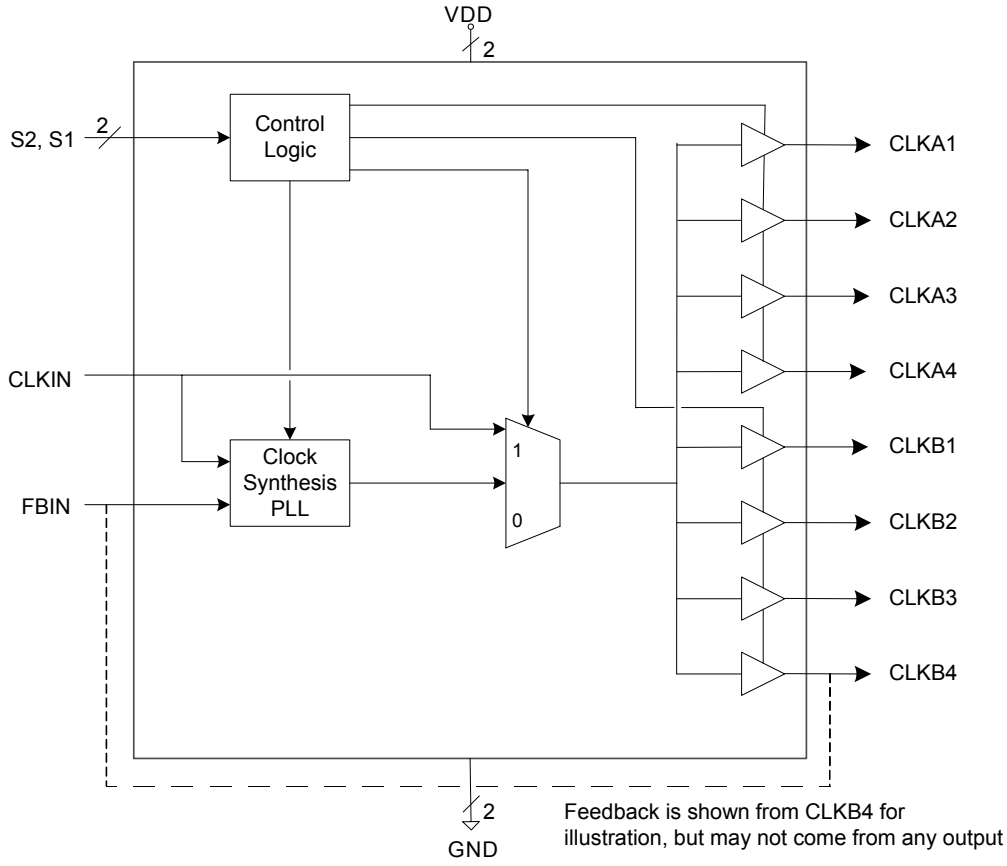
The ICS671-05 is a low phase noise, high-speed PLL based, 8-output, low skew zero delay buffer. Based on ICS' proprietary low jitter Phase-Locked Loop (PLL) techniques, the device provides eight low skew outputs at speeds up to 133 MHz at 3.3 V. The outputs can be generated from the PLL (for zero delay), or directly from the input (for testing), and can be set to tri-state mode or to stop at a low level. For normal operation as a zero delay buffer, any output clock is tied to the FBIN pin.

ICS manufactures the largest variety of clock generators and buffers and is the largest clock supplier in the world.

Features

- Clock outputs from 10 to 133 MHz
- Zero input-output delay
- Eight low skew (<200 ps) outputs
- Device-to-device skew <700 ps
- Low jitter (<200 ps)
- Full CMOS outputs with 25mA output drive capability at TTL levels
- 5V tolerant FBIN and CLKIN pins
- Tri-state mode for board-level testing
- Advanced, low power, sub-micron CMOS process
- Operating voltage of 3.3V
- Industrial temperature range available
- Packaged in 16-pin SOIC and TSSOP packages

Block Diagram



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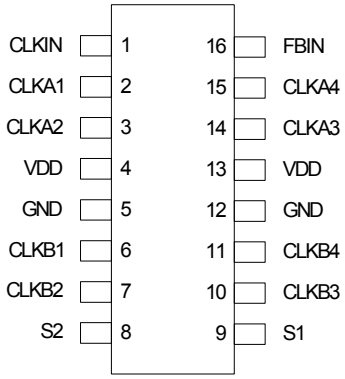
Pin Assignment



16-pin narrow (150 mil) SOIC and
16-pin (173 mil) TSSOP

Output Clock Mode Select Table

S1	S0	CLKA1:A4	CLKB1:B4	A and B Source	PLL Status
0	0	Tri-state (note 1)	Tri-state (note 1)	PLL	OFF
0	1	Running	Tri-state (note 1)	PLL	ON
1	0	Running	Running	CLKIN (note 2)	OFF
1	1	Running	Running	PLL	ON

Note 1. Outputs are in high impedence state
Note 2: Buffer mode only; not zero delay between input and output.

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	Clock input (5 V tolerant).
2-3	CLKA1:A4	Output	Clock outputs A1:A4. See table above.
4	VDD	Power	Power supply. Connect to 3.3 V.
5	GND	Power	Connect to ground.
6-7	CLKB1:B4	Output	Clock outputs B1:B4. See table above.
8	S2	Input	Select input 2. See table above. Internal pull-up.
9	S1	Input	Select input 1. See table above. Internal pull-up.
10-11	CLKB1:B4	Output	Clock outputs B1:B4. See table above.
12	GND	Power	Connect to ground.
13	VDD	Power	Power supply. Connect to 3.3 V.
14-15	CLKA1:A4	Output	Clock outputs A1:A4. See table above.
16	FBIN	Input	Feedback input. Connect to any output under normal operation (5 V tolerant).

External Components

The ICS671-05 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01mF should be connected between VDD and GND on pins 4 and 5, and VDD and GND on pins 13 and 12, as close to the device as possible. A series termination resistor of 33 W may be used to each clock output pin to reduce reflections.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS671-05. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
CLKIN and FBIN inputs	-0.5 V to 5.5 V
Electrostatic Discharge	2000 V
Ambient Operating Temperature	0 to +70°C
Industrial Temperature	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Electrical Characteristics

VDD=3.3 V ±10%, Ambient temperature -40 to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		3.6	V
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Low Current	I_{IL}	VIN = 0V			50	µA
Input High Current	I_{IH}	VIN = VDD			100	µA
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Ouput Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -8 mA	VDD-0.4			V
Operating Supply Current	IDD	No Load, S2 = 1, S1 = 1, Note 1		25		mA
Power Down Supply Current	IDDPD	CLKIN = 0, S2 = 0, S1 = 1		12		µA
		CLKIN = 0, Note 2		12		µA
Short Circuit Current	I_{OS}	Each output		±50		mA
Input Capacitance	C_{IN}	S2, S1, FBIN		5		pF

AC Electrical Characteristics

VDD = 3.3 V ±10%, Ambient Temperature -40 to +85°C, C_{LOAD} at CLK = 15 pF, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency	f_{IN}	See table on page 2	10		133	MHz
Output Clock Frequency		See table on page 2	10		133	MHz
Output Rise Time	t_{OR}	0.8 to 2.0V, CL=30 pF			1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8V, CL=30 pF			1.25	ns
Output Clock Duty Cycle	t_{DC}	measured at VDD/2	45	50	55	%
Device to Device Skew		rising edges at VDD/2, Note 3			700	ps
Output to Output Skew		rising edges at VDD/2, Note 3			200	ps
Input to Output Skew		rising edges at VDD/2, FBIN to CLKA4, S1 = 1, S0 = 1, Note 1			±250	ps
Maximum Absolute JItter		CL = 15 pF, measured at 66.67M		130		ps
Cycle to Cycle Jitter		CL = 30 pF, measured at 66.67M			200	ps
		CL = 15 pF, measured at 66.67M			200	
		CL = 15 pF, measured at 133.33M			100	
PLL Lock Time		Note 3			1.0	ms

Note 1: With CLKIN = 100 MHz, FBIN to CLKA4, all outputs at 100 MHz

Note 2:When there is no clock signal present at CLKIN, the device will enter power-down mode. The PLL is stopped and the outputs are tri-state.

Note 3: Withh VDD at a steady rate and valid clocks at CLKIN and FBIN.

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Thermal Characteristics (16-pin SOIC)

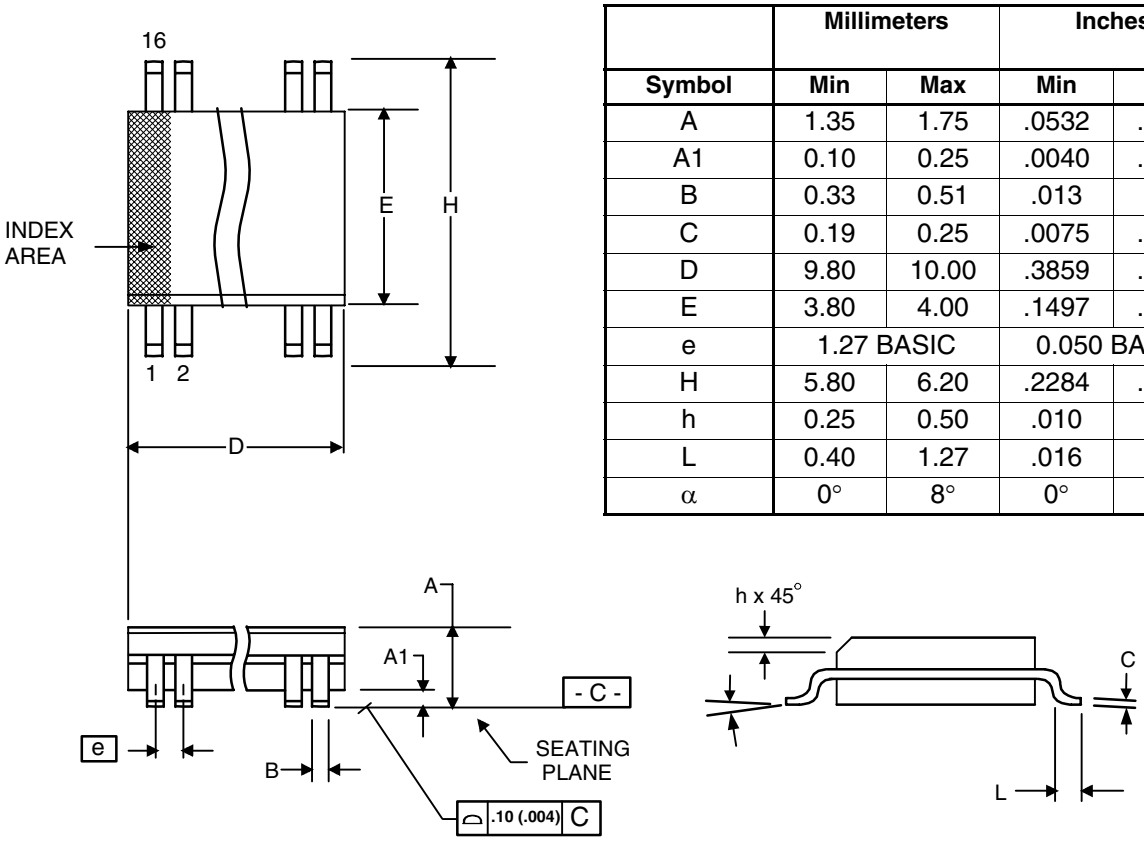
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

Thermal Characteristics (16-pin TSSOP)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

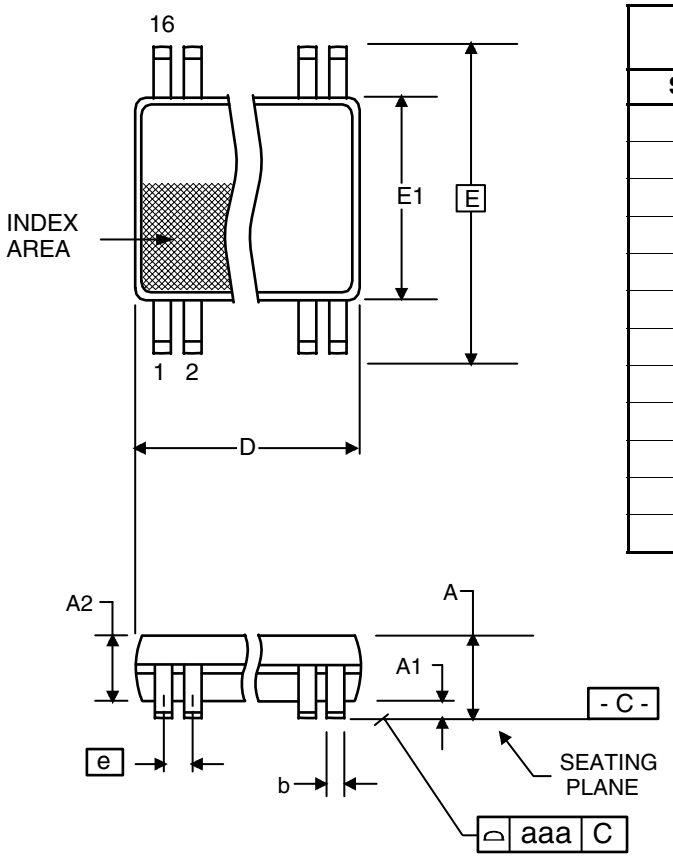
Package dimensions are kept current with JEDEC Publication No. 95

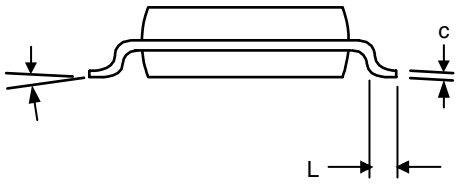


	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	9.80	10.00	.3859	.3937
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153





	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
ICS671M-05I	ICS671M-05I	Tubes	16-pin SOIC	-40 to +85°C
ICS671M-05IT	ICS671M-05I	Tape and Reel	16-pin SOIC	-40 to +85°C
ICS671G-05I	ICS671G-05I	Tubes	16-pin TSSOP	-40 to +85°C
ICS671G-05IT	ICS671G-05I	Tape and Reel	16-pin TSSOP	-40 to +85°C