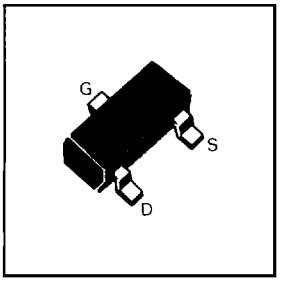
SOT23 P-CHANNEL SILICON JUNCTION FIELD EFFECT TRANSISTORS

FMMJ174 to FMMJ177

PARTMARKING DETAILS:

FMMJ174 – S74
FMMJ175 – S75
FMMJ176 – S76
FMMJ177 – S77



ABSOLUTE MAXIMUM RATINGS at $T_{amb} = 25°C$

Gate Drain or Gate-Source Voltage	30V
Continous Forward Gate Current	50mA
Continuous Device Dissipation at (or below) $T_{amb} = 25°C$	225mW

ELECTRICAL CHARACTERISTICS (25°C)

PARAMETER	SYMBOL	FMMJ174		FMMJ175		FMMJ176		FMMJ177		UNIT	TEST CONDITIONS
		Min.	Typ. Max.	Min.	Typ. Max.	Min.	Typ. Max	Min.	Typ. Max.		
Gate Reverse Current	I_{GSS}		1		1		1		1	nA	$V_{GS} = 20V$, $V_{DS} = 0$
Gate Source Cut-Off Voltage	$V_{GS(off)}$	5	10	3	6	1	4	0.8	2.25	V	$V_{DS} = 15V$, $I_D = 10nA$
Gate Source Breakdown Voltage	B_{VGSS}	30		30		30		30		V	$V_{DS} = 0$, $I_D = -1\mu A$
Saturation Drain Current (Note 2)	I_{DSS}	-20	-135	-7	-70	-2	-35	-1.5	-20	mA	$V_{DS} = -15V$, $V_{GS} = 0$
Drain Cut-Off Current	$I_{D(off)}$		-1		-1		-1		-1	nA	$V_{DS} = -15$, $V_{GS} = 10V$
Drain Source ON Resistance	$r_{DS(on)}$		85		125		250		300	ohms	$V_{DS} = -0.1V$, $V_{GS} = 0$
Drain Gate OFF Capacitance	$C_{dg(off)}$		5.5		5.5		5.5		5.5	pF	$V_{DS} = 0$, $V_{GS} = 10V$ f = 1MHz
Source Gate OFF Capacitance	$C_{sg(off)}$		5.5		5.5		5.5		5.5	pF	
Drain Gate Plus Source Gate ON Capacitance	$C_{dg(on)} + C_{sg(on)}$		32		32		32		32	pF	$V_{DS} = V_{GS} = 0$ f = 1MHz
Turn On Delay Time	$t_{d(on)}$		2		5		15		20	ns	Switching Time Test Conditions
Rise Time	t_r		5		10		20		25	ns	
Turn Off Delay Time	$t_{d(off)}$		5		10		15		20	ns	
Fall Time	t_f		10		20		20		25	ns	

	J174	J175	J176	J177
VDD	-10V	-6V	-6V	-6V
V_{GS}	12V	8V	6V	3V
R_L (off)	560 ohms	1.2K ohms	5.6K ohms	10K ohms
V_{GS}	0V	0V	0V	0V

Notes:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Pulse test duration = 300μs. Duty cycle less than or equal to 3%.