COS/MOS Presettable Up/Down Counter

Binary or BCD-Decade

The RCA-CD4029A consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, CARRY-IN (CLOCK INHIBIT), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals and a CARRY OUT signal are provided as outputs.

A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the CARRY-IN and PRESET ENABLE signals are low. Advancement is inhibited when the CARRY-IN or PRESET ENABLE signals are high. The CARRY-OUT signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY-IN signal is low. The CARRY-IN signal in the high state can thus be considered a CLOCK INHIBIT. The CARRY-IN terminal must be connected to V_{SS} when not in use.

Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts Up when the UP/DOWN INPUT is high, and Down when the UP/DOWN INPUT is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Fig. 13.

Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

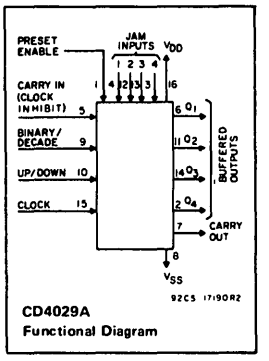
These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix)

Features:

- Medium speed operation . . . 5 MHz (typ.) @ C_L=15 pF and $V_{DD}-V_{SS}$=10 V
- Multi-package parallel clocking for synchronous high speed output response or ripple clocking for slow clock input rise and fall times
- "Preset Enable" and individual "Jam" inputs provided
- Binary or decade up/down counting
- BCD outputs in decade mode
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Programmable binary and decade counting/frequency synthesizers-BCD output
- Analog to digital and digital to analog conversion
- Up/Down binary counting
- Magnitude and sign generation
- Up/Down decade counting
- Difference counting



CD4029A
Functional Diagram

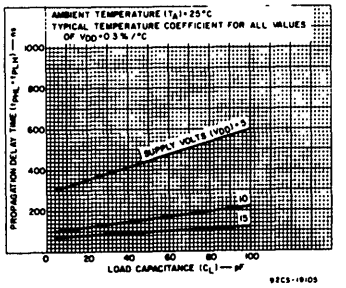


Fig 1– Typical propagation delay time vs. C_L for Q outputs.

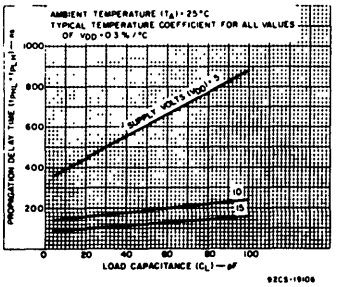


Fig. 2– Typical propagation delay time vs. C_L for carry output.

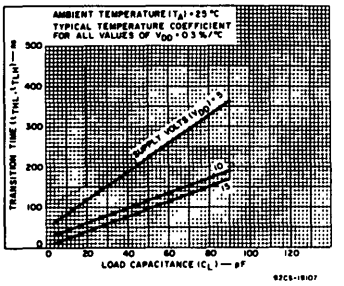


Fig. 3– Typical transition time vs. C_L for Q outputs.

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS D,F,H Packages Min.	LIMITS D,F,H Packages Max.	LIMITS E Package Min.	LIMITS E Package Max.	UNITS
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Setup Time, t_S*	5	650	–	1300	–	ns
	10	230	–	460	–	
Clock Pulse Width, t_W	5	340	–	500	–	ns
	10	170	–	250	–	
Clock Input Frequency, f_{CL}	5	dc	1 5	dc	1	MHz
	10	dc	3	dc	2	
Clock Rise or Fall Time, t_rCL,t_fCL**	5	–	15	–	15	μs
	10	–	15	–	15	
Preset Enable Pulse Width, t_W	5	330	–	660	–	ns
	10	160	–	320	–	

*From Up/Down, Binary/Decade, Carry In, or Preset Enable Control Inputs to Clock Edge

**If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load

MAXIMUM RATINGS, *Absolute-Maximum Values*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A)

PACKAGE TYPES D,F,H . . . . . −55 to +125°C

PACKAGE TYPE E . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) . . . . −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A=−40 to +60°C (PACKAGE TYPE E) . . . 500 mW

FOR T_A=+60 to +85°C (PACKAGE TYPE E) . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A=−55 to +100°C (PACKAGE TYPES D,F) . . . 500 mW

FOR T_A=+100 to +125°C (PACKAGE TYPES D,F) . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING)

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, Input t_r,t_f=20 ns, C_L=15 pF, R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D,F,H Packages Min.	D,F,H Typ.	D,F,H Max.	E Package Min.	E Typ.	E Max.	UNITS
Clocked Operation								
Propagation Delay Time t_{PHL}, t_{PLH} Q Outputs	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Output	5	–	425	850	–	425	1700	
	10	–	150	300	–	150	600	
Transition Time t_{THL}, t_{TLH} Q Outputs	5	–	100	200	–	100	400	ns
	10	–	50	100	–	50	200	
Carry Output	5	–	200	400	–	200	800	
	10	–	100	200	–	100	400	
Minimum Clock Pulse Width, t_W	5	–	200	340	–	200	500	ns
	10	–	100	170	–	100	250	
Clock Rise & Fall Time, t_rCL, t_fCL**	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Minimum Setup Times, t_S*	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Maximum Clock Input Frequency, f_{CL}	5	1.5	2.5	–	1	2.5	–	MHz
	10	3	5	–	2	5	–	
Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF
Preset Enable								
Propagation Delay Time t_{PHL}, t_{PLH} Q Outputs	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Output	5	–	425	850	–	425	1700	
	10	–	150	300	–	150	600	
Minimum Preset Enable Pulse Width, t_W	5	–	115	330	–	115	660	ns
	10	–	80	160	–	80	320	
Minimum Preset Enable Removal Time	5	–	325	650	–	325	1300	ns
	10	–	115	230	–	115	460	
Carry Input								
Propagation Delay Time t_{PHL}, t_{PLH} Carry Output	5	–	175	350	–	175	700	ns
	10	–	50	100	–	50	200	

For footnotes, see Recommended Operating Conditions.

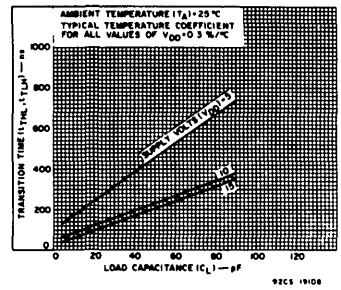


Fig. 4—Typical transition time vs. C_L for carry output.

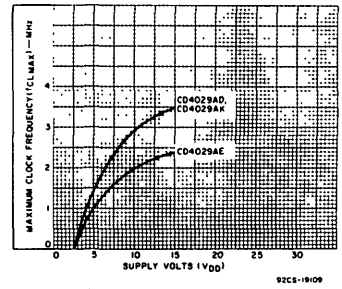


Fig. 5—Maximum clock input frequency vs. V_{DD}.

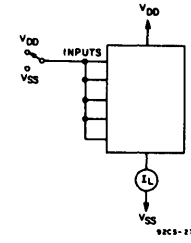


Fig. 6 – Quiescent-device-current test circuit.

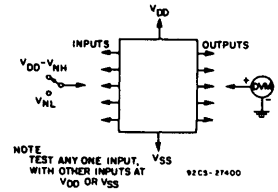


Fig. 7—Noise-immunity test circuit

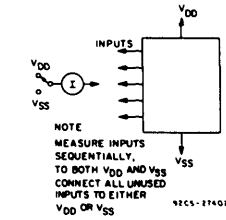


Fig. 8— Input-leakage-current test circuit

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D,F,H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0 5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage Low-Level, V_{OL}	–	5	5	0 Typ , 0 05 Max.								V
	–	10	10	0 Typ., 0 05 Max.								
High-Level, V_{OH}	–	0	5	4.95 Min , 5 Typ								
	–	0	10	9 95 Min , 10 Typ								
Noise Immunity Inputs Low, V_{NL}	4 2	–	5	1.5 Min , 2 25 Typ								V
	9	–	10	3 Min , 4 5 Typ								
Inputs High, V_{NH}	0 8	–	5	1 5 Min , 2 25 Typ								
	1	–	10	3 Min , 4 5 Typ								
Noise Margin Inputs Low, V_{NML}	4 5	–	5	1 Min								V
	9	–	10	1 Min								
Inputs High, V_{NMH}	0.5	–	5	1 Min								
	1	–	10	1 Min.								
Output Drive Current N-Channel (Sink), I_DN Min.												mA
Q Outputs	0 5	–	5	0 5	0 8	0 4	0 28	0 24	0.8	0 2	0.16	
	0 5	–	10	0 74	1 2	0 6	0.42	0 36	1 2	0 3	0 24	
Carry Output	0 5	–	5	0 1	0 16	0 08	0.06	0 05	0 16	0 04	0 03	
	0 5	–	10	0 4	0 64	0 32	0 22	0 19	0 64	0.16	0.13	
P-Channel (Source), I_DP Min												
Q Outputs	4 5	–	5	−0.18	−0.24	−0 12	−0.08	−0.07	−0 24	−0.06	−0.05	
	9 5	–	10	−0.3	−0 4	−0.2	−0.14	−0.14	−0.4	−0.1	−0.08	
Carry Output	4 5	–	5	−0.09	−0.12	−0.06	−0.04	−0.04	−0 12	−0.03	−0.02	
	9.5	–	10	−0 15	−0 2	−0 1	−0.07	−0.07	−0.2	−0.05	−0.04	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											μA
	–	–	15	±10⁻⁵ Typ., ±1 Max								

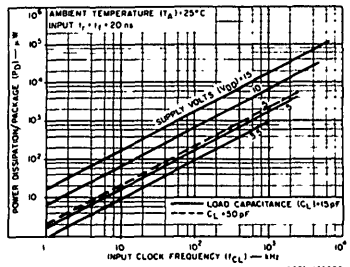


Fig. 9—Typical dissipation characteristics.

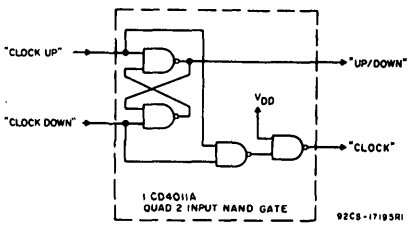
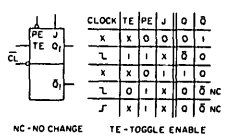


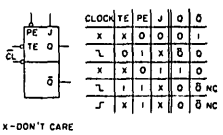
Fig. 10—Conversion of clock up, clock down input signals to clock and up/down input signals.

The CD4029A CLOCK and UP/DOWN inputs are used directly in most applications. In applications where CLOCK UP and CLOCK DOWN inputs are provided, conversion to the CD4029A CLOCK and UP/DOWN inputs can easily be realized by use of the circuit shown below.

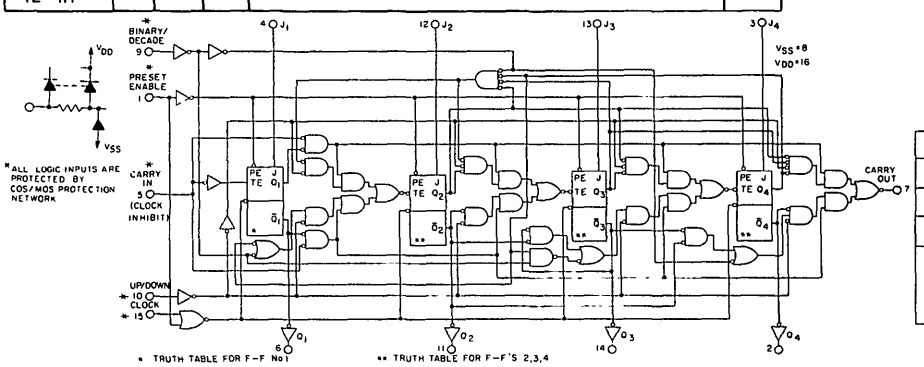
CD4029A changes count on positive transitions of CLOCK UP or CLOCK DOWN inputs. For the gate configuration shown below, when counting up the CLOCK DOWN input must be maintained high and conversely when counting down the CLOCK UP input must be maintained high.



CLOCK	TE	PE	J	Q	δ
X	X	0	0	0	1
↓	1	1	X	δ	0
X	X	0	1	1	0
↓	0	1	X	0	δ NC
↑	X	1	X	0	δ NC



CLOCK	TE	PE	J	Q	δ
X	X	0	0	0	1
↓	0	1	X	δ	0
X	X	0	1	1	0
↓	1	1	X	0	δ NC
↑	X	1	X	0	δ NC



CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	1	BINARY COUNT
	0	DECADE COUNT
UP/DOWN (U/D)	1	UP COUNT
	0	DOWN COUNT
PRESET ENABLE (PE)	1	JAM IN
	0	NO JAM
CARRY IN (CI) (CLOCK INHIBIT)	1	NO COUNTER ADVANCE AT POS CLOCK TRANSITION
	0	ADVANCE COUNTER AT POS CLOCK TRANSITION

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Fig. 11—Logic diagram.