DMOS Transistors

N-Channel Enhancement-Mode DMOS Transistors (≈TO-92 Plastic Package)

Type	Pin Config.	Maximum Drain-Source Voltage	Maximum Continuous Drain Current	Max. Power Dissipation at T_C = 25 °C	Gate Threshold Voltage at $V_{GS} = V_{DS}$, I_D = 1 mA		Drain-Source ON Resistance [1]				Gate-Body Leakage Current at V_{GS} = 15 V, V_{DS} = 0
									at V_{GS}	and I_D	
		Volts	Amps	Watts	typ.	max.	Ohms typ.	max.	Volts	Amps	I_{GSS} max. Nanoamps
BS108	A	200	0.23	0.83	1.5	2.5	5.5	8.0	2.8	0.10	10
BS123	A	60	1.1	0.83	1.0	3.0	0.3	0.4	10	0.60	500
BS170	A	60	0.3	0.83	1.0	3.0	3.5	5.0	10	0.20	10
2N7000	C	60	0.3	0.83	1.0	3.0	3.5	5.0	10	0.50	10

[1]) Pulse Test Width 80 μs; Pulse Duty Factor 1%

N-Channel Enhancement-Mode DMOS Transistors (TO-236 Plastic Package)

Type	Marking Code	Maximum Drain-Source Voltage	Maximum Continuous Drain Current	Max. Power Dissipation at T_C = 25 °C	Gate Threshold Voltage at $V_{GS} = V_{DS}$, I_D = 1 mA		Drain-Source ON Resistance [1]				Gate-Body Leakage Current at V_{GS} = 15 V, V_{DS} = 0
									at V_{GS}	and I_D	
		Volts	Amps	Watts	typ.	max.	Ohms typ.	max.	Volts	Amps	I_{GSS} max. Nanoamps
BS828	S70	200	0.23	0.31	1.5	2.5	5.5	8.0	2.8	0.1	10
BS870	S70	60	0.25	0.31	1.0	3.0	3.5	5.0	10	0.2	10
2N7002	S70	60	0.25	0.31	1.0	2.5	5.0	7.5	10	0.5	10

[1]) Pulse Test Width 80 μs; Pulse Duty Factor 1%
The pin configuration is the following: 1 = Drain, 2 = Gate, 3 = Source

P-Channel Enhancement-Mode DMOS Transistors (≈TO-92 Plastic Package)

Type	Pin Config.	Maximum Drain-Source Voltage	Maximum Continuous Drain Current	Max. Power Dissipation at T_C = 25 °C	Gate Threshold Voltage at $V_{GS} = V_{DS}$, I_D = 1 mA		Drain-Source ON Resistance [1]				Gate-Body Leakage Current at V_{GS} = 15 V, V_{DS} = 0
									at V_{GS}	and I_D	
		Volts	Amps	Watts	typ.	max.	Ohms typ.	max.	Volts	Amps	I_{GSS} max. Nanoamps
BS208	A	–200	–0.2	0.83	–2.8	–4.0	7.0	14	–10	–0.10	–10
BS250	A	–60	–0.25	0.83	–1.0	–3.0	–3.5	5	–10	–0.20	–20

[1]) Pulse Test Width 80 μs; Pulse Duty Factor 1%

P-Channel Enhancement-Mode DMOS Transistor (TO-236 Plastic Package)

Type	Marking Code	Maximum Drain-Source Voltage	Maximum Continuous Drain Current	Max. Power Dissipation at T_C = 25 °C	Gate Threshold Voltage at $V_{GS} = V_{DS}$, I_D = 1 mA		Drain-Source ON Resistance [1]				Gate-Body Leakage Current at V_{GS} = 15 V, V_{DS} = 0
									at V_{GS}	and I_D	
		Volts	Amps	Watts	typ.	max.	Ohms typ.	max.	Volts	Amps	I_{GSS} max. Nanoamps
BS850	S50	–60	–0.25	0.31	–1.0	–3.0	3.5	5	–10	–0.2	–10

[1]) Pulse Test Width 80 μs; Pulse Duty Factor 1%
The pin configuration is the following: 1 = Drain, 2 = Gate, 3 = Source