

# AN3830K

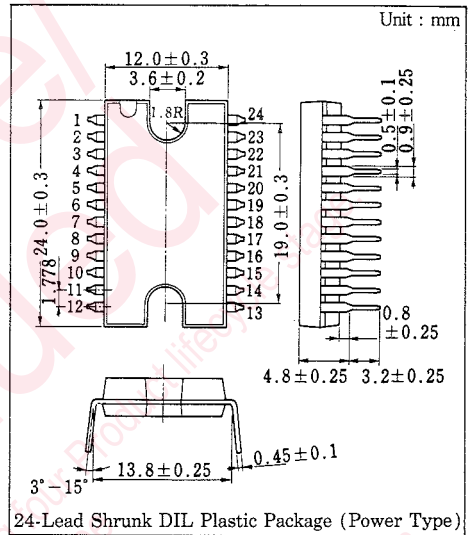
## VTR Reel Direct-Drive Motor Drive Circuit

### Outline

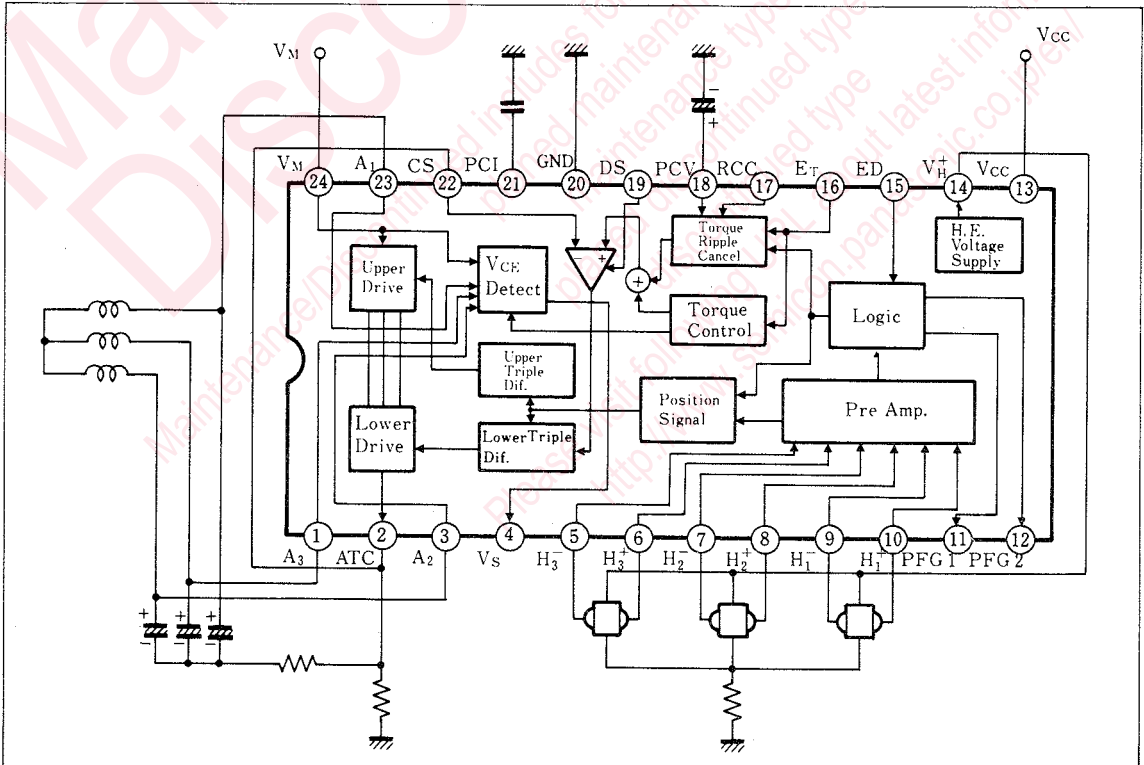
The AN3830K is an integrated circuit designed for a VTR reel direct-drive motor drive.

### Features

- Three-phase full-wave operation
- Built-in torque ripple canceller
- Built-in power transistor
- Forward or reverse motor drive, brake and stop



### Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

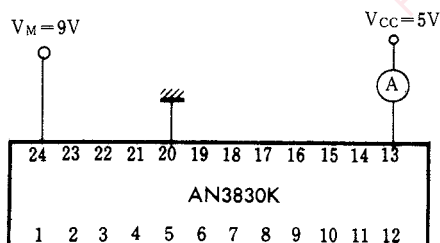
Item	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	6.0	V
Motor Supply Voltage	V <sub>24</sub>	24	V
Motor Drive Voltage	I <sub>1</sub> , I <sub>3</sub> , I <sub>23</sub>	±1.5	A
Output Terminal Voltage	V <sub>1</sub> , V <sub>3</sub> , V <sub>23</sub>	24	V
Power Dissipation	P <sub>D</sub>	2000	mW
Operating Ambient Temperature	T <sub>opr</sub>	-20~+70	°C
Storage Temperature	T <sub>stg</sub>	-55~+150	°C

■ Electrical Characteristics (Ta=25°C)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Supply Current	I <sub>CC</sub>	1	V <sub>CC</sub> =5V, V <sub>M</sub> =9V (Hall Element Current Excluded)	5		15	mA
Torque Command Voltage	E <sub>T</sub>	2	V <sub>CC</sub> =5V	0		1	V
Torque Command Voltage Offset	E <sub>Toffset</sub>	2	V <sub>CC</sub> =5V			5	mV
Output Idle Voltage	ATC <sub>idle</sub>	2	V <sub>CC</sub> =5V			5	mV
Input/Output Gain	G <sub>Io</sub>	2	V <sub>CC</sub> =5V	0.95		1.05	times
Output Limit Voltage	V <sub>limit</sub>	2	V <sub>CC</sub> =5V	0.65		0.84	V
Forward Command Voltage	ED <sub>F</sub>	2	V <sub>CC</sub> =5V			2.3	V
Reverse Command Voltage	ED <sub>R</sub>	2	V <sub>CC</sub> =5V	2.7			V
DS ON Voltage	DS <sub>ON</sub>	2	V <sub>CC</sub> =5V	2.7			V
DS OFF Voltage	DS <sub>OFF</sub>	2	V <sub>CC</sub> =5V			2.3	V
Ripple Cancel ON Voltage	RCC <sub>ON</sub>	2	V <sub>CC</sub> =5V			0.9	V
Ripple Cancel OFF Voltage	RCC <sub>OFF</sub>	2	V <sub>CC</sub> =5V	1.3			V
PFG 1. PFG 2 Output Voltage(H)	PFG(H)	3	V <sub>CC</sub> =5V, I <sub>PFG</sub> =-100μA	2.8			V
PFG 1. PFG 2 Output Voltage(L)	PFG(L)	3	V <sub>CC</sub> =5V, I <sub>PFG</sub> =1mA			0.5	V
Hall Element Supply Voltage	V <sub>H+</sub>	4	V <sub>CC</sub> =5V, I <sub>H</sub> =-200mA	2.6		3.2	V
Hall Element Input Allowable Voltage	V <sub>H(IN)</sub>	5	V <sub>CC</sub> =5V	1.2		2.35	V
Hall Element Offset Referred to Input	V <sub>H(offset)</sub>	2	V <sub>CC</sub> =5V	-5		5	mV
Output Stage Loss Voltage	V <sub>loss</sub>	2	V <sub>CC</sub> =5V, E <sub>T</sub> =0.56V, I <sub>O</sub> =1A			2.6	V
Lower Saturation Voltage	V <sub>N(sat)</sub>	2	V <sub>CC</sub> =5V, E <sub>T</sub> =0.56V, I <sub>O</sub> =1A			1.4	V
Upper Saturation Detection Output Gain	G <sub>VS</sub>	6	V <sub>CC</sub> =5V	2.2		2.9	times
Upper Saturation Detection Output	V <sub>SO</sub>	6	V <sub>CC</sub> =5V, E <sub>T</sub> =0.35V, V <sub>M-Al</sub> =1.55V	2		3	V

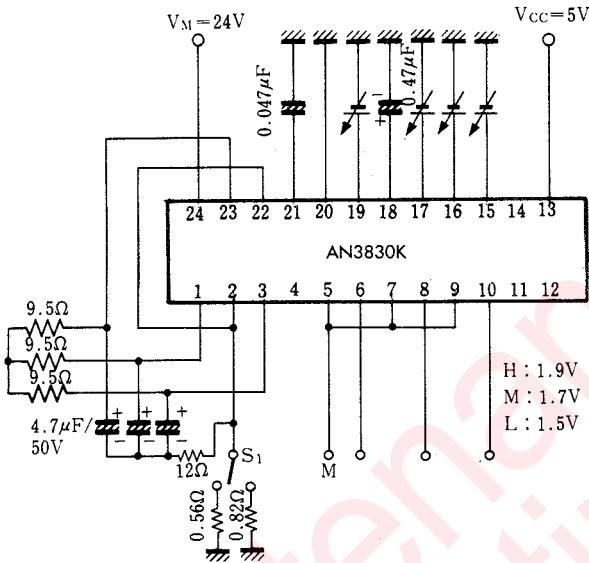
Note) Operating Supply Voltage : V<sub>CC(opp)</sub>=4.5 to 5.5V

Test Circuit 1 (I<sub>CC</sub>)



I<sub>CC</sub>: Measure the current flowing in from the V<sub>CC</sub> terminal.

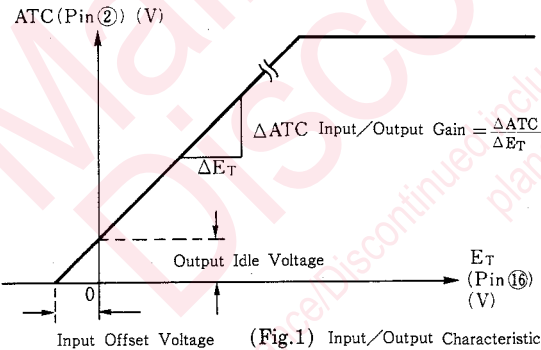
**Test Circuit 2** ( $E_T$ ,  $E_{T\text{offset}}$ ,  $ATC_{\text{idler}}$ ,  $G_{\text{io}}$ ,  $V_{\text{limit}}$ ,  $ED_F$ ,  $ED_R$ ,  $DS_{\text{ON}}$ ,  $DS_{\text{OFF}}$ ,  $RCC_{\text{ON}}$ ,  $RCC_{\text{OFF}}$ ,  $V_{H(\text{offset})}$ ,  $V_{\text{loss}}$ ,  $V_{H(\text{sat})}$ )



•  $E_{T\text{offset}}$ ,  $ATC_{\text{idler}}$  and  $G_{\text{io}}$ :

Measure the input/output characteristic under the following conditions

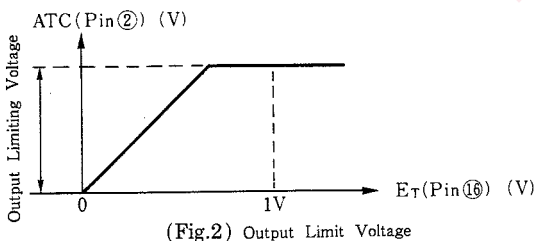
$S_1$	$H_1^+$	$H_2^+$	$H_3^+$	ED	RCC	DS
$0.56\Omega$	H	L	L	5V	0V	0V



•  $E_T$  and  $V_{\text{limit}}$

Measure the ATC voltage under the following conditions.

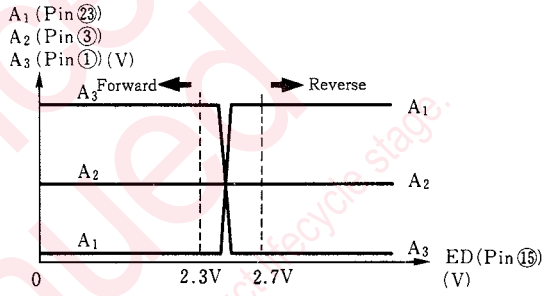
$S_1$	$H_1^+$	$H_2^+$	$H_2^+$	ED	$E_T$	RCC	DS
$0.82\Omega$	H	L	L	0V	1V	0V	0V



•  $ED_F$  and  $ED_R$

Measure the ED threshold under the following conditions.

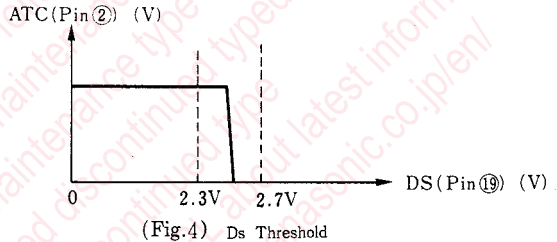
$S_1$	$H_1^+$	$H_2^+$	$H_3^+$	$E_T$	RCC	DS
$0.56\Omega$	H	L	L	0.56V	0V	0V



•  $DS_{\text{on}}$  and  $DS_{\text{off}}$ :

Measure the DS Threshold under the following conditions.

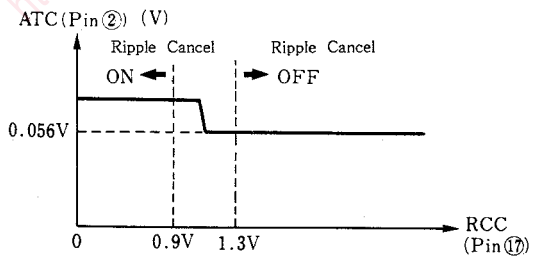
$s_1$	$H_1^+$	$H_2^+$	$H_3^+$	$E_T$	ED	Rcc
$0.56\Omega$	H	L	L	0.56V	5V	0V



•  $RCC_{\text{ON}}$  and  $RCC_{\text{OFF}}$ :

Measure the RCC threshold under the following conditions.

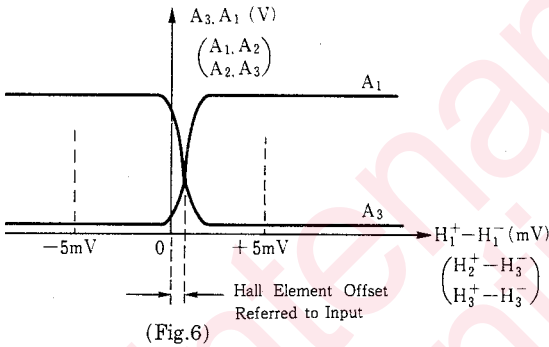
$S_1$	$H_1^+$	$H_2^+$	$H_3^+$	$E_T$	ED	DS
$0.56\Omega$	H	M	L	0.056V	5V	0V



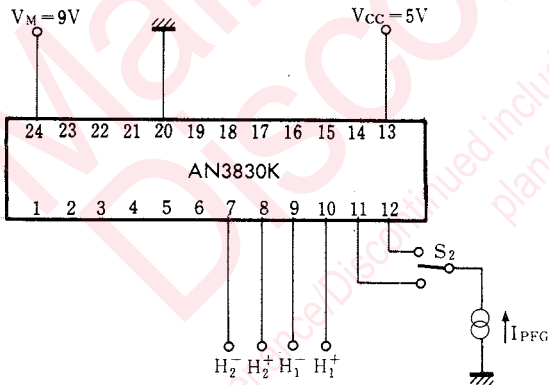
•  $V_{HIN}$ :

Measure the Hall element offset referred to input under the following conditions.

S <sub>1</sub>	H <sub>1</sub> <sup>+</sup>	H <sub>2</sub> <sup>+</sup>	H <sub>3</sub> <sup>+</sup>	E <sub>T</sub>	ED	DS	RCC	Measuring Points
0.56 Ω	H → L	H	L	0.056V	5V	0V	0V	A <sub>3</sub> , A <sub>1</sub>
	L	L → H	H					A <sub>1</sub> , A <sub>2</sub>
	H	L	L → H					A <sub>2</sub> , A <sub>3</sub>



Test Circuit 3 (PFG<sub>H</sub>, PFG<sub>L</sub>)



• PFG<sub>H</sub> and PFG<sub>L</sub>:

Measure the High levels and the Low Levels of PFG1 and PFG2 under the following conditions.

H <sub>1</sub> <sup>+</sup>	H <sub>1</sub> <sup>-</sup>	H <sub>2</sub> <sup>+</sup>	H <sub>2</sub> <sup>-</sup>	S <sub>2</sub>	I <sub>PFG</sub>	Measuring Points
H	M	L	M	P F	-100 μA	PFG1
L	M	L	M	PFG1	1mA	P F
L	M	H	M	PFG2	-100 μA	PFG2
L	M	L	M	PFG2	1mA	PFG2

Where H=1.9V. M=1.7V and L=1.5V.

•  $V_{loss}$ :

(1)Set the following conditions.

S <sub>1</sub>	H <sub>1</sub>	H <sub>2</sub>	H <sub>3</sub>	E <sub>T</sub>	ED	DS	RCC
0.56 Ω	H	L	L	0.56V	0V	0V	0V

(2)Regulate the  $V_M$  value is regulated so that

$$V_{N(sat)} + V_{P(sat)} = 2.6V.$$

$$V_N(sat) = V_{A1} - V_{ATC}$$

$$V_P(sat) = V_M - V_{A3}$$

$$V_{loss} = V_N(sat) + V_P(sat)$$

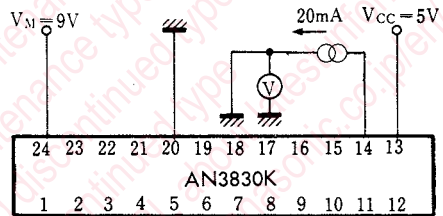
(3)Measure the voltage between the middle point and A<sub>2</sub> and confirm that the A<sub>2</sub> output transistor is not ON.

•  $V_{N(sat)}$ : Measure the collector to emitter voltage of the lower output transistor under the following

conditions.

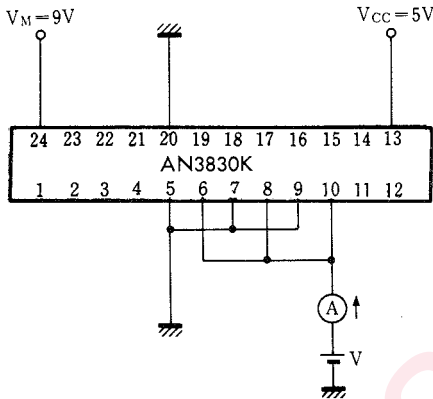
S <sub>1</sub>	H <sub>1</sub> <sup>+</sup>	H <sub>2</sub> <sup>+</sup>	H <sub>3</sub> <sup>+</sup>	E <sub>T</sub>	ED	DS	RCC	Measuring Point
0.56 Ω	H	L	L	0.56V	0V	0V	0V	A <sub>1</sub> -ATC
	L	H	L					A <sub>2</sub> -ATC
	L	L	H					A <sub>3</sub> -ATC

Test Circuit 4 ( $V_{H^+}$ )

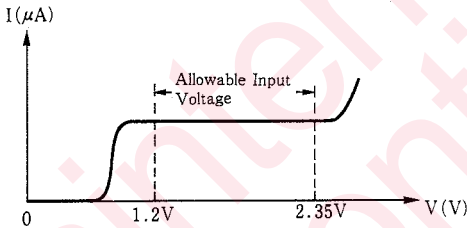


$V_{H^+}$ : Measure the Pin⑭ electric potential when Pin⑫ is connected at 20mA.

Test Circuit 5 ( $V_{H(IN)}$ )

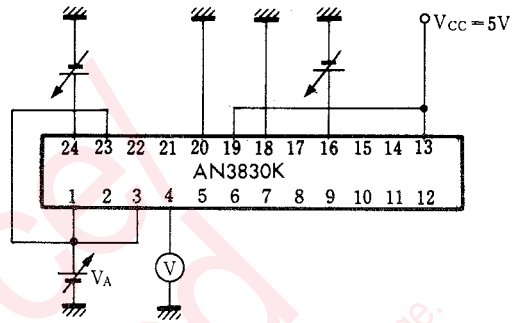


- $V_{H(IN)}$ : Measure the Hall element allowable input voltage in the above circuit.



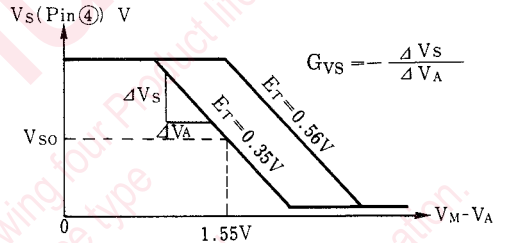
(Fig. 7) Hall Element Input Allowable Voltage

Test Circuit 6 ( $G_{VS}, V_{SO}$ )



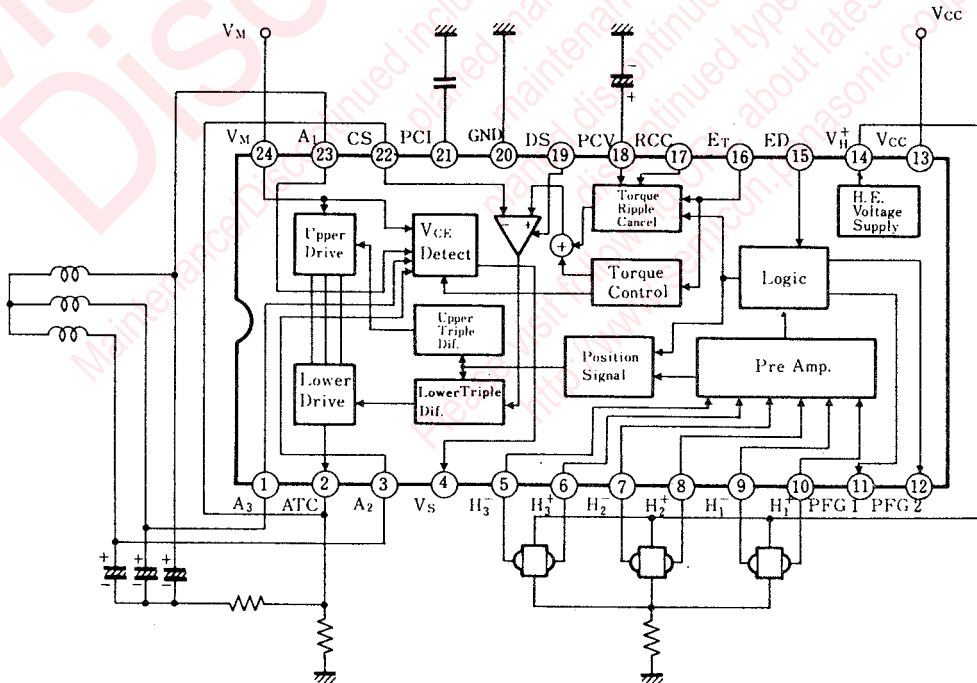
- $G_{VS}$  and  $V_{SO}$ :

Measure the  $V_s$  value when  $V_M = 9V$ , Gain  $G_{vs} = \Delta V_s / \Delta V_A$ ,  $E_T = 0.35V$ , and  $V_M - V_A = 1.55 V$ .



(Fig. 8) Upper Saturation Detection Output Characteristic

Application Circuit



## ■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	(A3) Drive Output 3	13	(V <sub>cc</sub> ) Power Source
2	(ATC) Current Output	14	(V <sub>H</sub> <sup>+</sup> ) H.E. Power Supply
3	(A2) Drive Output 2	15	(ED) Direction Control
4	(V <sub>s</sub> ) V <sub>cc</sub> Detect	16	(E <sub>T</sub> ) Control
5	(H <sub>3</sub> <sup>-</sup> ) H.E. Input	17	(RCC) Torque Ripple Cancel Control
6	(H <sub>3</sub> <sup>+</sup> ) H.E. Input	18	(PCV) Voltage Loop Phase Compensation
7	(H <sub>2</sub> <sup>-</sup> ) H.E. Input	19	(DS) Disable
8	(H <sub>2</sub> <sup>+</sup> ) H.E. Input	20	(GND) GND
9	(H <sub>1</sub> <sup>-</sup> ) H.E. Input	21	(PCI) Current Loop Phase Compensation
10	(H <sub>1</sub> <sup>+</sup> ) H.E. Input	22	(CS) Current Detection
11	(PFG1) PFG Output 1	23	(AI) Drive Output 1
12	(PFG1) PFG Output 1	24	(V <sub>M</sub> ) Motor Power

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