32K x 36 Fast CMOS Synchronous Static RAM with Interleaved Burst Counter and Output Register

Features

- Interfaces directly with the x86 and Pentium™ microprocessors (100, 80, 66, 60, 50 MHz)
- High-speed access times
  - Clock to data valid times: 4.5, 5, 6, 7, 8 ns
  - Cycle times: 8, 10, 13, 15 ns
- High-density 64K x 18 architecture
- Output register for pipelined designs
- Choice of 5V or 3V (±10%) output Vcc for output level compatibility
- High-output drive: 30 pF at rated T_A
- Asynchronous output enable
- Self-timed write cycle
- Individual byte write controls
- Internal interleaved burst read / write address counter
- Internal registers for address, data, controls
- Packages: 100-pin TQFP - TQ

Description

The PDM44056 is a 1,179,648 bit synchronous random access memory organized as 32,768 x 36 bits. It has burst mode capability and interface controls designed to provide high-performance in second level cache designs for x86 and Pentium microprocessors. Addresses, write data and all control signals except output enable are controlled through positive edge-triggered registers. Write cycles are self-timed and are also initiated by the rising edge of the clock. Controls are provided to allow burst reads and writes of up to four words in length. A 2-bit burst address counter controls the two least significant bits of the address during burst reads and writes. The burst address counter uses the 2-bit counting scheme required by the x86 and Pentium microprocessors. Individual write strobes provide byte write for the four 9-bit bytes of data. An asynchronous output enable simplifies interface to high-speed buses. Separate output Vcc pins provide user-controlled 5V or 3.3V TTL-compatible output levels.

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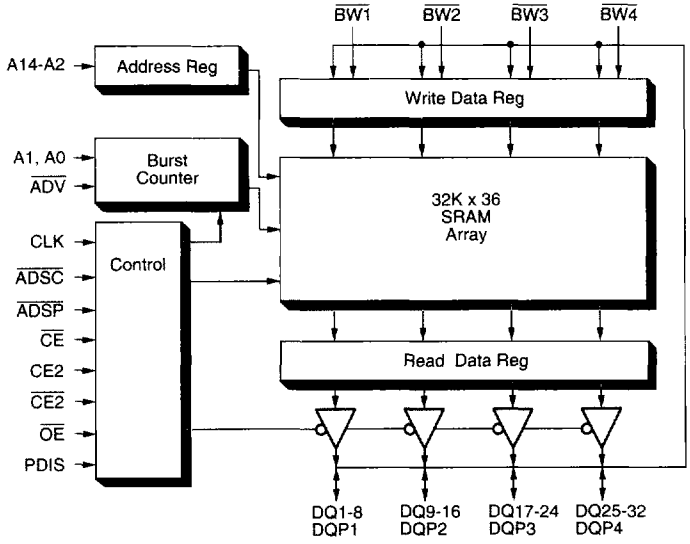
Functional Block Diagram



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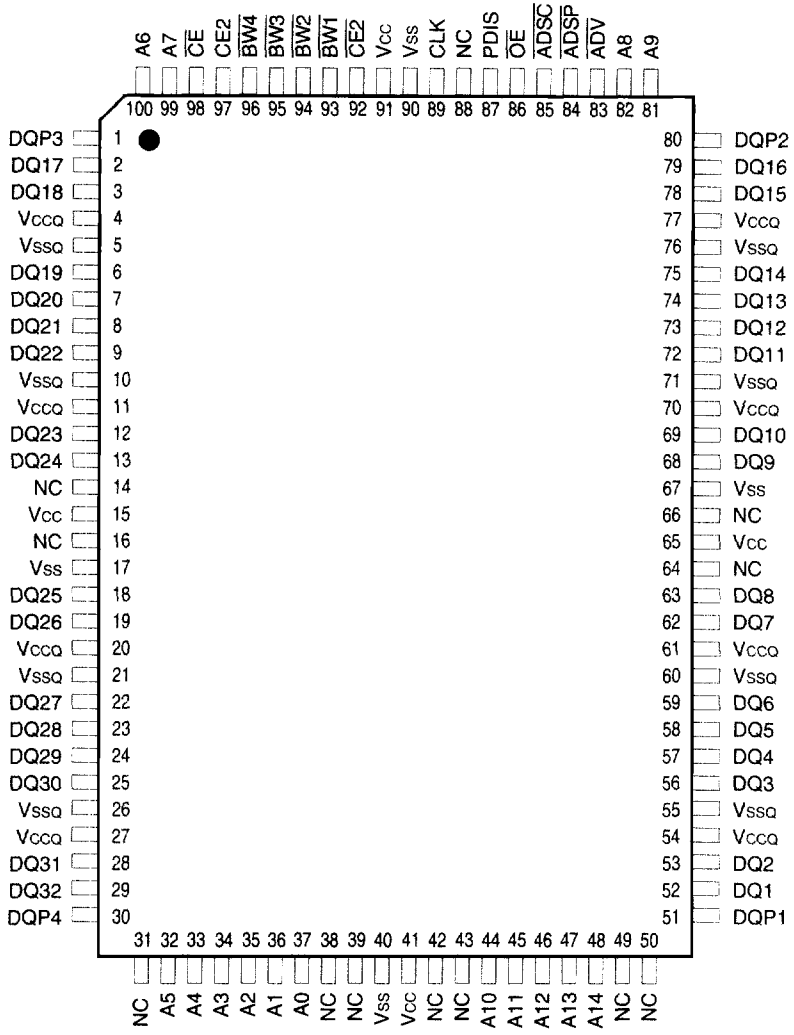
Pin Assignment



Pinout

Name	I/O	Description	Name	I/O	Description
A14-A2	I	Address Inputs A14-A2	$\overline{CE}$, CE2, $\overline{CE2}$	I	Chip Enables
A1, A0	I	Address Inputs A1 & A0	$\overline{BW1}$-$\overline{BW4}$	I	Byte Write Enables
DQ1-DQ32	I/O	Read/Write Data	$\overline{OE}$	I	Output Enable
DQP1-DQP4	I/O	Read/Write Data	CLK	I	Clock
PDIS	I	Parity Disable (disables DQP1-4)	V_{CC}	—	Array Power (+5V)
$\overline{ADV}$	I	Burst Counter Advance	V_{CCQ}	—	Output Power for DQ's (+3.3V or +5V)
$\overline{ADSC}$	I	Controller Address Status	V_{SS}	—	Array Ground
$\overline{ADSP}$	I	Processor Address Status	V_{SSQ}	—	Output Ground for DQ's

Asynchronous Truth Table

Operation	$\overline{OE}$	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z: Write Data In
Deselected	X	High-Z

NOTE: 1. L = Low, H = High, X = Don't Care.
2. For a write operation following a read operation, $\overline{OE}$ must be high before the input data required setup time and held high through the input data hold time.

Burst Sequence Table

Sequence	A14-A2	A1	A0
Start Address	XXXX	A1	A0
1st Burst Address	XXXX	A1	$\overline{A0}$
2nd Burst Address	XXXX	$\overline{A1}$	A0
3rd Burst Address	XXXX	$\overline{A1}$	$\overline{A0}$

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Synchronous Truth Table (See Notes 1 through 4)

$\overline{CE}$, CE2, $\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{BW1}$-$\overline{BW4}$	CLK	Address	Operation
HXX, XLX or XXH	X	L	X	X	↑	N/A	Deselected
LHL	L	X	X	X	↑	External	Read Cycle, Begin Burst
LHL	H	L	X	L	↑	External	Write Cycle, Begin Burst
LHL	H	L	X	H	↑	External	Read Cycle, Begin Burst
X	H	H	L	L	↑	Next	Write Cycle, Continue Burst
X	H	H	L	H	↑	Next	Read Cycle, Continue Burst
X	H	H	H	L	↑	Current	Write Cycle, Suspend Burst
X	H	H	H	H	↑	Current	Read Cycle, Suspend Burst
HXX	X	H	L	L	↑	Next	Write Cycle, Continue Burst
HXX	X	H	L	H	↑	Next	Read Cycle, Continue Burst
HXX	X	H	H	L	↑	Current	Write Cycle, Suspend Burst
HXX	X	H	H	H	↑	Current	Read Cycle, Suspend Burst

NOTE: 1. L = Low, H = High, X = Don't Care, ↑ = Low-to-High transition.
2. All inputs except $\overline{OE}$ must meet setup and hold times relative low-to-high transition of clock, CLK.
3. Wait states are inserted by suspending burst.
4. $\overline{ADSP}$ is gated by $\overline{CE}$. Both $\overline{ADSP}$ and $\overline{CE}$ must be valid for $\overline{ADSP}$ to load the address register and force a read.

Burst Mode Operation

This is a synchronous part. All activities are initiated by the positive, low-to-high edge of the clock (CLK). This part can perform burst reads and writes with burst lengths of up to four words. The four word burst is created by using a burst counter to drive the two least-significant bits of the internal RAM address. The burst counter is loaded at the start of the burst and is incremented for each word of the burst. The burst counter uses a modified binary sequence compatible with the cache line burst reload sequence of x86 microprocessors. This sequence is given in the Burst Sequence Table.

Burst transfers are initiated by the $\overline{ADSC}$ or $\overline{ADSP}$ signals. When the $\overline{ADSP}$ and $\overline{CE}$ signals are sampled low, a read cycle is started (independent of $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$ and $\overline{ADSC}$), and prior burst activity is terminated. $\overline{ADSP}$ is gated by $\overline{CE}$, so both must be active for $\overline{ADSP}$ to load the address register and to initiate a read cycle. The address and the chip enable input ($\overline{CE}$) are sampled by the same edge that samples $\overline{ADSP}$. Read data is valid at the output after the specified delay from the clock edge.

When $\overline{ADSC}$ is sampled low and $\overline{ADSP}$ is sampled high, a read or write cycle is started depending on the state of $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$. If $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ and $\overline{BW4}$ are all sampled high, a read cycle is started, as described above. If $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, or $\overline{BW4}$ is sampled low, a write cycle is begun. The address, write data, and the chip enable inputs ($\overline{CE}$, CE2 and $\overline{CE2}$) are sampled by the same edge that samples $\overline{ADSC}$ and $\overline{BW1}$-$\overline{BW4}$. The $\overline{ADV}$ line is held high for this clock edge to maintain the correct address for the internal write operation which will follow this second clock edge.

After the first cycle of the write burst, the state of $\overline{BW1}$-$\overline{BW4}$ determines whether the next cycle is a read or write cycle, and $\overline{ADV}$ controls the advance of the address counter. The $\overline{ADV}$ signal advances the address counter. This increments the address to the next available RAM address. You write the next word in the burst by taking $\overline{ADV}$ low and presenting the write data at the positive edge of the clock. If $\overline{ADV}$ is sampled low, the burst counter advances and the write data (which is sampled by the same clock) is written into the internal RAM during the time following the clock edge.

This part has an output register. Output read data is available one cycle after the address register and burst counter are loaded or the burst counter is incremented.

Absolute Maximum Ratings (1)

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to V_{SS}	–0.5 to +7.0	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA
T_j	Maximum Junction Temperature (2)	125	125	°C

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Appropriate thermal calculations should be performed in all cases and specifically for those where the chosen package has a large thermal resistance (e.g., TSOP). The calculation should be of the form: $T_j = T_a + P * \theta_{ja}$ where T_a is the ambient temperature, P is average operating power and θ_{ja} the thermal resistance of the package. For this product, use the following θ_{ja} value:

   TQFP: 50° C/W

Recommended DC Operating Conditions

Symbol	Description		Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
V_{CCQ}		5V	4.5	5.0	5.5	V
		3.3V	3.0	3.3	3.6	V
V_{SS}	Supply Voltage		0	0	0	V
Industrial	Ambient Temperature		–40	25	85	°C
Commercial	Ambient Temperature		0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V ± 5%, All Temperature Ranges)

Symbol	Description	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = MAX., V_{IN} = V_{SS} to V_{CC}	—	1	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = MAX., V_{OUT} = V_{SS} to V_{CC}	—	1	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8 mA	0	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4 mA	2.4	V_{CCQ}	V
V_{IH}	Input HIGH Voltage		2.2	6	V
V_{IL}	Input LOW Voltage (1)		–0.5	0.8	V

NOTE: 1. Undershoots to –1.5 for 10 ns are allowed once per cycle.

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Power Supply Characteristics

Symbol	Description	Test Conditions	-4.5	-5 ns	-6 ns	-7 ns	-8 ns	Unit
I_{CC1}	Active Supply Current: Outputs Open	V_{CC} = Max., Inputs @ 0.0V or 3.0V f = $1/t_{CYC}$ on Rclk & Wclk	390	380	370	360	360	mA
I_{SB}	Standby Current: Outputs Open	V_{CC} = Max., Inputs @ 0.0V or 3.0V f = $1/t_{CYC}$, $\overline{CE}$ = V_{IH}	135	130	125	120	120	mA

SHADED AREA = PRELIMINARY DATA

NOTE:All values are maximum guaranteed values.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTES: 1. This parameter is determined by device characterization, but is not production tested.

AC Test Conditions

Input pulse levels	V_{SS} to 3.0V
Input rise and fall times	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

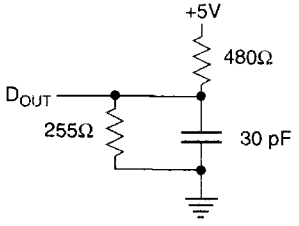


Figure 1. Output Load Equivalent

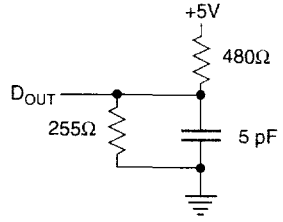


Figure 2. Output Load Equivalent (for t_{LZCE}, t_{HZCE}, t_{LZWE}, t_{HZWE}, t_{LZOE}, t_{HZOE})

AC Electrical Characteristics

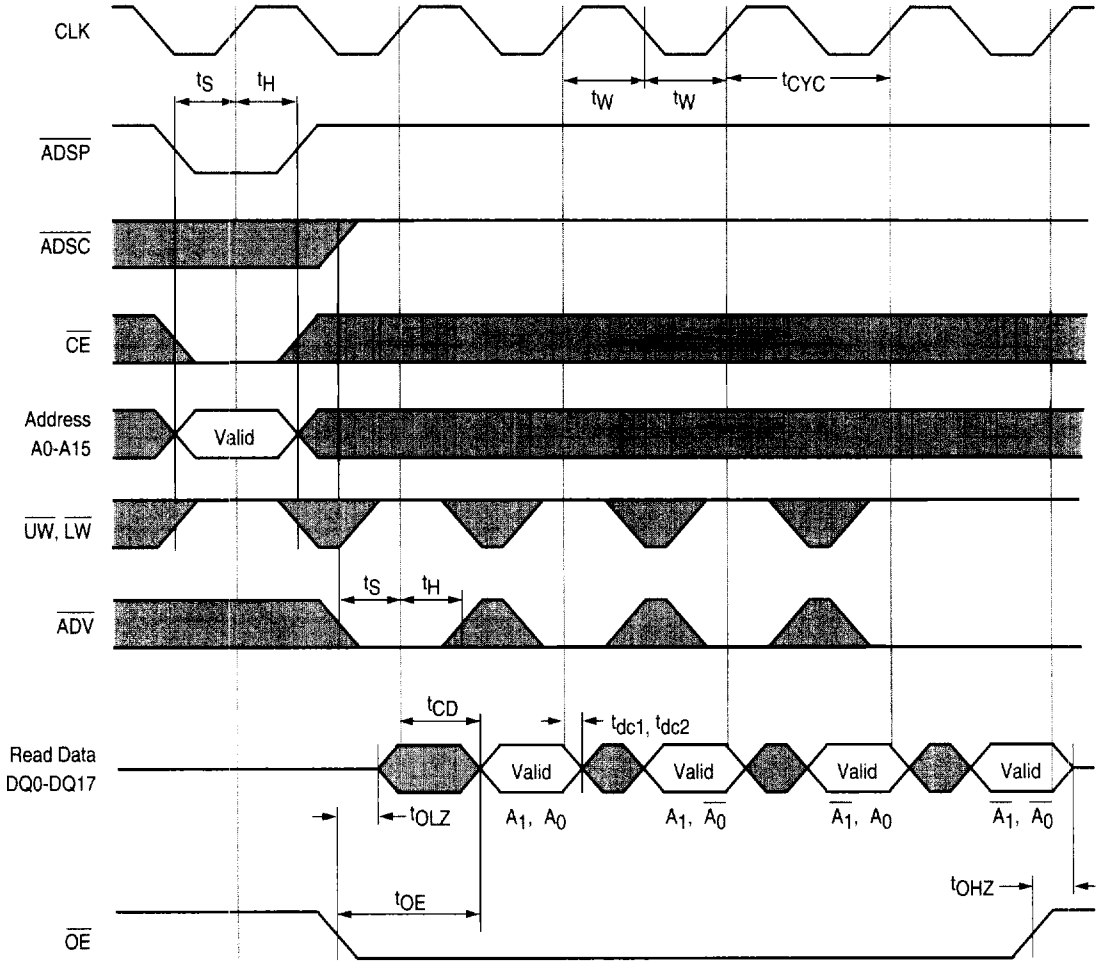
Parameter	Symbol	-4.5	-5	-6	-7	-8	Type	Units
Clock cycle time	t_{CYC}	8	10	13	15	15	Min.	ns
Clock to data valid (std. load)(5)	t_{CD}	4.5	5	6	7	8	Max.	ns
Clock to data valid (0 pF load)	t_{CD0}	4	4	5	6	7	Min.	ns
Output enable	t_{OE}	4.5	5	5	5	5	Max.	ns
Clock to data low-Z	t_{dc1}	2	3	3	3	3	Min.	ns
Clock to data hold time	t_{dc2}	2	3	3	3	3	Min.	ns
Output enable to output low-Z(1)	t_{OLZ}	0	0	0	0	0	Min.	ns
Output enable to output high-Z(1,6)	t_{OHZ}	2	2	2	2	2	Min.	ns
		3	4	5	5	5	Max.	ns
Clock to data high-Z(1,6)	t_{CHZ}	4	5	6	6	6	Max.	ns
Clock high/low	t_W	3	4	4.5	5	5	Min.	ns
Setup time(7)	t_S	2.5	2.5	2.5	2.5	2.5	Min.	ns
Hold time(7)	t_H	0.5	0.5	0.5	0.5	0.5	Min.	ns

SHADED AREA = PRELIMINARY DATA

NOTES:

1. Values characterized and guaranteed by design, not currently tested.
2. A read cycle is defined by $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ and $\overline{BW4}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{BW1}$, $\overline{BW2}$,$\overline{BW3}$ or $\overline{BW4}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from CLK or $\overline{OE}$.
4. $\overline{OE}$ is a "don't care" when $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$ is sampled low.
5. Maximum access times are guaranteed for all possible x86 external bus cycles.
6. Transition is measured ±500 mV from steady-state voltage with load of Figure 1b. This parameter is sampled rather than
   100% tested. At any given voltage and temperature, t_{CHZ} max is less than t_{dc1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ALL rising edges of CLK whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.
8. This device has an output data register. Read data is available one clock cycle after the address register and burst counter have been loaded or the burst counter has been incremented.

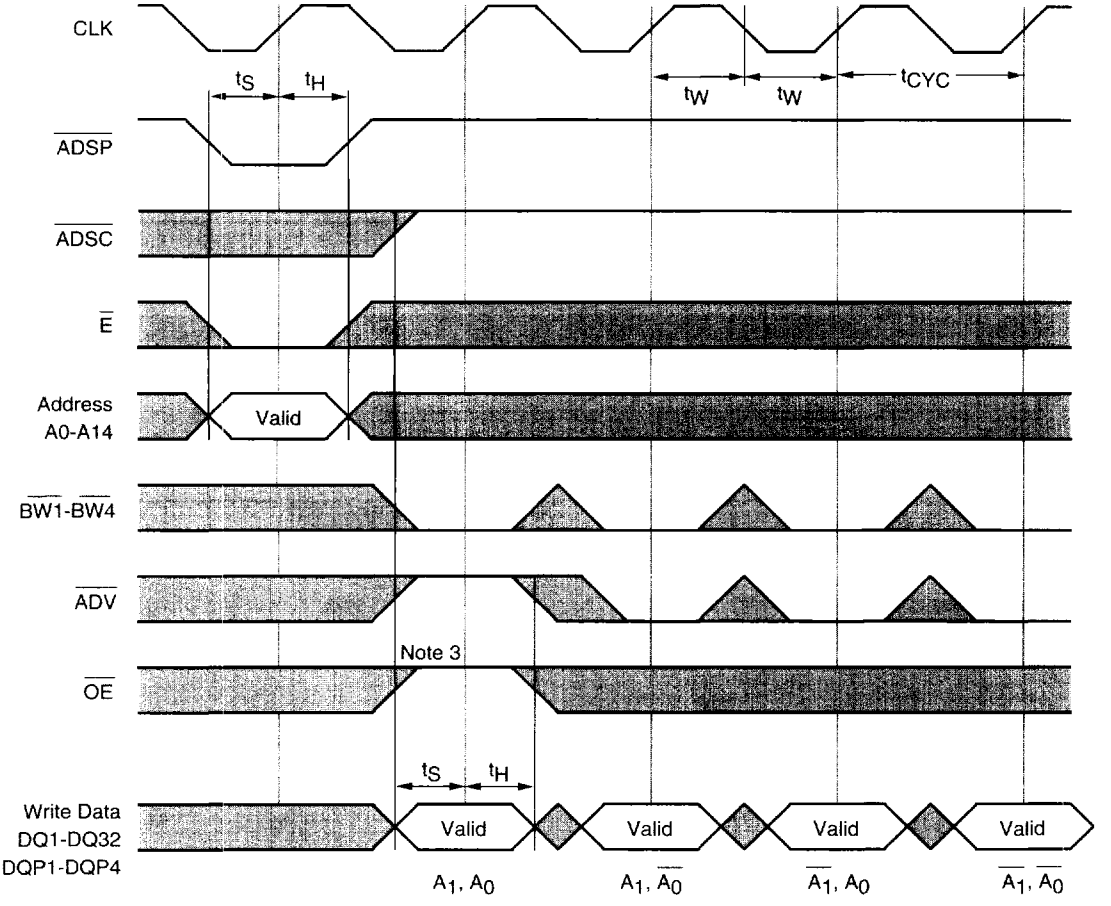
$\overline{ADSP}$ Read Timing Diagram



NOTE:

1. $\overline{E}$ is low when $\overline{CE}$ = low, CE2 = high and $\overline{CE2}$ = low. $\overline{E}$ is high otherwise.

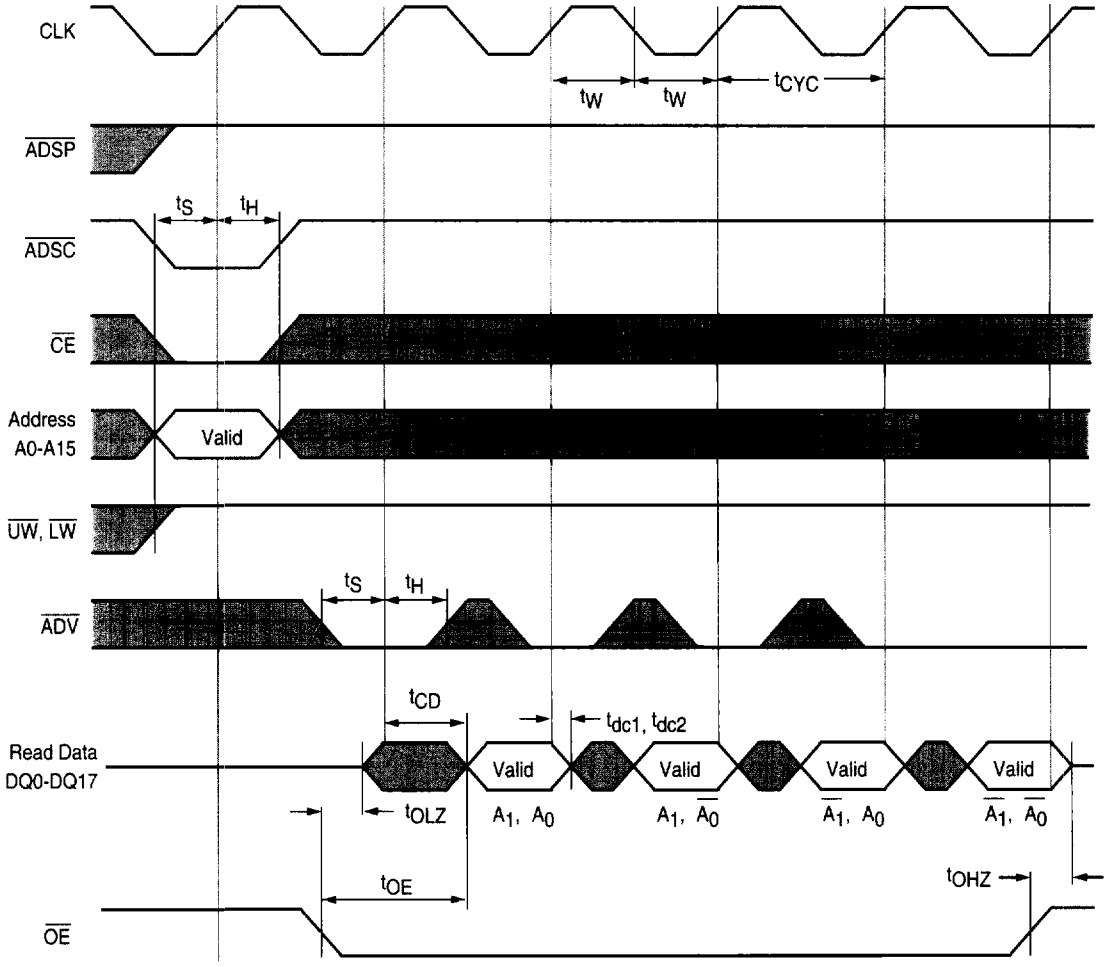
$\overline{ADSP}$ Write Timing Diagram



NOTES:

1. $\overline{E}$ is low when $\overline{CE}$ = low, CE2 = high and $\overline{CE2}$ = low. $\overline{E}$ is high otherwise.
2. $\overline{BW1}$–$\overline{BW4}$ are ignored for the first cycle when $\overline{ADSP}$ initiates the burst. $\overline{ADSP}$ active loads a new address into the address counter and forces the first cycle to be a read cycle.
3. $\overline{OE}$ is high before data in setup.

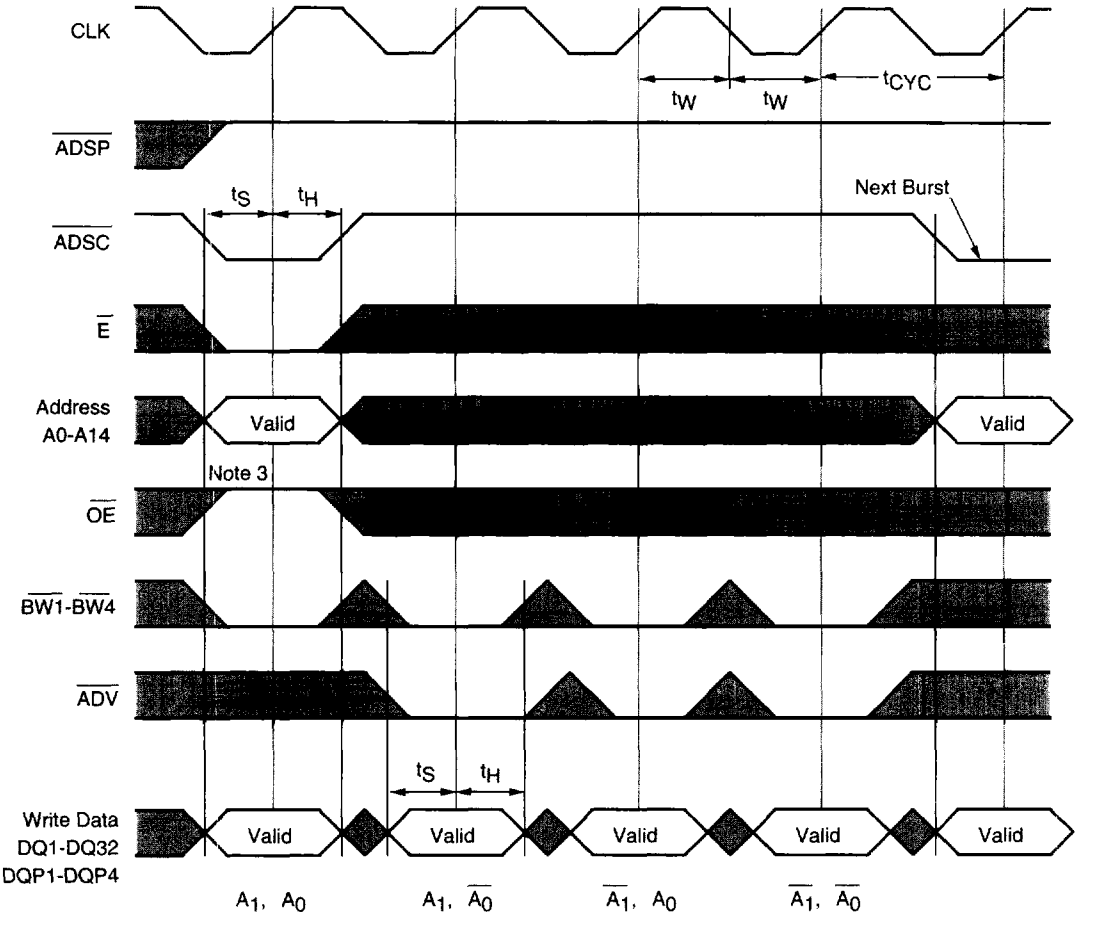
$\overline{ADSC}$ Read Timing Diagram



NOTE:

1. $\overline{E}$ is low when $\overline{CE}$ = low, CE2 = high and $\overline{CE2}$ = low. $\overline{E}$ is high otherwise.

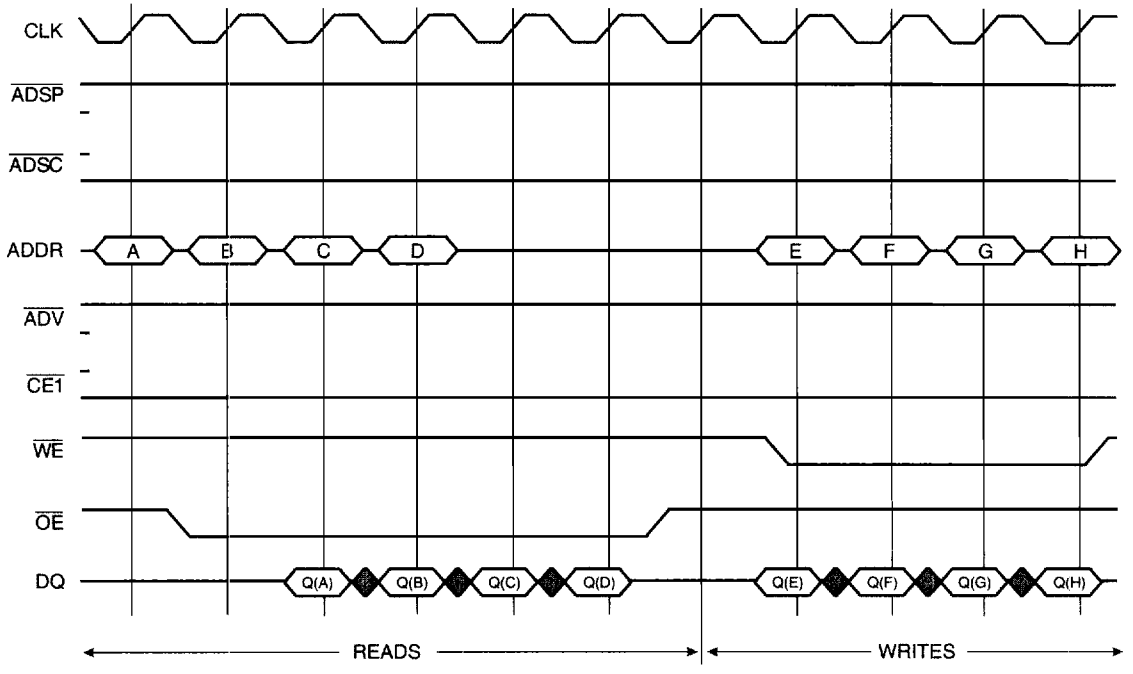
$\overline{ADSC}$ Write Timing Diagram



NOTES:

1. $\overline{E}$ is low when $\overline{CE}$ = low, CE2 = high and $\overline{CE2}$ = low. $\overline{E}$ is high otherwise.
2. $\overline{BW1}$–$\overline{BW4}$ are ignored for the first cycle when $\overline{ADSP}$ initiates the burst. $\overline{ADSP}$ active loads a new address into the address counter and forces the first cycle to be a read cycle.
3. $\overline{OE}$ is high before data in setup.

Sequential Non-burst Read and Write Timing Diagram



NOTES:

1. $\overline{ADSP}$ = high, $\overline{ADSC}$ = low, $\overline{ADV}$ = high, $\overline{CE1}$ = low.
2. H ≥ V_{IH}, L ≤ V_{IL}.

Ordering Information