ML610Q482/ML610482

8-bit Microcontroller

GENERAL DESCRIPTION

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I^2C bus interface (master), buzzer driver, battery level detect circuit, and RC oscillation type A/D converter, are incorporated around 8-bit CPU nX-U8/100.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by 3-stage pipe line architecture parallel procesing. The Flash ROM that is installed as program memory achieves low-voltage low-power consumption operation (read operation) equivalent to mask ROM and is most suitable for battery-driven applications.
The on-chip debug function that is installed enables program debugging and programming.
The ML610Q482P/ ML610482P supporting industrial temperature -40°C to +85°C, are also available.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function (ML610Q482)
  - Minimum instruction execution time
    30.5 μs (@32.768 kHz system clock)
    0.244μs (@4.096 MHz system clock)

- Internal memory
  - ML610Q482
    Internal 64KByte Flash ROM (32K×16 bits) (including unusable 1KByte TEST area)
    Internal 4KByte Data RAM (4096×8 bits)
  - ML610482
    Internal 64KByte Mask ROM (32K×16 bits) (including unusable 1KByte TEST area)
    Internal 4KByte Data RAM (4096×8 bits)

- Interrupt controller
  - 2 non-maskable interrupt sources (Internal source: 1, External source: 1)
  - 18 maskable interrupt sources (Internal sources: 14, External sources: 4)

- Time base counter
  - Low-speed time base counter ×1 channel
    Frequency compensation (Compensation range: Approx. −488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter ×1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s @32.768 kHz)

- Timers
  - 8 bits × 4 channels (Timer0-3: 16-bit x 2 configuration available by using Timer0-1 or Timer2-3)
  - Clock frequency measurement mode (in one channel of 16-bit configuration using Timer2-3)

- PWM
  - Resolution 16 bits × 1 channel

- Synchronous serial port
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- I^2C bus interface
  - Master function only
  - Fast mode (400 kbps@4MHz), standard mode (100 kbps@1MHz, 50kbps@500kHz)

- Buzzer driver
  - 4 output modes, 8 frequencies, 16 duty levels

- RC oscillation type A/D converter
  - 24-bit counter
  - Time division × 2 channels

- Analog Comparator
  - Operating voltage: V_{DD}=1.8V～3.6V
  - Common mode input voltage: 0.2V～VDD－1.0V
  - Input offset voltage: 50mV(max)
  - Interrupt allow edge selection and sampling selection

- General-purpose ports
  - Non-maskable interrupt input port × 1 channel
  - Input-only port × 6 channels (including secondary functions)
  - Output-only port × 4 channels (including secondary functions)
  - Input/output port × 22 channels (including secondary functions)

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected
  - Reset by the watchdog timer (WDT) overflow

- Power supply voltage detect function
  - Judgment voltages: One of 16 levels
  - Judgment accuracy: ±2% (Typ.)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation without low-speed clock)
    Crystal oscillation (32.768 kHz/38.4KHz)
  - High-speed clock:
    Built-in RC oscillation (500 kHz)
    Built-in PLL oscillation (8.192 MHz ±2.5%), crystal/ceramic oscillation (4.096 MHz), external clock
  - Selection of high-speed clock mode by software:
    Built-in RC oscillation, built-in PLL oscillation, crystal/ceramic oscillation, external clock

- Power management
  – HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  – STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  – Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  – Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Guaranteed operating range
  – Operating temperature: –20°C to +70°C (P version: –40°C to +85°C)
  – Operating voltage: V_{DD} = 1.1V to 3.6V

- Product name – Supported Function

- Chip (Die) -	ROM type	Operating temperature	Product availability
ML610Q482-xxxWA	Flash ROM	-20°C to +70°C	Yes
ML610Q482P-xxxWA	Flash ROM	-40°C to +85°C	Yes
ML610482-xxxWA	Mask ROM	-20°C to +70°C	Yes
ML610482P-xxxWA	Mask ROM	-40°C to +85°C	Yes

-48-pin plastic TQFP -	ROM type	Operating temperature	Product availability
ML610Q482-xxxTB	Flash ROM	-20°C to +70°C	Yes
ML610Q482P-xxxTB	Flash ROM	-40°C to +85°C	Yes
ML610482-xxxTB	Mask ROM	-20°C to +70°C	-
ML610482P-xxxTB	Mask ROM	-40°C to +85°C	-

xxx: ROM code number
Q:Flash ROM version
P: Wide range temperature version
WA: Chip
TB: TQFP

BLOCK DIAGRAM

ML610Q482 Block Diagram

Figure 1 show the block diagram of the ML610Q482.
"*" indicates the secondary function of each port.

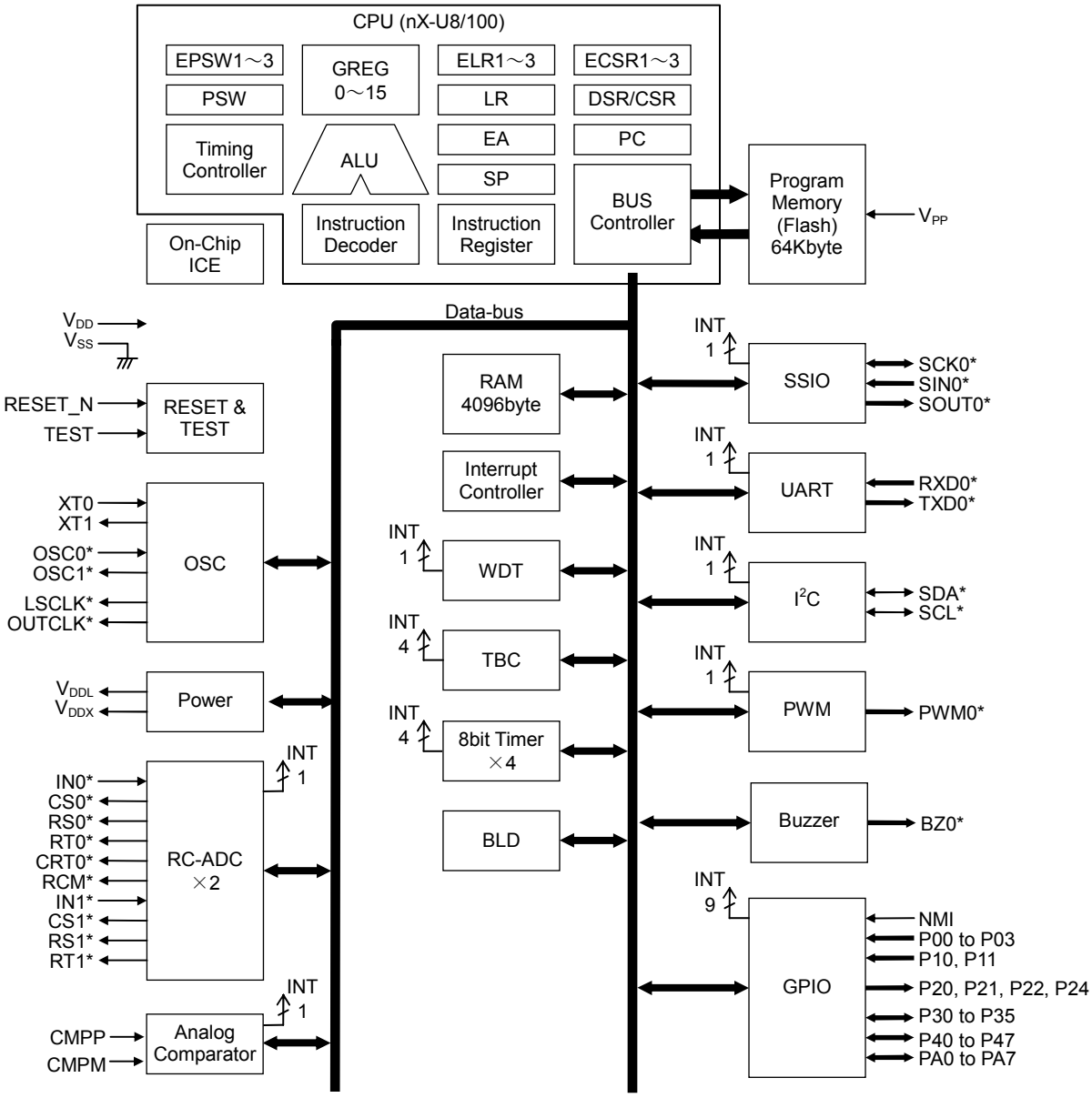
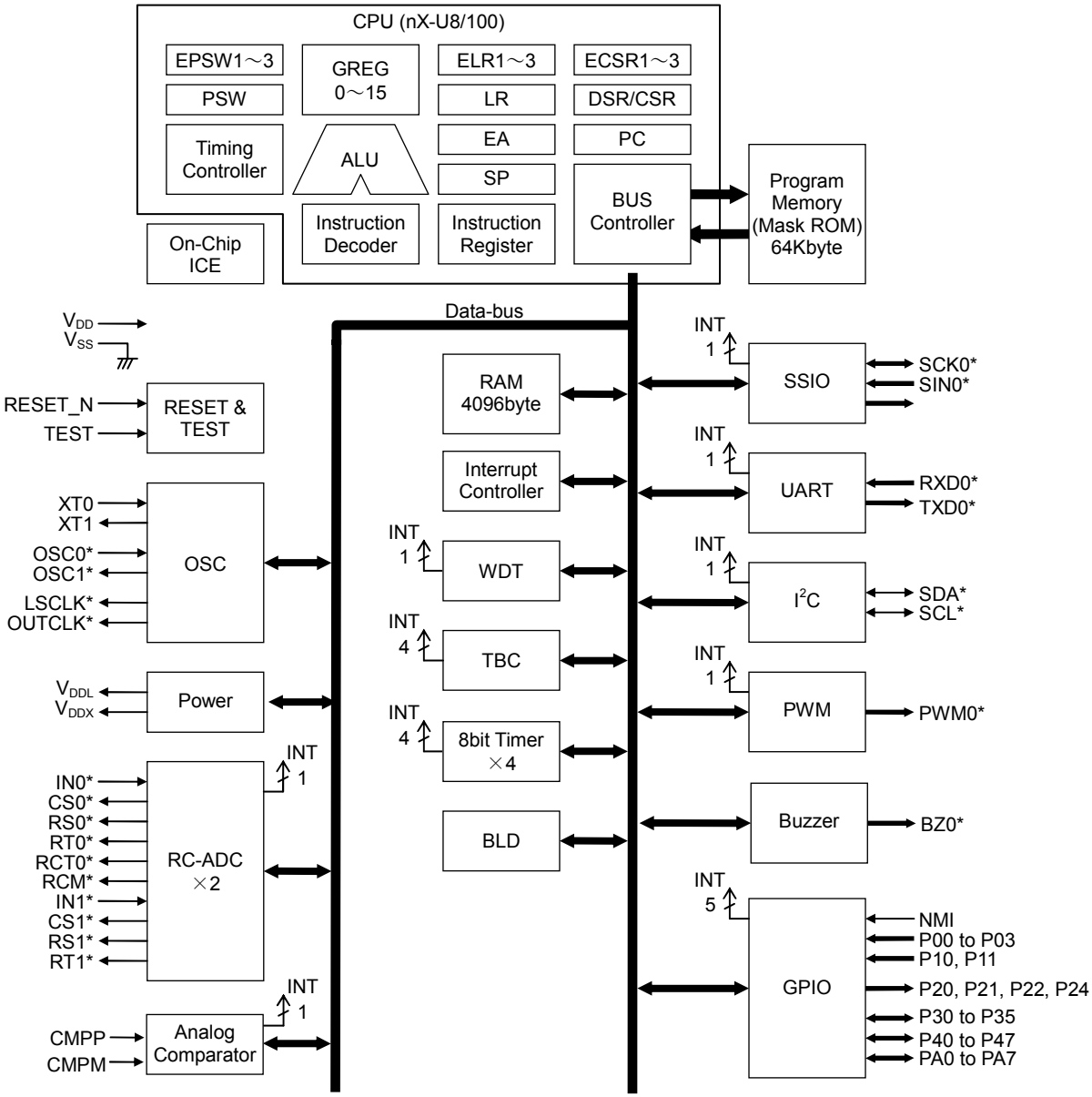


Figure 1 ML610Q482 Block Diagram

ML610482 Block Diagram

Figure 2 show the block diagram of the ML610482.
"*" indicates the secondary function of each port.

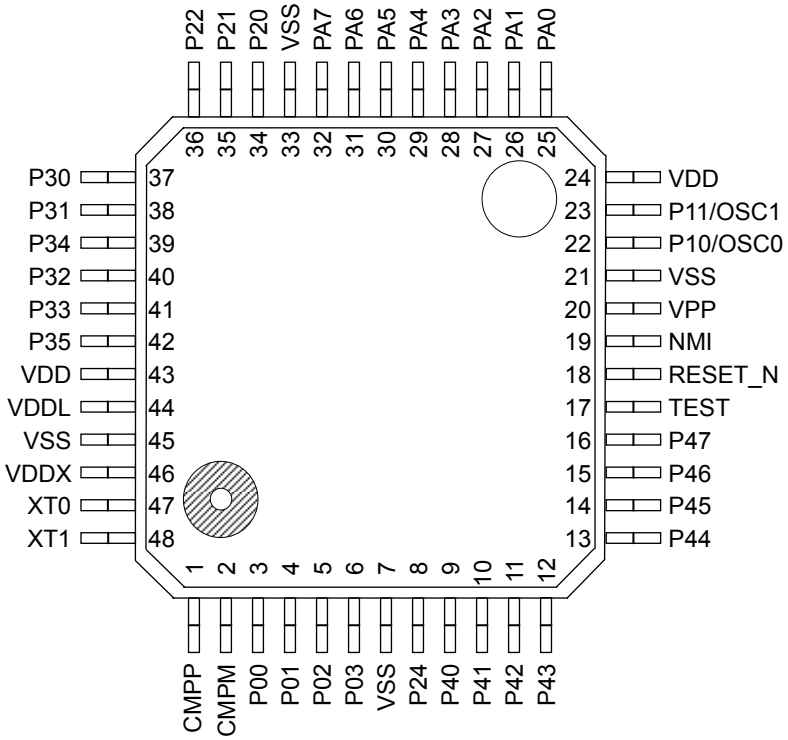


* Secondary function or Tertiary function

Figure 2 ML610482 Block Diagram

PIN CONFIGURATION

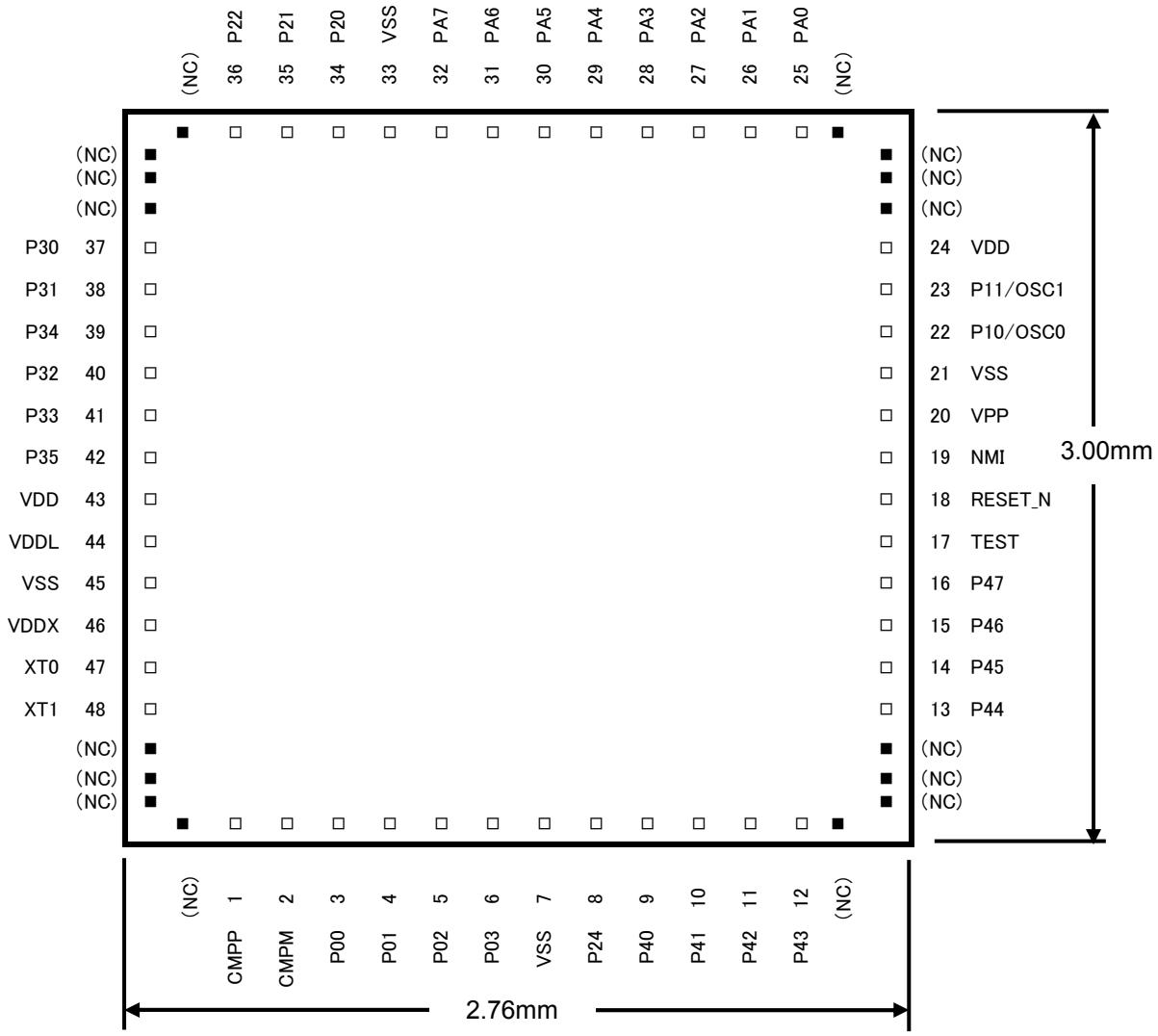
ML610Q482 TQFP48 Pin Layout (Flash ROM version only)



Note:
The assignment of the pads P30 to P35 are not in order.

Figure 3 ML610Q482 TQFP48 Pin Configuration

ML610Q482 Chip Pin Layout & Dimension



(NC): No Connection
Note:
The assignment of the pads P30 to P35 are not in order.

Chip size:	2.76 mm × 3.00 mm
PAD count:	48 pins
Minimum PAD pitch:	100 µm
PAD aperture:	80 µm × 80 µm
Chip thickness:	350 µm
Voltage of the rear side of chip:	V_{SS} level

Figure 4 ML610Q482 Chip Layout & Dimension

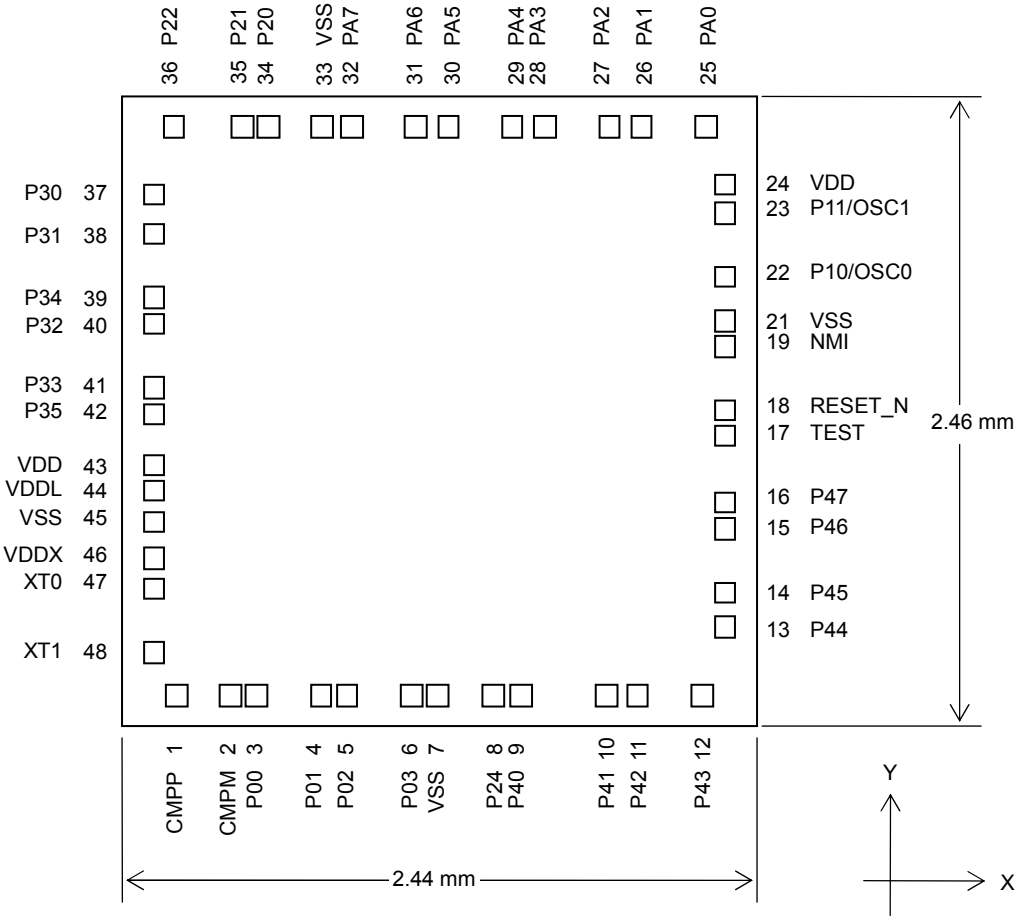
ML610Q482 Pad Coordinates

Table 1 ML610Q482 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	CMPP	-1036.0	-1380.0	25	PA0	1023.0	1380.0
2	CMPM	-830.0	-1380.0	26	PA1	775.0	1380.0
3	P00	-730.0	-1380.0	27	PA2	651.0	1380.0
4	P01	-482.0	-1380.0	28	PA3	403.0	1380.0
5	P02	-382.0	-1380.0	29	PA4	279.0	1380.0
6	P03	-134.0	-1380.0	30	PA5	31.0	1380.0
7	VSS	-34.0	-1380.0	31	PA6	-93.0	1380.0
8	P24	219.0	-1380.0	32	PA7	-341.0	1380.0
9	P40	327.0	-1380.0	33	VSS	-458.0	1380.0
10	P41	655.0	-1380.0	34	P20	-666.0	1380.0
11	P42	775.0	-1380.0	35	P21	-766.0	1380.0
12	P43	1023.0	-1380.0	36	P22	-1032.0	1380.0
13	P44	1260.0	-912.0	37	P30	-1260.0	922.0
14	P45	1260.0	-778.0	38	P31	-1260.0	769.0
15	P46	1260.0	-530.0	39	P34	-1260.0	521.0
16	P47	1260.0	-426.0	40	P32	-1260.0	417.0
17	TEST	1260.0	-167.0	41	P33	-1260.0	169.0
18	RESET_N	1260.0	-67.0	42	P35	-1260.0	67.0
19	NMI	1260.0	181.0	43	VDD	-1260.0	-122.0
20	VPP	1260.0	281.0	44	VDDL	-1260.0	-333.0
21	VSS	1260.0	411.0	45	VSS	-1260.0	-503.0
22	P10	1261.3	610.0	46	VDDX	-1260.0	-673.0
23	P11	1261.3	858.0	47	XT0	-1260.0	-773.0
24	VDD	1260.0	1010.0	48	XT1	-1260.0	-1021.0

ML610482 Chip Pin Layout & Dimension



Note:
The assignment of the pads P30 to P35 are not in order.

Chip size:	2.44 mm × 2.46mm
PAD count:	48 pins
Minimum PAD pitch:	100 µm
PAD aperture:	80 µm × 80 µm
Chip thickness:	350 µm
Voltage of the rear side of chip:	V_{SS} level

Figure 5 ML610482 Chip Layout & Dimension

ML610482 Pad Coordinates

Table 2 ML610482 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	CMPP	-1010	-1110	25	PA0	1025	1110
2	CMPM	-804	-1110	26	PA1	777	1110
3	P00	-704	-1110	27	PA2	653	1110
4	P01	-456	-1110	28	PA3	405	1110
5	P02	-356	-1110	29	PA4	281	1110
6	P03	-108	-1110	30	PA5	33	1110
7	VSS	-8	-1110	31	PA6	-91	1110
8	P24	205	-1110	32	PA7	-339	1110
9	P40	313	-1110	33	VSS	-451	1110
10	P41	641	-1110	34	P20	-659	1110
11	P42	761	-1110	35	P21	-759	1110
12	P43	1009	-1110	36	P22	-1025	1110
13	P44	1100	-842	37	P30	-1100	844
14	P45	1100	-708	38	P31	-1100	691
15	P46	1100	-460	39	P34	-1100	443
16	P47	1100	-356	40	P32	-1100	339
17	TEST	1100	-97	41	P33	-1100	91
18	RESET_N	1100	3	42	P35	-1100	-11
19	NMI	1100	251	43	VDD	-1100	-212
20				44	VDDL	-1100	-312
21	VSS	1100	351	45	VSS	-1100	-434
22	P10	1100	524	46	VDDX	-1100	-574
23	P11	1100	772	47	XT0	-1100	-694
24	VDD	1100	885	48	XT1	-1100	-942

Note: PADNo.20 does not exist.

PIN LIST

PAD No.	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
7,21, 33,45	Vss	—	Negative power supply pin	—	—	—	—	—	—
24,43	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
44	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
46	V_{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—	—	—
20	V_{PP}	—	Power supply pin for Flash ROM	—	—	—	—	—	—
17	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—
18	RESET_N	I	Reset input pin	—	—	—	—	—	—
47	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
48	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
19	NMI	I	Non-maskable interrupt pin	—	—	—	—	—	—
3	P00/EXI 0	I	Input port, External interrupt 0, Capture 0 input	—	—	—	—	—	—
4	P01/EXI 1	I	Input port, External interrupt 1, Capture 1 input	—	—	—	—	—	—
5	P02/EXI 2/RXD0	I	Input port, External interrupt 2, UART0 receive	—	—	—	—	—	—
6	P03/EXI 3	I	Input port, External interrupt 3	—	—	—	—	—	—
1	CMPP	I	Analog comparator non-inverted input	—	—	—	—	—	—
2	CMPM	I	Analog comparator inverted input	—	—	—	—	—	—
22	P10	I	Input port	OSC0	I	High-speed oscillation	—	—	—
23	P11	I	Input port	OSC1	O	High-speed oscillation	—	—	—
34	P20/LE D0	O	Output port	LSCLK	O	Low-speed clock output	—	—	—
35	P21LED 1	O	Output port	OUTCLK	O	High-speed clock output	—	—	—
36	P22/LE D2	O	Output port	BZ0	O	BZ0 output	—	—	—
8	P24/LE D4	O	Output port	PWM0	O	PWM0 output	—	—	—
37	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin	—	—	—
38	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin	—	—	—
40	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin	—	—	—
41	P33	I/O	Input/output port	RT0	O	RC type ADC0 resistor sensor connection pin	—	—	—
39	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin	PWM0	O	PWM0 output

PAD No.	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
42	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor	—	—	—
9	P40	I/O	Input/output port	SDA	I/O	I^2C data input/output	SIN0	I	SSIO data input
10	P41	I/O	Input/output port	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO synchronous clock
11	P42	I/O	Input/output port	RXD0	I	UART data input	SOUT0	I	SSIO data output
12	P43	I/O	Input/output port	TXD0	O	UART data output	PWM0	O	PWM output
13	P44/T02 P0CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	IN1	I	RC type ADC1 oscillation input pin	SIN0	I	SSIO0 data input
14	P45/T13 P1CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin	SCK0	I/O	SSIO0 synchronous clock
15	P46	I/O	Input/output port	RS1	O	RC type ADC1 reference resistor connection pin	SOUT0	O	SSIO0 data output
16	P47	I/O	Input/output port	RT1	O	RC type ADC1 resistor sensor connection pin	—	—	—
25	PA0	I/O	Input/output port	—	—	—	—	—	—
26	PA1	I/O	Input/output port	—	—	—	—	—	—
27	PA2	I/O	Input/output port	—	—	—	—	—	—
28	PA3	I/O	Input/output port	—	—	—	—	—	—
29	PA4	I/O	Input/output port	—	—	—	—	—	—
30	PA5	I/O	Input/output port	—	—	—	—	—	—
31	PA6	I/O	Input/output port	—	—	—	—	—	—
32	PA7	I/O	Input/output port	—	—	—	—	—	—

Note:
*[1]: A VPP terminal exists only ML610Q482.

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V_{SS} as required.	—	—
OSC0	I	Crystal/ceramic connection pin for high-speed clock.	Secondary	—
OSC1	O	A crystal or ceramic is connected to this pin (4.1 MHz max.). Capacitors CDH and CGH (see measuring circuit 1) are connected across this pin and V_{SS}. This pin is used as the secondary function of the P10 pin(OSC0) and P11 pin(OSC1).	Secondary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P03	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P10,P11	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20,P21, P22,P24	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
PA0-PA7	I/O	General-purpose input/output port.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/Secondary	Positive
I^2C bus interface				
SDA	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL	O	I^2C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P24 or P43 or P34 pin.	Tertiary	Positive
T02P0CK	O	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
External interrupt				
NMI	I	External non-maskable interrupt input pin. An interrupt is generated on both edges.	Primary	Positive/ negative
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P03 pins.	Primary	Positive/ negative
Timer				
T02P0CK	I	External clock input pin used for both Timer 0 and Timer 2. The clocks for these timers are selected by software. This pin is used as the primary function of the P44 pin.	Primary	—
T13P1CK	I	External clock input pin used for both Timer 1 and Timer 3. The clocks for these timers are selected by software. This pin is used as the primary function of the P45 pin.	Primary	—
Buzzer				
BZ0	O	Buzzer signal output pin. This pin is used as the secondary function of the P22 pin.	Secondary	Positive/ negative
LED drive				
LED0,1,2,4	O	NMOS open drain output pins to drive LED. These pins are used as the primary function of the P20,P21,P22,P24 pins.	Primary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
CRT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
Analog comparator				
CMPP	I	Non-inverted input pin.	—	—
CMPM	I	Inverted input pin.	—	—
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors CL0 and CL1 (see measuring circuit 1) are connected between this pin and V_{SS}.	—	—
V_{DDX}	—	Plus-side power supply pin (internally generated) for low-speed oscillation. Capacitor Cx (see measuring circuit 1) is connected between this pin and V_{SS}.	—	—
V_{PP}	—	Power supply pin for programming Flash ROM. A pull-up resistor is internally connected.	—	—

Note:

*[1]: A VPP terminal exists only ML610Q482.

TERMINATION OF UNUSED PINS

Table 2 shows methods of terminating the unused pins.

Table 2 Termination of Unused Pins

Pin	Recommended pin termination
V_{PP} *1	Open
RESET_N	Open
TEST	Open
NMI	Open
P00 to P03	V_{DD} or V_{SS}
P10, P11	V_{DD}
P20, P21, P22, P24	Open
P30 to P35	Open
P40 to P47	Open
PA0 to PA7	Open
CMPP,CMPM	V_{DD}

*1: A VPP terminal exists only ML610Q482.

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 2	V_{PP} *1	Ta = 25°C	–0.3 to +9.5	V
Power supply voltage 3	V_{DDL}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 4	V_{DDX}	Ta = 25°C	–0.3 to +3.6	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3–A, Ta = 25°C	–12 to +11	mA
Output current 2	I_{OUT2}	Port2, Ta = 25°C	–12 to +20	mA
Power dissipation	PD	Ta = 25°C	1.16	W
Storage temperature	T_{STG}	—	–55 to +150	°C

*1: ML610Q482 only

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	ML610Q482, ML610482	–20 to +70	°C
		ML610Q482P, ML610482P	–40 to +85	
Operating voltage	V_{DD}	—	1.1 to 3.6	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.1 to 3.6V	30k to 36k	Hz
		V_{DD} = 1.3 to 3.6V	30k to 650k	
		V_{DD} = 1.8 to 3.6V	30k to 4.2M	
Capacitor externally connected to V_{DDL} pin	C_{L0}	—	1.0±30%	µF
	C_{L1}	—	0.1±30%	
Capacitor externally connected to V_{DDX} pin	C_X	—	0.1±30%	µF

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Low-speed crystal oscillation frequency	f_{XTL}	—	—	32.768k/38.4k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R_L	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor *1	C_{DL}/C_{GL}	C_L=6pF of crystal oscillation *2	—	0	—	pF
		C_L=9pF of crystal oscillation	—	6	—	
		C_L=12pF of crystal oscillation	—	12	—	
High-speed crystal/ceramic oscillation frequency	f_{XTH}	—	—	4.0M / 4.096M	—	Hz
High-speed crystal oscillation external capacitor	C_{DH}	—	—	24	—	pF
	C_{GH}	—	—	24	—	

*1: The external C_{DL} and C_{GL} need to be adjusted in consideration of variation of internal loading capacitance C_D and C_G, and other additional capacitance such as PCB layout.
*2: When using a crystal oscillator C_L = 6pF, there is a possibility that can not be adjusted by external C_{DL} and C_{GL}.

OPERATING CONDITIONS OF FLASH ROM (ML610Q482 only)

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase*1	2.75 to 3.6	V
	V_{DDL}	At write/erase*1	2.5 to 2.75	
	V_{PP}	At write/erase*1	7.7 to 8.3	
Write cycles	C_{EP}	—	10	cycles
Data retention	Y_{DR}	—	10	years

*1: Those voltages must be supplied to V_{DDL} pin and V_{PP} pin when programming and eraseing Flash ROM. V_{PP} pin has an internal pulldown resister.

CONDITIONS OF ANALOG COMPARATOR

(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Common mode Input voltage	CMV_{IN}	V_{DD} = 1.8 to 3.6V	0.2	—	V_{DD}−1	V	1
Input offset voltage	V_{CMPOF}	V_{DD} = 1.8 to 3.6V, Ta = 25°C	—	—	50	mV	
Response time	T_{CMP}	V_{DD} = 1.8 to 3.6V, Ta = 25°C Over drive = 100mV	—	—	100	µs	
Wake-up time	T_{CMPw}		—	—	3	ms	
Circuit current (during operation)	I_{CMP}	V_{DD} = 1.8 to 3.6V,Ta = 25°C	—	2	4	µA	

DC CHARACTERISTICS (1/6)

(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

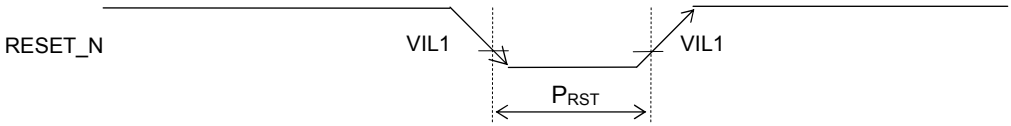
Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
500kHz RC oscillation frequency	f_{RC}	V_{DD} = 1.3 to 3.6V	Ta = 25°C	Typ. −10%	500	Typ. +10%	kHz	1
			Ta = −40 to +85°C	Typ. −35%	500	Typ. +35%	kHz	
PLL oscillation frequency*4	f_{PLL}	LSCLK = 32.768kHz V_{DD} = 1.8 to 3.6V		-2.5%	8.192	+2.5%	MHz	
Low-speed crystal oscillation start time*2	T_{XTL}	—		—	0.3	2	s	
500kHz RC oscillation start time	T_{RC}	—		—	50	500	µs	
High-speed crystal oscillation start time*3	T_{XTH}	V_{DD} = 1.8 to 3.6V		—	2	20	ms	
PLL oscillation start time	T_{PLL}	V_{DD} = 1.8 to 3.6V		—	1	10		
Low-speed oscillation stop detect time*1	T_{STOP}	—		0.2	3	20		
Reset pulse width	P_{RST}	—		200	—	—	µs	
Reset noise elimination pulse width	P_{NRST}	—		—	—	0.3		
Power-on reset activation power rise time	T_{POR}	—		—	—	10	ms	

*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.

*2 : Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C_{GL}/C_{DL}=0pF.

*3 : Use 4.096MHz Crystal Oscillator CHC49SFWB (Kyocera).

*4 : 1024 clock average.



Reset pulse width (P_{RST})

Power-on reset activation power rise time (T_{POR})

DC CHARACTERISTICS (2/6)

(VDD = 1.1 to 3.6V, VSS = 0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
BLD threshold voltage	V_{BLD}	V_{DD} = 1.35 to 3.6V	LD2–0 = 0H	Typ. –2%	1.35	Typ. +2%	V	1
			LD2–0 = 1H		1.4			
			LD2–0 = 2H		1.45			
			LD2–0 = 3H		1.5			
			LD2–0 = 4H		1.6			
			LD2–0 = 5H		1.7			
			LD2–0 = 6H		1.8			
			LD2–0 = 7H		1.9			
			LD2–0 = 8H		2.0			
			LD2–0 = 9H		2.1			
			LD2–0 = 0AH		2.2			
			LD2–0 = 0BH		2.3			
			LD2–0 = 0CH		2.4			
			LD2–0 = 0DH		2.5			
			LD2–0 = 0EH		2.7			
			LD2–0 = 0FH		2.9			
BLD threshold voltage temperature deviation	ΔV_{BLD}	V_{DD} = 1.35 to 3.6V		—	0.1	—	%/°C	

DC CHARACTERISTICS (ML610Q482) (3/6)

(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	Ta = 25°C	—	0.2	0.5	µA	1
			—	—	—	5		
Supply current 2	IDD2	CPU: In HALT state (LTBC, WDT: Operating*2*4). High-speed oscillation: Stopped.	Ta = 25°C	—	0.5	1.3	µA	
			—	—	—	6		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*1*2 High-speed oscillation: Stopped.	Ta = 25°C	—	5	7	µA	
			—	—	—	12		
Supply current 4	IDD4	CPU: In 500kHz CR operating state.	Ta = 25°C	—	70	85	µA	
			—	—	—	100		
Supply current 5	IDD5	CPU: In 4.096MHz operating state*2.PLL: In oscillating state. V_{DD} = 1.8 to 3.6V	Ta = 25°C	—	0.83	1	mA	
			—	—	—	1.2		
Supply current 6	IDD6	CPU: In 4.096MHz operating state.Crystal/ceramic: In oscillating state. *2*3 V_{DD} = 3.0V	Ta = 25°C	—	1.3	1.4	mA	
			—	—	—	2.0		

*1: When the CPU operating rate is 100% (No HALT state).
*2: Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C_{GL}/C_{DL}=0pF.
*3: Use 4.096MHz Crystal Oscillator HC49SFWB (Kyocera).
*4: Significant bits of BLKCON0~BLKCON4 registers are all "1".

DC CHARACTERISTICS (ML610482) (4/6)

(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	Ta = 25°C	—	0.2	0.5	µA	1
			—	—	—	2.5		
Supply current 2	IDD2	CPU: In HALT state (LTBC, WDT: Operating*2*4). High-speed oscillation: Stopped.	Ta = 25°C	—	0.5	1.3	µA	
			—	—	—	3.5		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*1*2 High-speed oscillation: Stopped.	Ta = 25°C	—	3	5	µA	
			—	—	—	8		
Supply current 4	IDD4	CPU: In 500kHz CR operating state.	Ta = 25°C	—	40	65	µA	
			—	—	—	75		
Supply current 5	IDD5	CPU: In 4.096MHz operating state*2.PLL: In oscillating state. V_{DD} = 1.8 to 3.6V	Ta = 25°C	—	0.5	0.65	mA	
			—	—	—	0.75		
Supply current 6	IDD6	CPU: In 4.096MHz operating state.Crystal/ceramic: In oscillating state. *2*3 V_{DD} = 3.0V	Ta = 25°C	—	0.9	1.1	mA	
			—	—	—	1.3		

*1: When the CPU operating rate is 100% (No HALT state).
*2: Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C_{GL}/C_{DL}=0pF.
*3: Use 4.096MHz Crystal Oscillator HC49SFWB (Kyocera).
*4: Significant bits of BLKCON0~BLKCON4 registers are all “1”.

DC CHARACTERISTICS (5/6)

(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Output voltage 1 (P20, P21, P22, P24/2nd function is selected) (P30–P35) (P40–P47) (PA0–PA7)	VOH1	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V		V_{DD} –0.5	—	—	V	2
		IOH1 = -0.1mA, V_{DD} = 1.3 to 3.6V		V_{DD} –0.3	—	—		
		IOH1 = -0.03mA, V_{DD} = 1.1 to 3.6V		V_{DD} –0.3				
	VOL1	IOL1 = +0.5mA, V_{DD} = 1.8 to 3.6V		—	—	0.5		
		IOL1 = +0.1mA, V_{DD} = 1.3 to 3.6V		—	—	0.5		
		IOL1 = +0.03mA, V_{DD} = 1.1 to 3.6V		—	—	0.3		
Output voltage 2 (P20, P21, P22, P24/2nd function is Not selected)	VOL2	IOL2 = +5mA, V_{DD} = 1.8 to 3.6V		—	—	0.5		
Output voltage 3 (P40, P41)	VOL3	IOL3 = +3mA, V_{DD} = 2.0 to 3.6V (when I^2C mode is selected)		—	—	0.4		
Output leakage (P20, P21, P22, P24) (P30–P35) (P40–P47) (PA0–PA7)*1	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	µA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		–1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}		0	—	1	µA	4
	IIL1	VIL1 = V_{SS}	V_{DD} = 1.8 to 3.6V	–600	–300	–20		
			V_{DD} = 1.3 to 3.6V	–600	–300	-10		
			V_{DD} = 1.1 to 3.6V	–600	–300	-2		
Input current 1 (TEST)	IIH1	VIH1 = V_{DD}	V_{DD} = 1.8 to 3.6V	20	300	600		
			V_{DD} = 1.3 to 3.6V	10	300	600		
			V_{DD} = 1.1 to 3.6V	2	300	600		
	IIL1	VIL1 = V_{ss}		-1	—	—		
Input current 2 (NMI) (P00–P03) (P10, P11) (P30–P35) (P40–P47) (PA0–PA7)	IIH2	VIH2 = V_{DD} (when pulled-down)	V_{DD} = 1.8 to 3.6V	2	30	200		
			V_{DD} = 1.3 to 3.6V	0.2	30	200		
			V_{DD} = 1.1 to 3.6V	0.01	30	200		
	IIL2	VIL2 = V_{SS} (when pulled-up)	V_{DD} = 1.8 to 3.6V	–200	–30	–2		
			V_{DD} = 1.3 to 3.6V	–200	–30	-0.2		
			V_{DD} = 1.1 to 3.6V	–200	–30	-0.01		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)		—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)		–1	—	—		

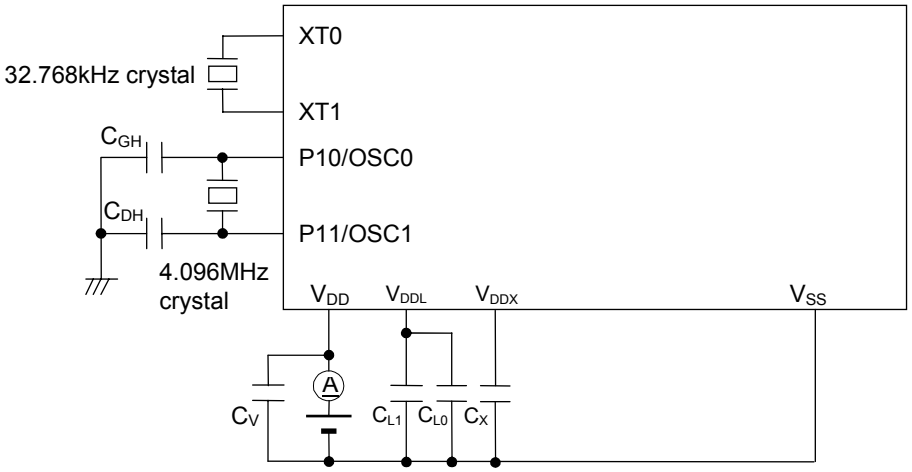
DC CHARACTERISTICS (6/6)

(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST) (NMI) (P00–P03) (P10, P11) (P31–P35) (P40–P43) (P45–P47) (PA0–PA7)*1	VIH1	V_{DD} = 1.3 to 3.6V	0.7 ×V_{DD}	—	V_{DD}	V	5
		V_{DD} = 1.1 to 3.6V	0.7 ×V_{DD}	—	V_{DD}		
	VIL1	V_{DD} = 1.3 to 3.6V	0	—	0.3 ×V_{DD}		
		V_{DD} = 1.1 to 3.6V	0	—	0.2 ×V_{DD}		
Input voltage 2 (P30, P44)	VIH2	—	0.7 ×V_{DD}	—	V_{DD}		
	VIL2	—	0	—	0.3 ×V_{DD}		
Input pin capacitance (NMI) (P00–P03) (P10, P11) (P30–P35) (P40–P47) (PA0–PA7)	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	5	pF	—

MEASURING CIRCUITS

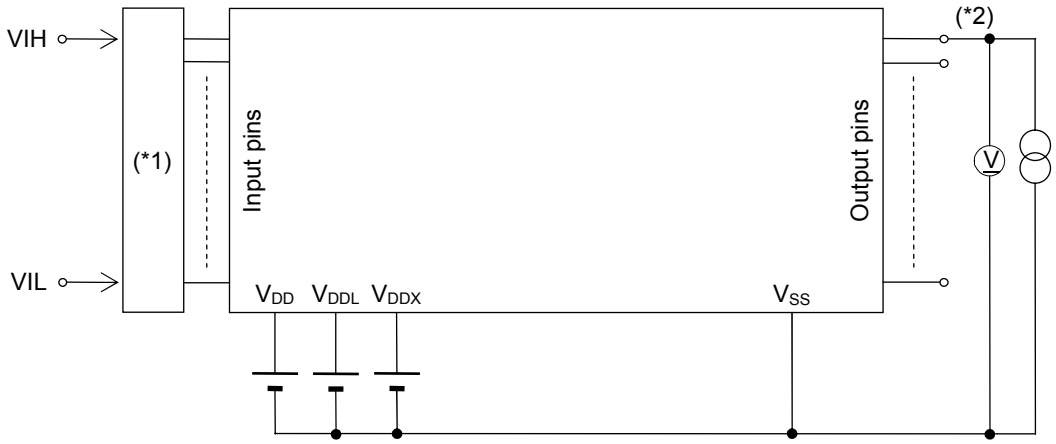
MEASURING CIRCUIT 1



C_V:	1μF
C_{L0}:	1μF
C_{L1}:	0.1μF
C_X:	0.1μF
C_{GH}:	24pF
C_{DH}:	24pF

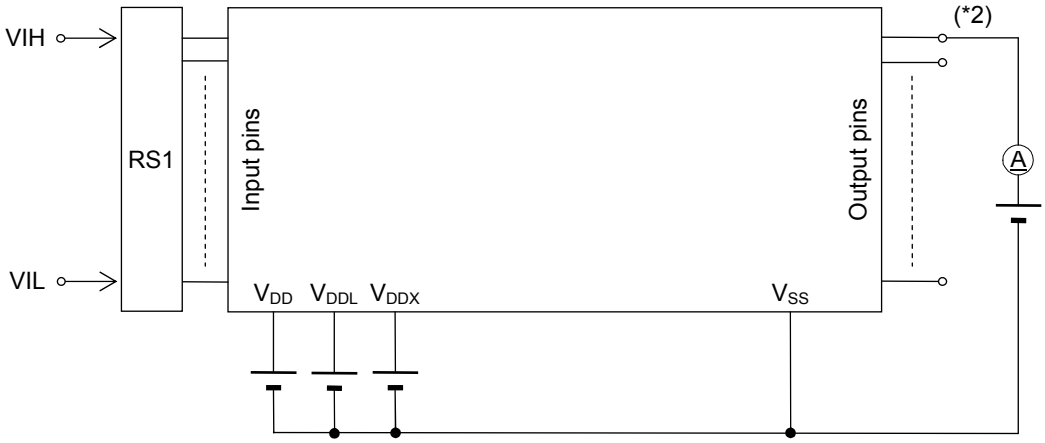
32.768kHz crystal:
C-001R (Epson Toyocom)
4.096MHz crystal:
HC49SFWB (Kyocera)

MEASURING CIRCUIT 2



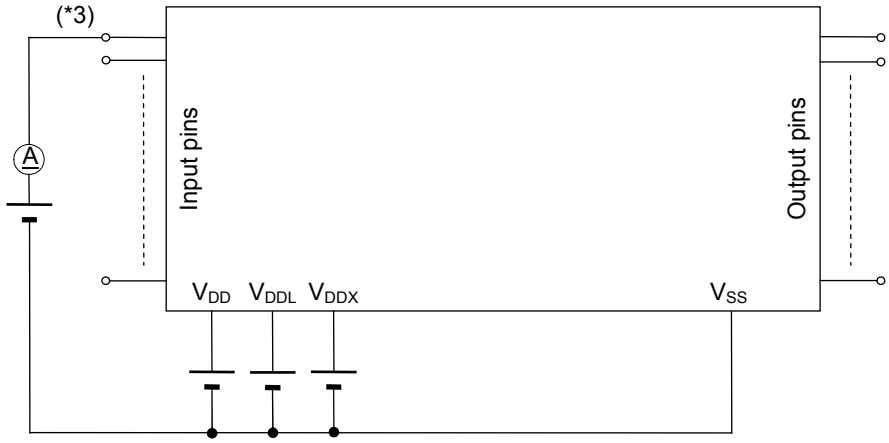
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

MEASURING CIRCUIT 3



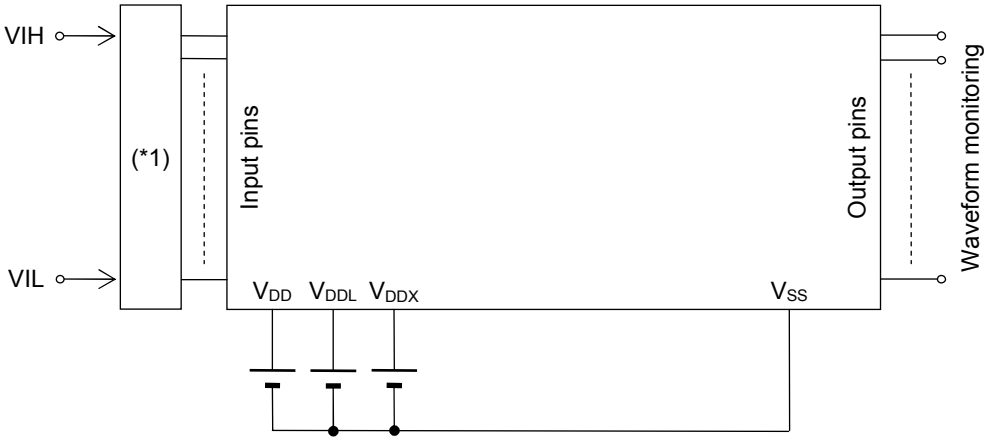
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

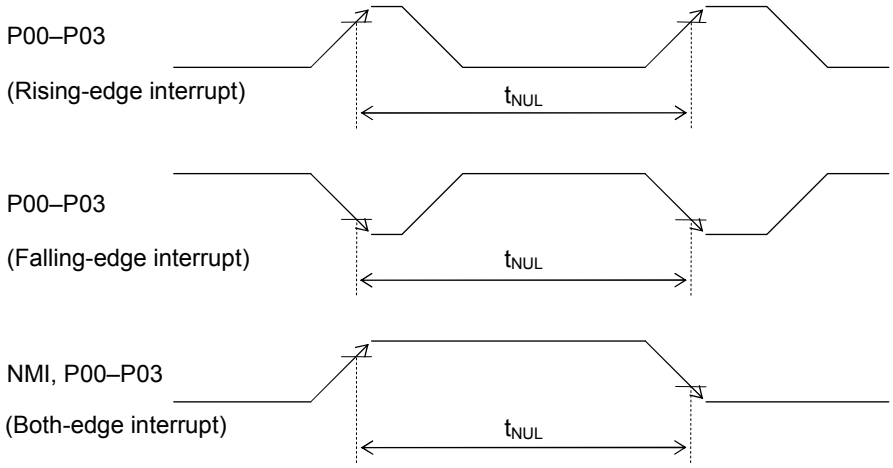


*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	µs

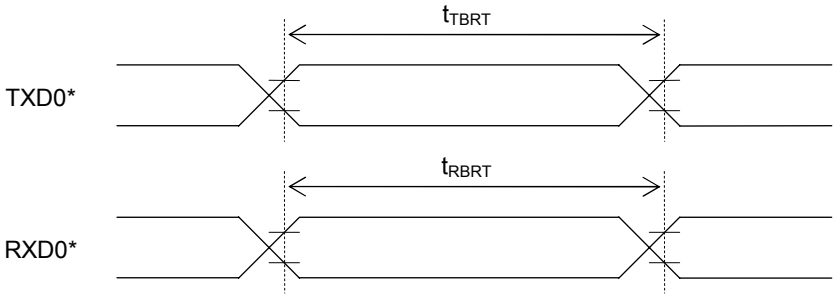


AC CHARACTERISTICS (UART)

(V_{DD} = 1.3 to 3.6V, V_{SS} = 0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*1	—	s
Receive baud rate	t_{RBRT}	—	BRT*1 −3%	BRT*1	BRT*1 +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the UART0 baud rate register (UA0BRTL,H) and the UART0 mode register 0 (UA0MOD0).



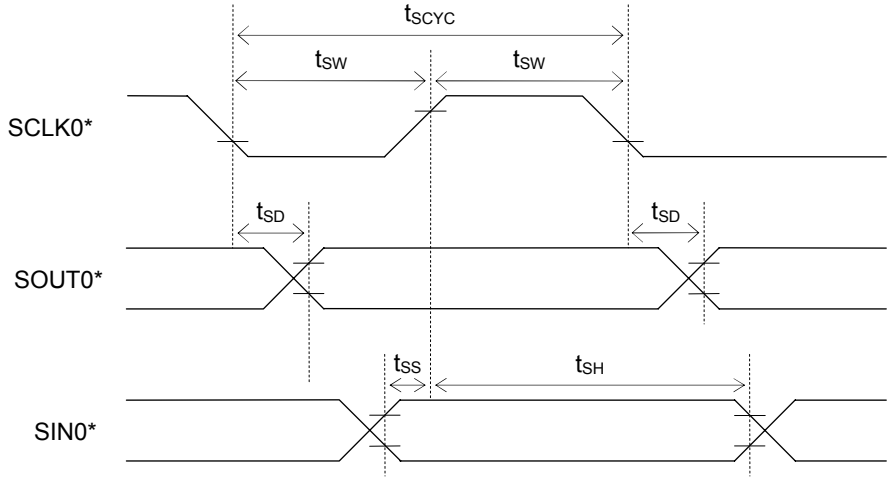
*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

(V_{DD} = 1.3 to 3.6V, V_{SS} = 0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	When RC oscillation is active *2 (V_{DD} = 1.3 to 3.6V)	10	—	—	µs
		When high-speed oscillation is active *3(V_{DD} = 1.8 to 3.6V)	1	—	—	µs
SCLK output cycle (master mode)	t_{SCYC}	—	—	SCLK*1	—	s
SCLK input pulse width (slave mode)	t_{SW}	When RC oscillation is active *2 (V_{DD} = 1.3 to 3.6V)	4	—	—	µs
		When high-speed oscillation is active *3(V_{DD} = 1.8 to 3.6V)	0.4	—	—	µs
SCLK output pulse width (master mode)	t_{SW}	—	SCLK*1 ×0.4	SCLK*1 ×0.5	SCLK*1 ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	When RC oscillation is active *2 (V_{DD} = 1.3 to 3.6V)	—	—	500	ns
		When high-speed oscillation is active *3(V_{DD} = 1.8 to 3.6V)			240	
SOUT output delay time (master mode)	t_{SD}	When RC oscillation is active *2 (V_{DD} = 1.3 to 3.6V)	—	—	500	ns
		When high-speed oscillation is active *3(V_{DD} = 1.8 to 3.6V)			240	
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	When RC oscillation is active *2 (V_{DD} = 1.3 to 3.6V)	500	—	—	ns
		When high-speed oscillation is active *3(V_{DD} = 1.8 to 3.6V)	240	—	—	
SIN input hold time	t_{SH}	When RC oscillation is active *2 (V_{DD} = 1.3 to 3.6V)	300	—	—	ns
		When high-speed oscillation is active *3(V_{DD} = 1.8 to 3.6V)	80	—	—	

*1: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)
*2: When RC oscillation is selected with OSCM1–0 of the frequency control register (FCON0)
*3: When Crystal/ceramic oscillation , built-in PLL oscillation , or external clock input is selected with OSCM1–0 of the frequency control register (FCON0)



*: Indicates the secondary function of the port.

AC CHARACTERISTICS (I^2C Bus Interface: Standard Mode 100kbit/s)

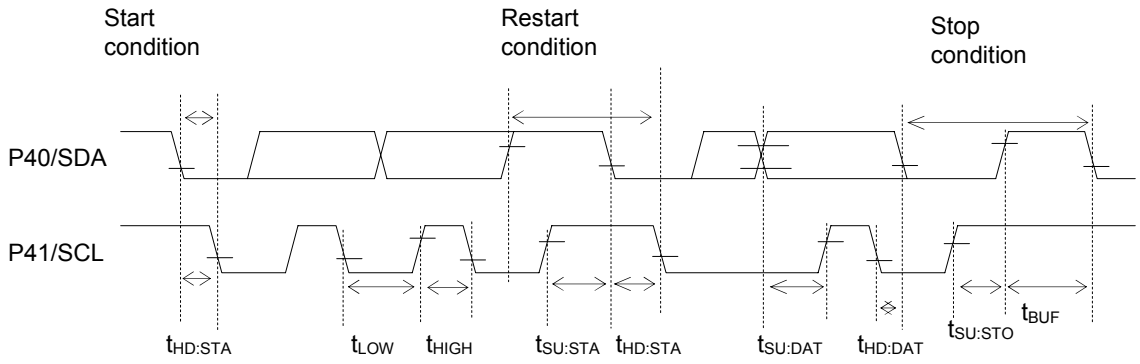
(V_{DD} = 1.8 to 3.6V, V_{SS} = 0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

AC CHARACTERISTICS (I^2C Bus Interface: Fast Mode 400kbit/s)

(V_{DD} = 1.8 to 3.6V, V_{SS} = 0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL "L" level time	t_{LOW}	—	1.3	—	—	µs
SCL "H" level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs



AC CHARACTERISTICS (RC Oscillation A/D Converter)

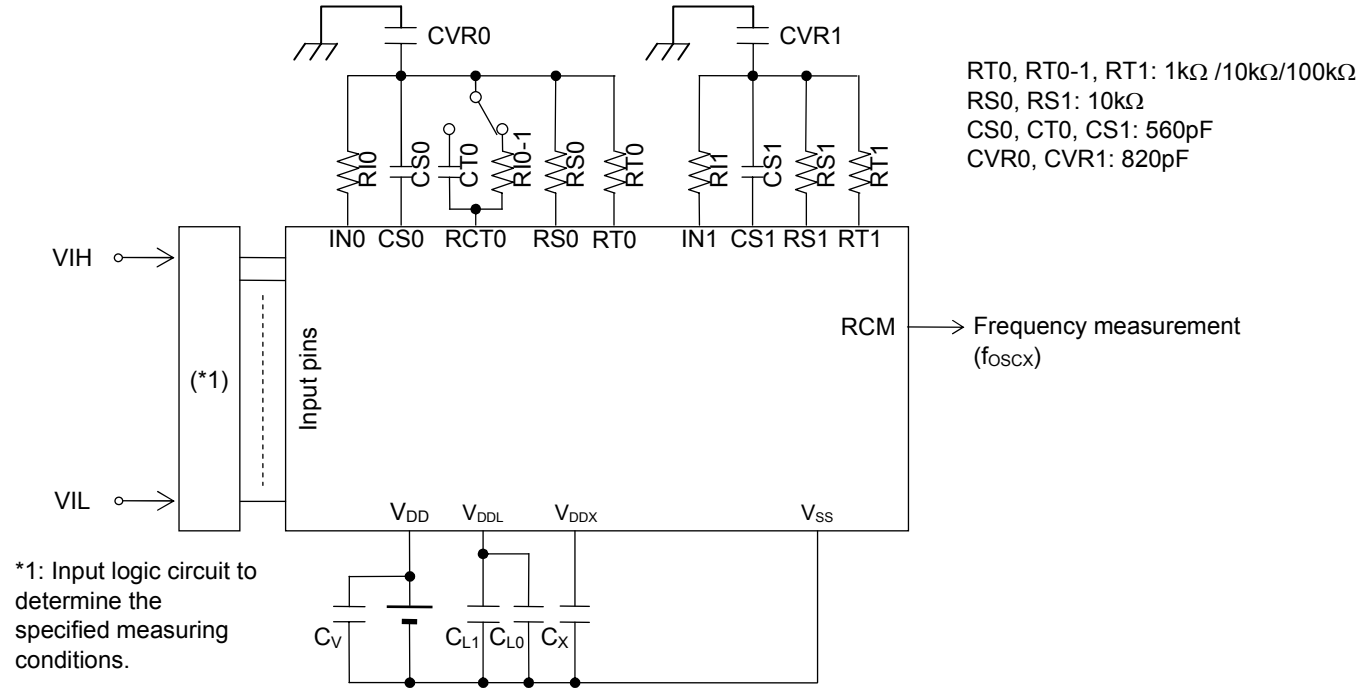
(V_{DD} = 1.3 to 3.6V, V_{SS} = 0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resistors for oscillation	RS0, RS1, RT0, RT0-1,RT1	CS0, CT0, CS1 ≥ 740pF	1	—	—	kΩ
Oscillation frequency VDD = 1.5V	f_{OSC1}	Resistor for oscillation = 1kΩ	209.4	330.6	435.1	kHz
	f_{OSC2}	Resistor for oscillation = 10kΩ	41.29	55.27	64.16	kHz
	f_{OSC3}	Resistor for oscillation = 100kΩ	4.71	5.97	7.06	kHz
RS to RT oscillation frequency ratio *1 VDD = 1.5V	Kf1	RT0, RT0-1, RT1 = 1kHz	5.567	5.982	6.225	—
	Kf2	RT0, RT0-1, RT1 = 10kHz	0.99	1	1.01	—
	Kf3	RT0, RT0-1, RT1 = 100kHz	0.104	0.108	0.118	—
Oscillation frequency VDD = 3.0V	f_{OSC1}	Resistor for oscillation = 1kΩ	407.3	486.7	594.6	kHz
	f_{OSC2}	Resistor for oscillation = 10kΩ	49.76	59.28	72.76	kHz
	f_{OSC3}	Resistor for oscillation = 100kΩ	5.04	5.993	7.04	kHz
RS to RT oscillation frequency ratio *1 VDD = 3.0V	Kf1	RT0, RT0-1, RT1 = 1kHz	8.006	8.210	8.416	—
	Kf2	RT0, RT0-1, RT1 = 10kHz	0.99	1	1.01	—
	Kf3	RT0, RT0-1, RT1 = 100kHz	0.100	0.108	0.115	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(RT0\text{–}CS0\ oscillation)}{f_{OSCx}(RS0\text{–}CS0\ oscillation)}, \frac{f_{OSCx}(RT0\text{-}1\text{–}CS0\ oscillation)}{f_{OSCx}(RS0\text{–}CS0\ oscillation)}, \frac{f_{OSCx}(RT1\text{–}CS1\ oscillation)}{f_{OSCx}(RS1\text{–}CS1\ oscillation)}$$

(x = 1, 2, 3)

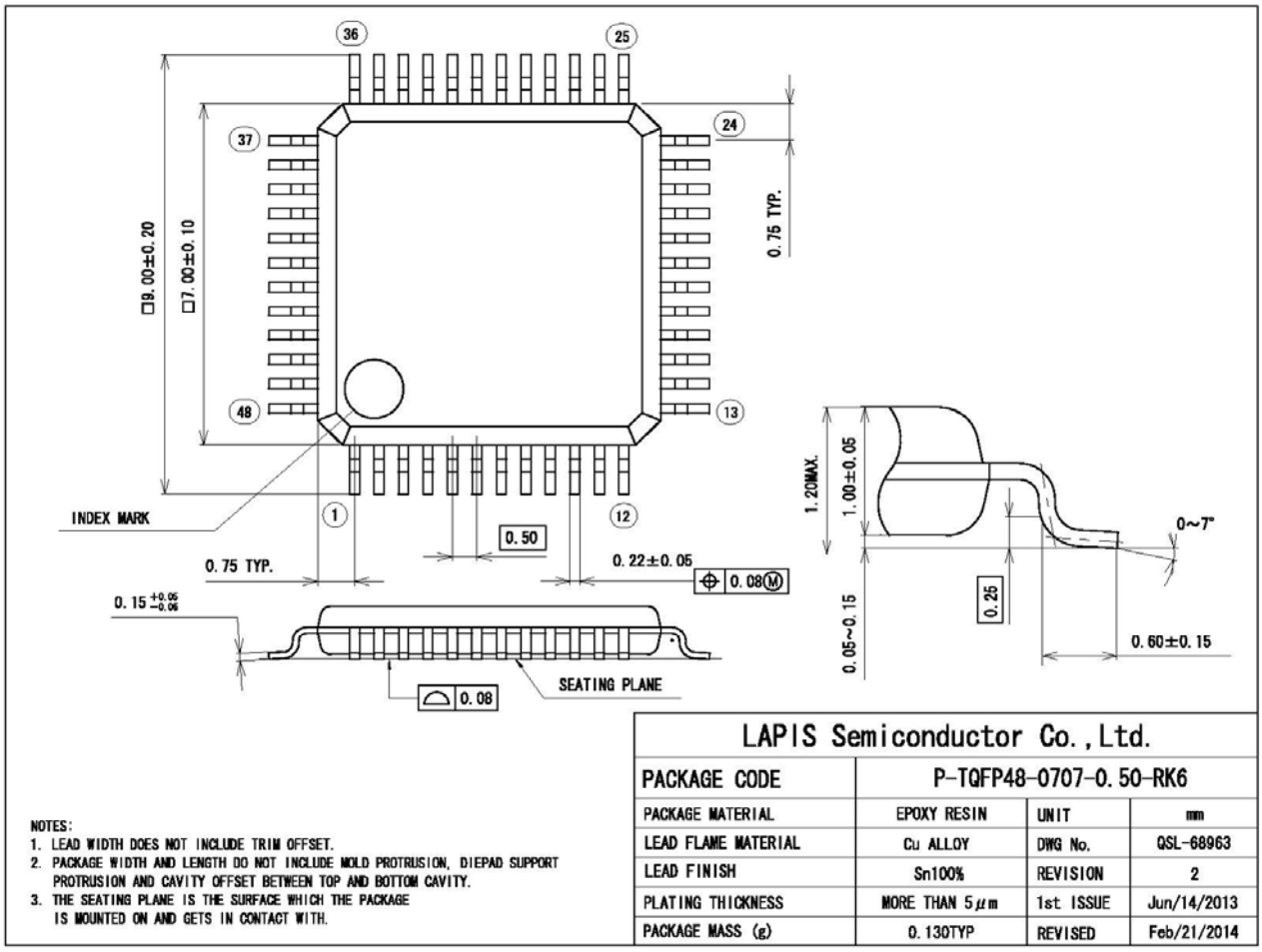


Note:

- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.
- Please make wiring to components (capacitor, resisteor and etc.) necessory for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

PACKAGE DIMENSIONS

(Unit: mm)



LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-TQFP48-0707-0.50-RK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68963
LEAD FINISH	Sn100%	REVISION	2
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jun/14/2013
PACKAGE MASS (g)	0.130TYP	REVISED	Feb/21/2014

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q482P-01	Dec.9, 2009	–	–	Formally edition 1
FEDL610Q482-02	May.9,2014	All	All	Change header and footer
		1,3,4,5,6, 7,9,12,14 ,1516,17, 18,21,22, 23,24	1,3,4,5,6, 7,,8,9,10, 11,13,16, 1718,19, 20,21,22, 23,26,27, 28,29	Add ML610Q482, ML610482 and ML610482P
		3	4	Change from "Shipment" to " Product name – Supported Function "
		-	18	
		18	19	Change "RESET" to "Reset pulse width (P_{RST})" and " Power-on reset activation power rise time (T_{POR})".
		29	30	Update Package Dimensions

NOTES

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