Ordering number : EN*A1990

Preliminary

SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

# LV23411V — Bi-CMOS LSI For Home Stereo Systems FM/AM Tuner IC

## Overview

The LV23411V is single chip tuner IC, and FM/AM radio is able to be realized with few external parts.

## Functions

- FM tuner
- AM tuner
- MPX Stereo Decoder
- Tuning system

## Features

- No alignments necessary
- Reduction of external component counts
- Large audio output signal is available for home stereo systems
- Worldwide FM band support (64 to 108MHz)
- Worldwide AM band support (520 to 1710kHz)
- Soft-mute, Stereo-blend function
- LV23411 corresponds to Europe Immunity standard (EN55020-S1)
- $I^2C$ control interface




SANYO Semiconductor Co., Ltd.
http://semicon.sanyo.com/en/network

# Specifications

## Absolute Maximum Ratings at Ta = 25°C, GND1 = GND2 = GND3 = GND4 = GND5 = 0V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{CC}$ max | | 10.0 | V |
| Digital output voltage | $V_O$ max | SDA | 3.6 | V |
| Digital input voltage | $V_{IN}1$ max | SDA, SCL | 3.6 | V |
| | $V_{IN}2$ max | CLK IN | 3.6 | V |
| Allowable power dissipation | Pd max | Ta ≤ 70°C *1 | 450 | mW |
| Operating temperature | Topr | | -20 to +70 | °C |
| Storage temperature | Tstg | | -40 to +125 | °C |

*1 : Mounted on a specified board. Board size is 114.3mm × 76.1mm × 1.6mm, glass epoxy.

## Operating Conditions at Ta = 25°C, GND1 = GND2 = GND3 = GND4 = GND5 = 0V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Recommended supply voltage | $V_{CC}$ | | 9.0 | V |
| Operating supply voltage Range * Note | $V_{CC}$ op | Register 1Eh bit 1 (LEVSHIF) = 0 | 4.5 to 6.5 | V |
| | | Register 1Eh bit 1 (LEVSHIF) = 1 | 8.5 to 9.5 | V |

* Note : supply the stabilized voltage.

## Interface Conditions at Ta = -20 to +70°C, GND1 = GND2 = GND3 = GND4 = GND5 = 0V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| High level input voltage | $V_{IH}1$ | SDA, SCL | 2.3 | | 3.5 | V |
| | $V_{IH}2$ | CLK IN | 2.3 | | 3.5 | V |
| Low level input voltage | $V_{IL}1$ | SDA, SCL | 0 | | 0.5 | V |
| | $V_{IL}2$ | CLK IN | 0 | | 0.3 | V |
| Output voltage | $V_O$ | SDA | 0 | | 3.5 | V |
| Crystal frequency | fin | CLK IN | | 32.768 | | kHz |
| Crystal frequency accuracy | faccuracy | | -100 | | +100 | ppm |

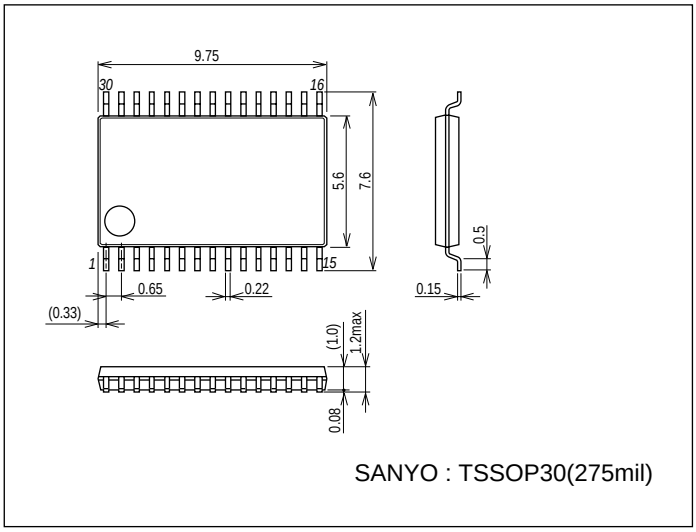
## Operating Characteristics at Ta = 25°C, $V_{CC}$ = 9.0V, with the designated circuit.

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| [FM characteristics ; MONO] : fc = 98MHz, $V_{IN}$ = 60dBμV, fm = 1kHz, De-emphasis = 50μs, IF = 225KHz, BW = 45%<br>MONO : 75kHz dev<br>STEREO : L+R = 67.5kHz dev, Pilot = 7.5kHz dev<br>Volume level = 3, Register 1Eh bit 1 (LEVSHIF) = 1, Pin 9 output, Audio filter = IHF-BP F, Soft mute = off ,Soft stereo = off | | | | | | |
| Current drain | $I_{CC}$ FM | No input | 35 | 40 | 45 | mA |
| 30dB S/N sensitivity | SN30 | S/N = 30dB input level | | 10 | 15 | dBμV |
| Signal-to-noise ratio | SNR | MONO | 62 | 70 | | dB |
| Total harmonic distortion | THD | MONO | | 0.5 | 1.5 | % |
| | THD-ST | STEREO | | 0.5 | 2.5 | % |
| Demodulation output | $V_O$3 | MONO | 518 | 775 | 1160 | mVrms |
| SD operation level | SD | FS = 4 | 17 | 25 | 33 | dBμV |
| Mute attenuation | Mute | MONO | 60 | 75 | | dB |
| Stereo separation | Sep | Pin 10 output/Pin 9 output | 20 | 35 | | dB |
| Carrier leak | CL | STEREO SNR, Audio filter = OFF | 30 | 40 | | dB |
| Stereo on level | ST-ON | L+R = 67.5kHz dev, Pilot level | | 3.0 | 6.5 | % |
| [AM characteristics] : fc = 1MHz, $V_{IN}$ = 94dBμV, fm = 400Hz, mod = 30% IF = 53KHz, BW = 50%<br>Volume level = 2, Register 1Eh bit 1 (LEVSHIF) = 1, Pin 9 output, Audio filter = 15kHz LPF OFF | | | | | | |
| Current drain | $I_{CC}$ AM | No input | 30 | 35 | 40 | mA |
| 20dB S/N sensitivity | SN20 | S/N = 20dB input level | | 48 | 65 | dBμV |
| Signal-to-noise ratio | SNR | | 42 | 50 | | dB |
| Total harmonic distortion | THD | | | 0.8 | 2.8 | % |
| Demodulation output | $V_O$2 | | 122 | 173 | 245 | mVrms |
| SD operation level | SD | FS = 4 | 46 | 54 | 64 | dBμV |
| Mute attenuation | Mute | 15kHz LPF ON | 50 | 65 | | dB |

## Package Dimensions

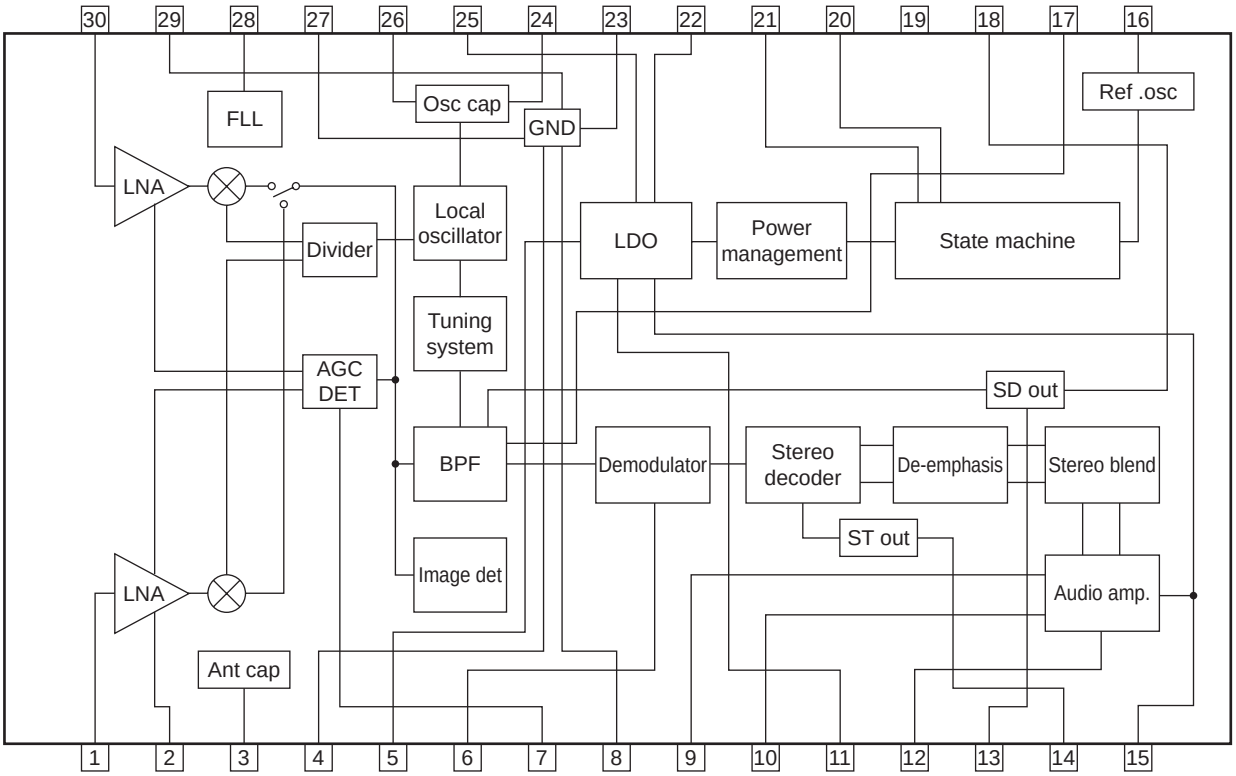
unit : mm (typ)

3259




SANYO : TSSOP30(275mil)

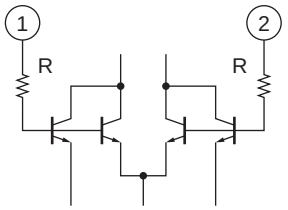
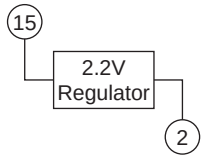
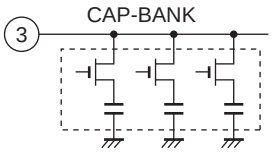
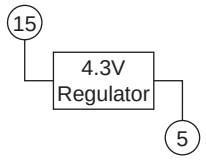
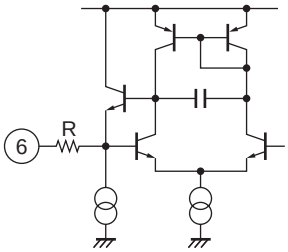
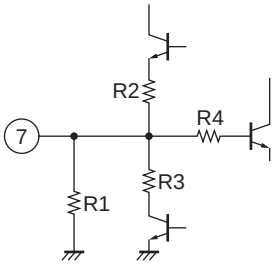
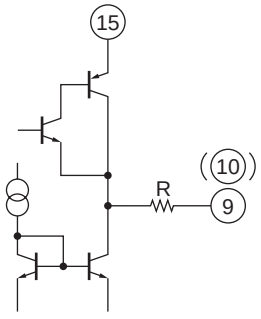
## Block Diagram



## Pin descriptions

| Pin | Pin name | I/O | Descriptions | Remarks | DC voltage |
|---|---|---|---|---|---|
| 1 | AM-ANT | I | AM antenna input | Connect to pin2 through Matching coil or Ferrite antenna. | - |
| 2 | AM-REF | O | Reference voltage for AM part | Connect to pin1 through Matching coil or Ferrite antenna. | 2.2V |
| 3 | AM-CAP | I | AM capacitor bank | Exteranal inductor (recommendation value) is connected between this pin and GND. | - |
| 4 | GND1 | - | AM antenna GND | Connected to GND | 0V |
| 5 | VREF1 | O | Reference voltage for analog | Capacitor of 1μF is connected between this pin and GND. | 4.3V |
| 6 | MPX IN_OUT | O | Demodulato output | When RDS used, LC72725 is applicable | 2.5V |
| 7 | AM RF-AGC | O | AM RF AGC output | Capacitor of 1μF is connected between this pin and GND. | - |
| 8 | GND2 | - | Analog GND | Connected to GND | 0V |
| 9 | L-OUT | O | Audio Lch output | According to the $V_{CC}$_application, Reference Output_level setting is cangeable by Register Bit.<br>Register 1Eh bit 1 (LEVSHIF) =1:<br>Register 1Eh bit 1 (LEVSHIF) =0: | 2.6V<br>(3.7V) |
| 10 | R-OUT | O | Audio Rch output | | |
| 11 | $V_{CC}$-Low | - | Voltage supply pin at low voltage operation mode | When using $V_{CC}$ < 6V, Connect to Pin15 directly | - |
| 12 | AM LCF | O | AM low_cut filter | Capacitor of 0.047uF is connected between this pin and GND. | 2.2V |
| 13 | SD-OUT | O | SD indicator output | Active low output | 3.0V<br>(0.1V) |
| 14 | ST-OUT | O | ST indicator output | Active low output | 3.0V<br>(0.1V) |
| 15 | $V_{CC}$ | - | Voltage supply pin | | - |
| 16 | CLK_IN | I | Reference clock input | 32.768kHz crystal connected to GND.<br>It is Also applicable to input directly clock signals ( square wave GND_reference) | - |
| 17 | IF AGC CAP | - | IF-AGC monitor point (test) | Open | - |
| 18 | SD-ADJ | - | Adjustment for SD on level | Incase of changing SD on level, put Resistor between this pin and GND. | - |
| 19 | NC | I | | | - |
| 20 | SCL | I | $I^2C$ interface CLK input | | - |
| 21 | SDA | I/O | $I^2C$ interface Data input/output | | - |
| 22 | VREF2 | O | Output voltage pin for $V_{DD}$ | $V_{DD}$ output_pin of 3.0V.<br>This pin is applicable to supply the current other IC up to 10mA. | 3.0V |
| 23 | GND3 | - | Digital GND for control part | | 0V |
| 24 | L1 | - | Local oscillator | 39nH connected to pin 25 | - |
| 25 | VREF3 | O | Reference voltage for local OSC part | | 5.0V |
| 26 | L2 | - | Local oscillator | 39nH connected to pin 25 | - |
| 27 | GND4 | - | Analog GND for OSC part | Connected to GND | 0V |
| 28 | FLL-CAP | - | Oscillator tuning voltage output | Capacitor of 0.1μF is connected between this pin and GND. | - |
| 29 | GND5 | - | Analog GND for FMRF part | Connected to GND | 0V |
| 30 | FM-ANT | I | FM antenna input 1 | Input impedance is 75Ω | 0.8V |

## Pin internal circuit description

| Pin No. | Pin name | Pin voltage (V) | Description | Internal equivalent circuit |
|---|---|---|---|---|
| 1 | AM-ANT | 2.2 | AM antenna input pin.<br>The AM antenna coil is connected between pins 40 and this pin.<br>R = 100Ω |  |
| 2 | AM-REF | 2.2 | Reference voltage pin for AM.<br>VAM-REF = 2.2V |  |
| 3 | AM-CAP | - | Tuning pinl for AM.<br>(AM Capacitor Bank) |  |
| 4 | GND1 | 0 | GND pin for Analogue AM_FE part. | |
| 5 | VREF1 | 4.3 | Analogue part (tuner) reference bias terminal.<br>VREF1 = 4.3V |  |
| 6 | MPX IN_OUT | 2.5 | FM demodulation output /input for MPX.<br>R = 100Ω |  |
| 7 | AM RF-AGC | - | Pin for AM_RF AGC.<br>R1 = 2MΩ<br>R2 = 5kΩ<br>R3 = 250Ω<br>R4 = 1kΩ |  |
| 8 | GND2 | 0 | GND pin for Analogue tuner part. | |
| 9<br>10 | L-OUT<br>R-OUT | 2.6<br>(3.7V when LEVSHIF = 1) | L-ch (R-ch) output pin.<br>R = 100Ω<br>$R_{OUT}$ = 150Ω |  |

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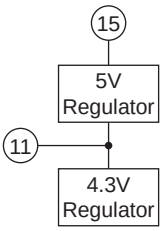
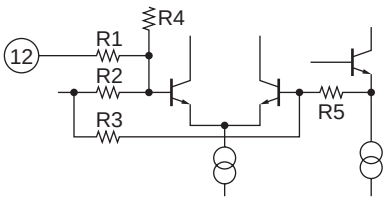
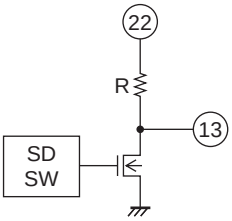
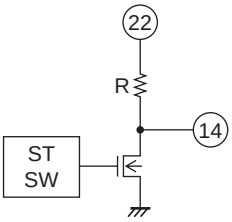
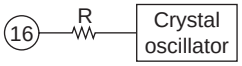
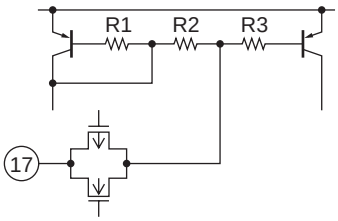
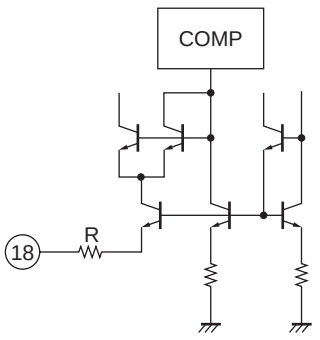
| Pin No. | Pin name | Pin voltage (V) | Description | Internal equivalent circuit |
|---|---|---|---|---|
| 11 | $V_{CC}$-Low | - | when using with $V_{CC}$ < 6.0V, 11Pin-15 Pin is shorted. |  |
| 12 | AM LCF | 2.2 | Terminal for AM Low-cut Filter.<br>R1 = 250Ω<br>R2 = 100kΩ<br>R3 = 100kΩ<br>R4 = 50kΩ<br>R5 = 50kΩ |  |
| 13 | SD-OUT | 3.0<br>(less than 0.1) | SD indicator output pin.<br>Active Low output.<br>R = 100kΩ |  |
| 14 | ST-OUT | 3.0<br>(less than 0.1) | FM stereo indicator output pin<br>Active Low output<br>R = 100kΩ |  |
| 15 | $V_{CC}$ | $V_{CC}$ | Analogue part power supply pin.<br>When using 8.5 to 9.5V, set to Register 1Eh Bit 1 (LEVSHIF) = 1<br>When using with $V_{CC}$ < 6.5V, set to Register 1Eh Bit 1 (LEVSHIF) = 0<br>And 11Pin-15Pin must be shorted “ | |
| 16 | CLK_IN | 2.1<br>(OSC mode) | For internal reference clock.<br>32.768kHz crystal connected to GND. It is Also applicable to input directly clock signals ( square wave GND_reference)<br>R = 100Ω |  |
| 17 | IF AGC CAP | - | This pin is for test.<br>Open<br>R1 = 1.5kΩ, R2 = 1kΩ, R3 = 500Ω |  |
| 18 | SD-ADJ | - | Open normally.<br>Adjust pin for SD sensitivity with to kΩ resistor connected to GND |  |

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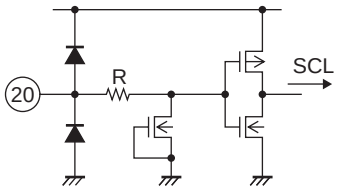
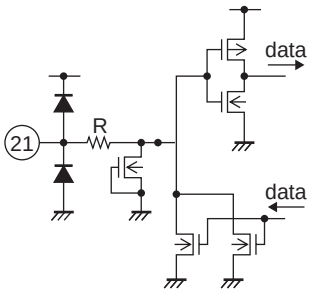
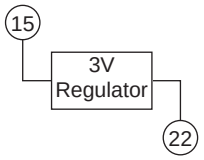
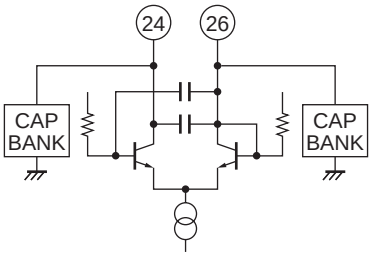
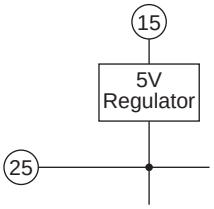
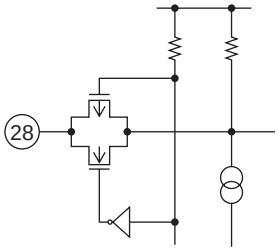
| Pin No. | Pin name | Pin voltage (V) | Description | Internal equivalent circuit |
|---|---|---|---|---|
| 19 | NC | - | | |
| 20 | SCL | - | Digital interface CLK line.<br><br>R = 1kΩ |  |
| 21 | SDA | | Digital interface DATA line.<br>(Interactive data communication line.)<br>Require pull_up resistor 3.3k to 10k<br>between this pin and Vref2 ($V_{DD}$).<br>R = 250Ω |  |
| 22 | VREF2 | 3 | Reference voltage output pin for Logic part.<br>Vref2 = 3V |  |
| 23 | GND3 | 0 | GND pin for digital part (Control part). | |
| 24<br>26 | L1<br>L2 | 5 | OSC coil of 39nH to be connected between this pin and pin 25. |  |
| 25 | VREF3 | 5 | Reference voltage pin for local oscillation circuit. |  |
| 27 | GND4 | 0 | GND pin for local oscillation circuit. | |
| 28 | FLL-CAP | - | LPF pi n for controlled FLL internally.<br>R = 80kΩ |  |
| 29 | GND5 | 0 | GND pin for local oscillation circuit. | |

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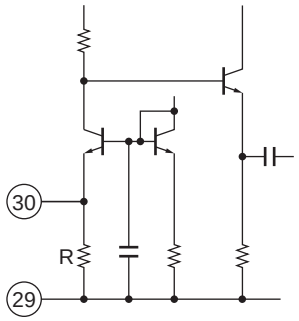
| Pin No. | Pin name | Pin voltage (V) | Description | Internal equivalent circuit |
|---|---|---|---|---|
| 30 | FM-ANT | 0.8 | FM antenna input pin FM.<br>R = 1.5kΩ<br>Rin = 75Ω |  |

## Used parts

| Component | Parameter | Value | Tolerance | Type | Supplier |
|---|---|---|---|---|---|
| L1 | Local Osc Coil | 39nH | 5% | LL2012-FHL39NJ | TOKO |
| L2 | Local Osc Coil | 39nH | 5% | LL2012-FHL39NJ | TOKO |
| L3 | AM Loop antenna | 18.1μH | 5% | 4910-CSL18R1JN1 | SAGAMI |
| T1 | AM RF matching | 250μH | - | A90326057 | COILS |
| | | | | #7003RNS-A1109YZS | TOKO |
| C1 | Ripple Filter | 1μF | | | |
| C2 | AM RF AGC Capacitor | 1μF | | | |
| C3 | Coupling Capacitor | 1μF | | | |
| C4 | Coupling Capacitor | 1μF | | | |
| C5 | Supply Bypass Capacitor | 0.1μF | | | |
| C6 | Supply Bypass Capacitor | 22μF | | | |
| C7 | AM Low-cut Filter | 0.1μF | | | |
| C8 | Supply Bypass Capacitor | 22μF | | | |
| C9 | Osc Filter | 0.1μF | | | |
| C10 | Ripple Filter | 0.1μF | | | |
| R1 | Pulled-up Resistor | 4.7kΩ | | | |
| R2 | Pulled-up Resistor | 4.7kΩ | | | |
| R3 | SD Adjust Resistor | to kΩ | | | |
| BPF | FM ANT BPF | - | - | GFMB7 | SOSHIN |
| X1 | Crystal | 32.768kHz | 100ppm | DT-26 | KDS |
| LO1 | AM Ferrite antenna | 260μH | TBD | - | - |

### Format of Bus Transfers

Bus transfers are primarily based on the $I^2C$ primitives

- Start condition
- Repeated start condition
- Stop condition
- Byte write
- Byte read

Start, restart, and stop conditions are specified as shown in Table 1 below.

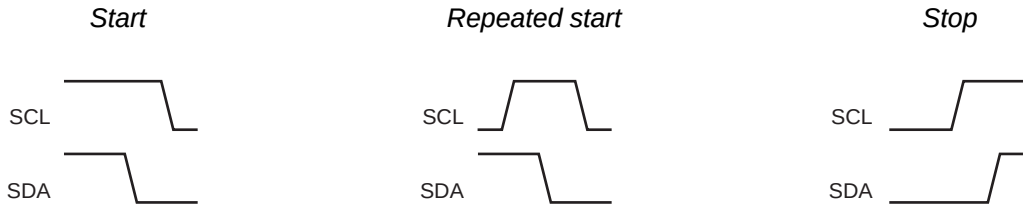



Fig. 1 the $I^2C$ start, repeated start and stop conditions.

For details, like timing, etc., refer to specifications of $I^2C$.

8-bit write

8-bit data is sent from the master microcomputer to LV23411.
Data bit consists of MSB first and LSB last.
Data transmission is latched at the rising edge of SCL in synchronization with the SCL clock generated at the master IC.
Do not change data while SCL remains HIGH.
LV23411 outputs the ACK bit between eighth and ninth falling edges of SCL

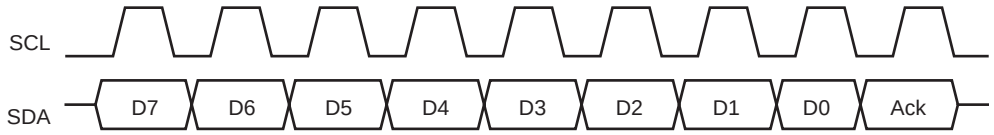



Fig. 2 Signal pattern of the $I^2C$ byte write

Read is of the same form as write, only except that the data direction is opposite.
Eight data bits are sent from LV23411 to the master while Ack is sent from the master to LV23411.

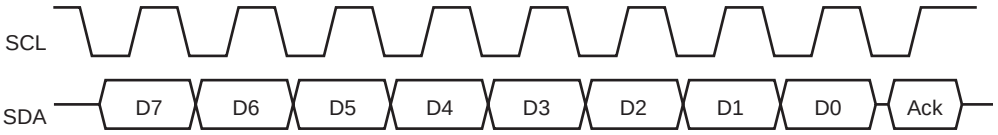



Fig. 3 Signal pattern of the $I^2C$ byte read

The serial clock SCL is supplied from the master side. It is essential that data bit is output from LV23411 in synchronization with the falling edge while the master side performs latching at the rising edge.

LV23411 latches ACK at the rising edge.
The sequence to write data D into the register A of LV23411 is shown below.

- Start condition
- write the device address (C0h)
- write the register address, A
- write the target data, D
- stop condition

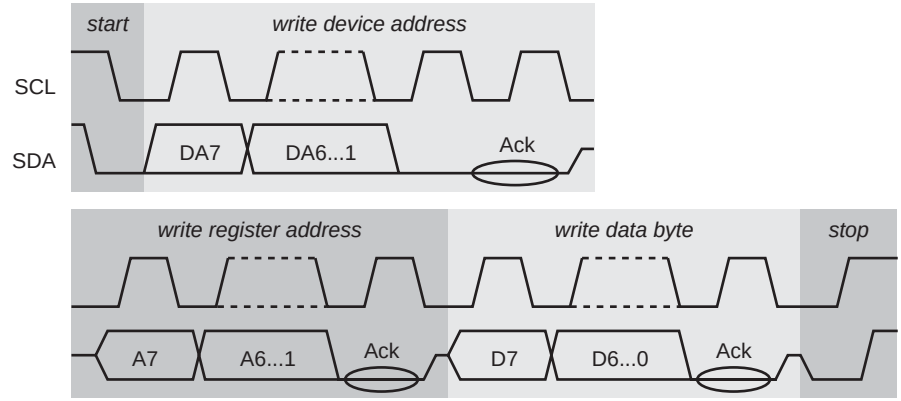



Fig. 4 Register write through $I^2C$

When one or more data has been provided for writing, only the first data is allowed to be written.

Read sequence

- start condition
- write the device address (C0h)
- write the register address, A
- repeated start condition (or stop + start in a single master network)
- write the device address + 1 (C1h)
- read the register contents D, transmit NACK (no more data to be read)
- stop condition

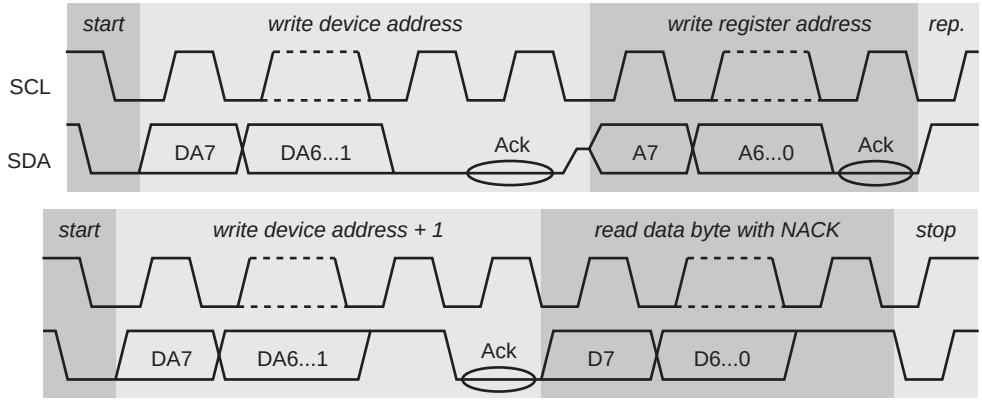


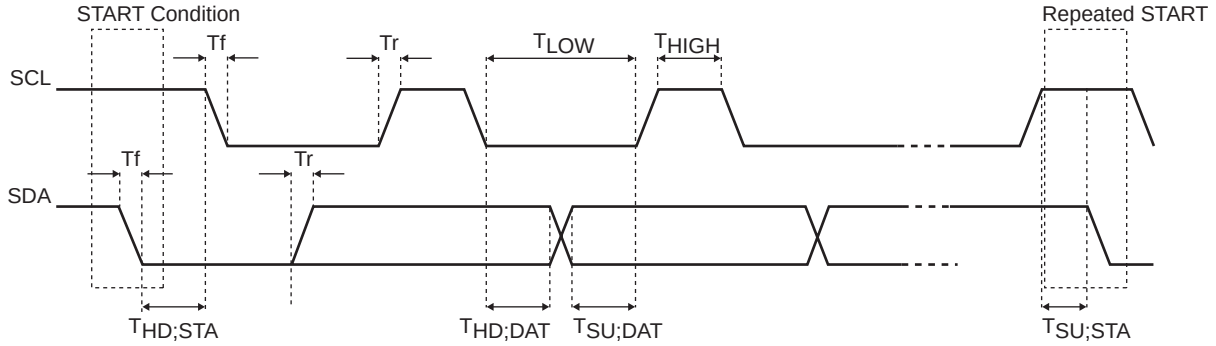

Fig. 5 Register read through $I^2C$

## Interrupt Pin INT

LV23411 has the dedicated interrupt output pin. For the active level to the host, either LOW or HIGH can be selected.
The INT output pin is kept floating while the PWRAD bit is cleared during initialization.
Therefore, to avoid influence on the CPU side during initialization, it is recommended to secure the non-active state by means of the pull-up or pull-down resistor.
This enables direct INT output connection to non-masking interruption of the host CPU.

## Digital interface specification (interface specification : reference)

(1). Characteristics of SDA and SCL bus line relative to the $I^2C$ bus interface




| Parameter | Symbol | Standard-mode | | High_Speed-mode | | unit |
|---|---|---|---|---|---|---|
| | | min | max | min | max | |
| SCL clock frequency | $F_{SCL}$ | 0 | 100 | 0 | 400 | kHz |
| Fall time of both SDA and SCL | Tf | | 300 | 20+0.1Cb | 300 | ns |
| Rise time of both SDA and SCL | Tr | | 1000 | 20+0.1Cb | 300 | ns |
| High time of SCL | $T_{HIGH}$ | 4.0 | | 0.6 | | µs |
| Low time of SCL | $T_{LOW}$ | 4.7 | | 1.3 | | µs |
| Hold time of STAT condition | $T_{HD\ ;\ STA}$ | 4.0 | | 0.6 | | µs |
| Hold time of Data | $T_{HD\ ;\ DAT}$ | 0 | 3.45 | 0 | 0.9 | µs |
| Set-up time of STAT condition | $T_{SU\ ;\ STA}$ | 4.7 | | 0.6 | | µs |
| Set-up time of STOP condition | $T_{SU\ ;\ STO}$ | 4.0 | | 0.6 | | µs |
| Set-up time of Data | $T_{SU\ ;\ DAT}$ | 250 | | 100 | | ns |
| Bus free time between a STOP and START condition | $T_{BUF}$ | 4.7 | | 1.3 | | µs |
| Capacitivie load for each bus line | Cb | | 400 | | 400 | pF |

*Cb = Total capacitance of one bus line

## Description of the Register of LV23411V

*Register 00h - CHIP_ID - Chip identify register (Read-Only)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ID[7:0] | | | | | | | |

Bit 7-0 : ID[7:0] : 8-bit Chip ID
LV243411 : 1Bh
Note : To abort the command, write any value in this register.

*Register 01h - CHIP_REV - Chip Revision identify register (Read-Only)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Revision[7:0] | | | | | | | |

Bit 7-0 : ID[7:0] : 8-bit Chip Revision
ES1 : 00h
Note : To abort the command, write any value in this register.

*Register 02h - RADIO_STAT - Radio station status (Read-Only)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IM_STAT | IM_FS[1:0] | | MO_ST | FS[2:0] | | | TUNED |

Bit 7 : IM_STAT : State of Image-station avoidance
0 = Normal (Possible to write)
1 = The Image-station avoidance is being processed (Impossible to write)
Note :
This bit works only at Register14h_bit7 (IM_EVAS) is set to “1”.
The writing processing to LV23411 is prohibited when this bit is “1”.

Bit 6-5 : IM_FS : Image-signal Fieldstrength
0 : No image-signal
1 : There are weak Image-signal that level is less -10dB or more weaker than desire’s
2 : The level of the image –signal is around 0 - 10dB compared with desire’s
3 : The level of the image-signal is +10dB or more stronger than that of desire’s

Bit 4 : MO_ST : Mono/Stereo indicator
0 = Forced monaural
1 = Normal (Receiving in stereo mode)

Bit 3-1 : FS[2:0] : Fieldstrength
0 : FS < 10 dBμV
1 : FS = 10 - 20 dBμV
2 : FS = 20 - 30 dBμV
……
7 : FS > 70 dBμV

Bit 0 : TUNED : Radio tuning flag.
0 = No tuned
1 = Tuned
Note : When the tuning command succeeds, this bit is set.
This bit is cleared under 3 conditions as below.
1. PW_RAD = 0
2. Tuning Frequency
3. When FLL becomes outside the correction range

*Register 04h - TNPL - Tune position low (Read-Only)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TUNEPOS[7:0] | | | | | | | |
| Bit 7-0 : TUNEPOS[7:0] : Current RF Frequency (Low 8 bit) | | | | | | | |

*Register 05h - TNPH_STAT - Tune position high/status (Read-Only)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ERROR[1:0] | | TUNEPOS[12:8] | | | | | |

Bit 7-6 : ERROR[1:0] : Error code

| ERROR[1:0] | Remark |
|---|---|
| 0 | OK, Command end (No Error) |
| 1 | DAC Limit Error |
| 2 | Command forced End |
| 3 | Command busy |

Bit 5:0 : TUNEPOS[13:8] : Current RF Frequency (High 5 bit)

*Register 06h - COUNT_L - Counter low (Read-Only)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COUNT[7:0] | | | | | | | |
| Bit 7-0 : COUNT[7:0] : Counter value (Low 8 bit) | | | | | | | |

*Register 07h - COUNT_H - Counter High (Read-Only)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| COUNT[15:8] | | | | | | | |
| Bit 7-0 : COUNT[15:8] : Counter value (High 8 bit) | | | | | | | |

*Register 08h - IF_OSC - DAC for IF OSC (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IFOSC[7:0] | | | | | | | |
| Bit 7-0 : IFOSC[7:0] : IF Oscillator DAC | | | | | | | |

*Register 09h - IFBW-DAC for IF - Filter Band width (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IFBW[7:0] | | | | | | | |
| Bit 7-0 : IFBW[7:0] : IF-Filter Band width DAC | | | | | | | |

*Register 0Bh - STEREO_OSC - DAC for Stereo Decoder OSC (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SDOSC[7:0] | | | | | | | |
| Bit 7-0 : SDOSC[7:0] : Stereo Decoder Oscillator DAC | | | | | | | |

*Register 0Ch - RF_OSC - DAC for RF OSC (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RFCAP[7:0] | | | | | | | |
| Bit 7-0 : RFOSC[7:0] : RF Oscillator DAC | | | | | | | |

*Register 0Dh - RFCAP - RF Cap bank (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RFCAP[7:0] | | | | | | | |
| Bit 7-0 : RFCAP[7:0] : RF Oscillator Capacitor-Bank | | | | | | | |

*Register 0Eh - AMCAP1 - AM - ANT Cap bank1 (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AMCAP[7:0] | | | | | | | |

Bit 7-0 : AMCAP[7:0] : AM Antenna Capacitor-Bank

Note :
The AM antenna capacitor bank is composed of 12 bits.
High 4 bit is arranged at “AMCTRL” register.

*Register 0Fh - AMCTRL - AM Station Control (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AMDIV[2:0] | | | AM_CAL | ACAP11 | ACAP10 | ACAP9 | ACAP8 |

Bit 7-5 : AMDIV[2:0] : AM Clock Divider
Bit 7 : AM_CD2 : AM Clock Divider bit 2.
Bit 6 : AM_CD1 : AM Clock Divider bit 1.
Bit 5 : AM_CD0 : AM Clock Divider bit 0.

Note : The AM_CD[2:0] is used to decrease frequency from FM - band to AM - band.
Please set AM_CD to “0” at FM mode.

| AM_CD[2:0] | Divide-Rate | AM-RF frequency (In kHz) |
|---|---|---|
| 0,1 | Divider OFF | 0 (FM mode) |
| 2 | 224 | 338 - 483 |
| 3 | 160 | 474 - 676 |
| 4 | 112 | 676 - 966 |
| 5 | 80 | 947 - 1353 |
| 6 | 64 | 1183 - 1692 |
| 7 | 48 | 1578 - 2256 |

Bit 4 : NA (Fixed to “0”)

Bit 3-0 : AMCAP[11:8] : AM Antenna Capacitor-Bank
Bit 3 : AMCAP_bit 11
Bit 2 : AMCAP_bit 10
Bit 1 : AMCAP_bit 9
Bit 0 : AMCAP_bit 8

*Register 10h - DO_REF_CLK_CNF - DO output mode and reference clock configuration (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IPOL | DO_SEL[1:0] | | EXT_CLK_CFG[1:0] | | FS_S[2:0] | | |

Bit 7-5 : NA (Fixed to “0”)

Bit 4-3 : EXT_CLK_CFG[1:0] : External Clock Setting

| EXT_CLK_CFG[1:0] | Reference clock |
|---|---|
| 00 | Off |
| 01 | Oscillator clock source (External Clock source) |
| 10 | 32768Hz crystal oscillator |
| 11 | No use |

Bit 2-0 : FS_S[2:0] : SD (Station Detector) operation level setting

*Register 11h - IF_SEL - IF frequency selection (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FLL_MOD | AMIF[2:0] | | | FMIF[3:0] | | | |

Bit 7 : FLL_MOD: FLL operation mode
0 : Smoothing Filter = OFF
1 : Smoothing Filter = ON

Bit 6-4 : AMIF[2:0] : IF frequency setting at AM mode

| AMIF[2:0] | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 20kHz | 31kHz | 42kHz | 53kHz | 64kHz | 75kHz | 86kHz | 97kHz |

Bit 3-0 : FMIF[3:0] : IF frequency setting at FM mode (kHz)

| SE_AM | RF_SEL | FMIF[3:0] | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 0 | 0 | 112.5 | 125 | 137.5 | 150 | 162.5 | 175 | 187.5 | 212.5 | 225 | 237.5 | 250 | 262.5 | 275 | 287.5 | 312.5 | 325 |
| 0 | 1 | 112.5 | 127.5 | 142.5 | 157.5 | 157.5 | 172.5 | 187.5 | 202.5 | 217.5 | 232.5 | 247.5 | 262.5 | 277.5 | 292.5 | 307.5 | 322.5 |

*Register 12h - REF_CLK_MOD - Slope correction (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REFMOD[7:0] | | | | | | | |

Bit 7-0 : REFMOD[7:0] : Reference clock collection

*Register 13h - SM_CTRL - Statemachine control (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FLL_ON | CLKS_SE[2:0] | | | nSD_PM | nIF_PM | CM_SE[1:0] | |

Bit 7 : FLL_ON : FLL control
0 = FLL OFF
1 = FLL ON

Bit 6-4 : CLKS_SE : Clock source selection
0 = No select
1 = Stereo Decoder Oscillator is selected
2 = IF Oscillator is selected
3 = AM Antenna Oscillator is selected
4 = FM RF Oscillator is selected
5 = AM RF Oscillator is selected
6 - 7 = No select

Note : Bit[6-4] set oscillator source.
Select arbitrary clock oscillator at tuning or calibrations or measure.

Bit 3 : nSD_PM : Stereo Decoder PLL mute
0 = SD PLL Off (Calibration)
1 = SD PLL On (Normal operation)

Bit 2 : nIF_PM : IF PLL mute
0 = IF PLL Off (Calibration)
1 = IF PLL On (Normal operation)

Bit 1-0 : CM_SE : Command mode selection
0 = No command
1 = Measure mode
2 = Calibration mode
3 = Radio tuning (RF frequency tuning) mode

Note : This bit used to select command mode.
Select the arbitrary command to be executed.
The command is executed by setting TARGET_VAL_L/H.

Command execution time :
SD calibration = 540ms
IF calibration = 134ms
RF (FM) tuning = 105ms
RF (AM) tuning = 158ms

Note:
Please wait the time provided for the above-mentioned before all processing including reading the register after having executed the command.

*Register 14h - REF_CLK_PRS - Reference clock pre-scaler (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IM_EVAS | Reserved | WAIT_SEL | AM_FINE | REFPRE[3:0] | | | |

Bit 7 : IM_EVAS : Image signal avoidance function ON/OFF
0 = OFF
1 = ON (Recommend)

Bit 6 : Reserved : Fixed to “0”

Bit 5 : WAIT_SEL : Selection mute release standby time after tuning
0 = 8ms wait
1 = 4ms wait

Bit 4 : AM_FINE : Selection AM_ANT adjustment standby time
0 = No wait when DAC value is changed
1 = 2ms wait when DAC value is changed

Bit 3-0 : REFPRE[3:0] : Reference Clock pre- scaler
0 = 1 : 1
1 = 1 : 2
2 = 1 : 4
…
15 = 1 : 32768

*Register 15h - REF_CLK_DIV - Reference clock divider (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REFDIV[7:0] | | | | | | | |

Bit 7-0 : REFDIV[7:0] : Reference Clock Divider
0 : Divide rate = 1
1 : Divide rate = 2
…
255 : Divide rate = 256

*Register 16h - TARGET_VAL_L - Target Value Low Register (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TARGET[7:0] | | | | | | | |

Bit 7-0 : TARGET[7:0] : Target frequency low 8 bit :
Tuning frequency or Calibration frequency : low byte

*Register 17h - TARGET_VAL_H - Target Value High Register (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TARGET[15:8] | | | | | | | |

Bit 7-0 : TARGET[15:8] : Target frequency high 8 bit :
Tuning frequency or Calibration frequency : high byte

With radio power ON, lower eight bits of the target frequency are set. Then, set higher eight bits of the target frequency to this register. The command is executed.

TUNEPOS and TARGET :
- AM mode : 1kHz span
- FM mode : 10kHz span

*Register 18h - RADIO_CTRL1 - Radio control 1 (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IQC_CTR | IFPOL | OSC_LEV[1:0] | | DEEM | VOL[1:0] | | EN_AMHC |

Bit 7 : IQC_CTR : I/Q phase change
0 = Normal mode (Upper heterodyne)
1 = I/Q phase change : for image signal avoidance (Lower heterodyne)
Note : Usually, no-need to change

Bit 6 : IF pole change by State Machine
0 = The IF frequency is added to local frequency (Normal)
1 = The IF frequency is subtracted from local frequency
Note : Usually, no-need to change

Bit 5-4 : OSC_LEV[1:0] : RF-OSC oscillation level setting
0 = minimum level
3 = maximum level
Note : 3dB steps, Level = 2 is recommended

Bit 3 : DEEM : De-emphasis setting
0 = 50µs : Korea China, Europe, Japan
1 = 75µs : USA

Bit 2-1 : VOL[1:0] : Volume setting
0 = minimum (VOL0)
……
3 = maximum (VOL3)

Bit 0 : EN_AMHC : AM High-cut Filter ON/OFF
0 = AM HCF OFF
1 = AM HCF ON

*Register 19h - RADIO_CTRL2 - Radio control 2 (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | EN_AMM | Reserved | IF_AGC_LEV | RF_AGC_LEV[1:0] | | EN_RFAGC |

Bit 7 : Reserved : Fixed to “0”

Bit 6 : Reserved : Fixed to “1”

Bit 5 : EN_AMM : AM Mute ON/OFF
0 = AM mute OFF
1 = AM mute ON

Bit 4 : Reserved : Fixed to “0”

Bit 3 : IF_AGC_LEV : IF-AGC Level Control
0 = AGC slow mode
1 = AGC first mode

Bit 2-1 : RF_AGC_LEV[1:0] : RF-AGC Level Control
0 = AGC slow mode
1 = AGC normal mode
3 = AGC first mode

Bit 0 : EN_RFAGC : RF-AGC ON/OFF
0 = AGC OFF
1 = AGC ON (Normal)

*Register 1Ah - RADIO_CTRL3 - Radio control 3 (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DEEM_100 | NA | | IF_AGC_CAP | AM_WIDE_AGC_OFF | | AM_WIDE_AGC_ON | |

Bit 7 : DEEM_100 : Additional De-emphasis (100µs)
0 = 0µs (Default setting)
1 = 100µs (DEEM = 1 : 75µS)

Bit 6 : NA

Bit 4 : IF_AGC_CAP
0 = OFF (Normal)
1 = ON

Bit 3-2 : AM_WIDE_AGC_OFF[1:0] : AM WIDE AGC OFF Level Control
0 = First mode
3 = Slow mode

Bit 1-0 : AM_WIDE_AGC_ON[1:0] : AM WIDE AGC ON Level Control
0 = WIDE AGC OFF
1 = First mode
3 = Slow mode

*Register 1Ch - STEREO_CTRL1 - Stereo control 1 (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CRC[1:0] | | SS_SP2 | Reserved | Reserved | PICAN_EN | FOSTEREO | ST_M |

Bit 7-6 : CRC[1:0] : Capture Range Control
0 = Narrow mode
3 = Wide mode

Bit 5 : SS_SP2 : Stereo=ON sensitivity speed2 (First mode)
0 : First mode = OFF
1 : First mode = ON (Recommend)

Bit 4 : Reserved : Fixed to “0”

Bit 3 : Reserved : Fixed to “0

Bit 2 : PICAN_EN : PILOT signal Cancellation ON/OF
0 = OFF
1 = ON (Recommend)

Bit 1 : FOSTEREO : Forced Stereo
0 = OFF (Normal)
1 = ON

Bit 0 : ST_M : Mono/Stereo setting
0 = Stereo on (Normal)
1 = Stereo off (Forced mono)

*Register 1Dh - STEREO_CTRL2 - Stereo control 2 (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NA | | | FOAMAGC | Reserved | OVER_MOD | CPAJ[2:0] | |

Bit 7-5 : NA

Bit 4 : FOAMAGC
0 : Forced - AGC = OFF
1 : Forced - AGC = ON

Bit 3 : Reserved: Fixed to “0”

Bit 2 : OVER_MOD : Over-modulation detector ON/OFF
0 = OFF
1 = ON

Bit 1-0 : CPAJ[1:0] : Channel separation adjacent
0 = Minimum Sub-signal level
7 = Maximum Sub-signal level

*Register 1Eh - RADIO_CTRL4 - Radio control 4 (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SOFTST[2:0] | | | SOFTMU[2:0] | | | LEVSHIF | FO_SOFTT |

Bit 7-5 : SOFTST[2:0] : Soft Stereo Function (Stereo-Blend)
0 : Soft Stereo = OFF
7 : Soft Stereo = Lev7 (Max)

Bit 4-2 : SOFTMU[2:0] : Soft Audio mute Function
0 : Soft mute = OFF
7 : Soft mute = Lev7 (Max)

Bit 1 : LEVSHIF : Audio Line-out DC level shift
0 = Normal DC level ($V_{CC}$ = 5.0V)
1 = DC level is shifted ($V_{CC}$ =9.0V)

Bit 0 : FO_SOFTST : Forced Soft Stereo Function
0 : ON (Normal)
1 : OFF

*Register 1Fh - RADIO_CTRL5 - Radio control 5 (Read/Write)*

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RF_SEL | IFRIM | nAGC_SPD | SE_FM/AM | AMP_CTR | MUTE | AM_CAL | PW_RAD |

Bit 7 : RF_SEL : RF tuning range select
0 = Normal ( Japan/USA/Europe)
1 = OILT (65MHz to 74MHz)

Bit 6 : IFRIM : IF OSC limit setting
0 : Max = 350kHz (FM mode)
1 : Max = 150kHz (AM mode)

Bit 5 : nAGC_SPD : IF AGC speed setting
0 = High speed (FM mode)
1 = Normal (AM mode)

Bit 4 : SE_FM/AM : AM/FM mode select
0 = FM mode
1 = AM mode

Bit 3 : AMP_CTR : Audio Amp ON/OFF
0 = OFF
1 = ON

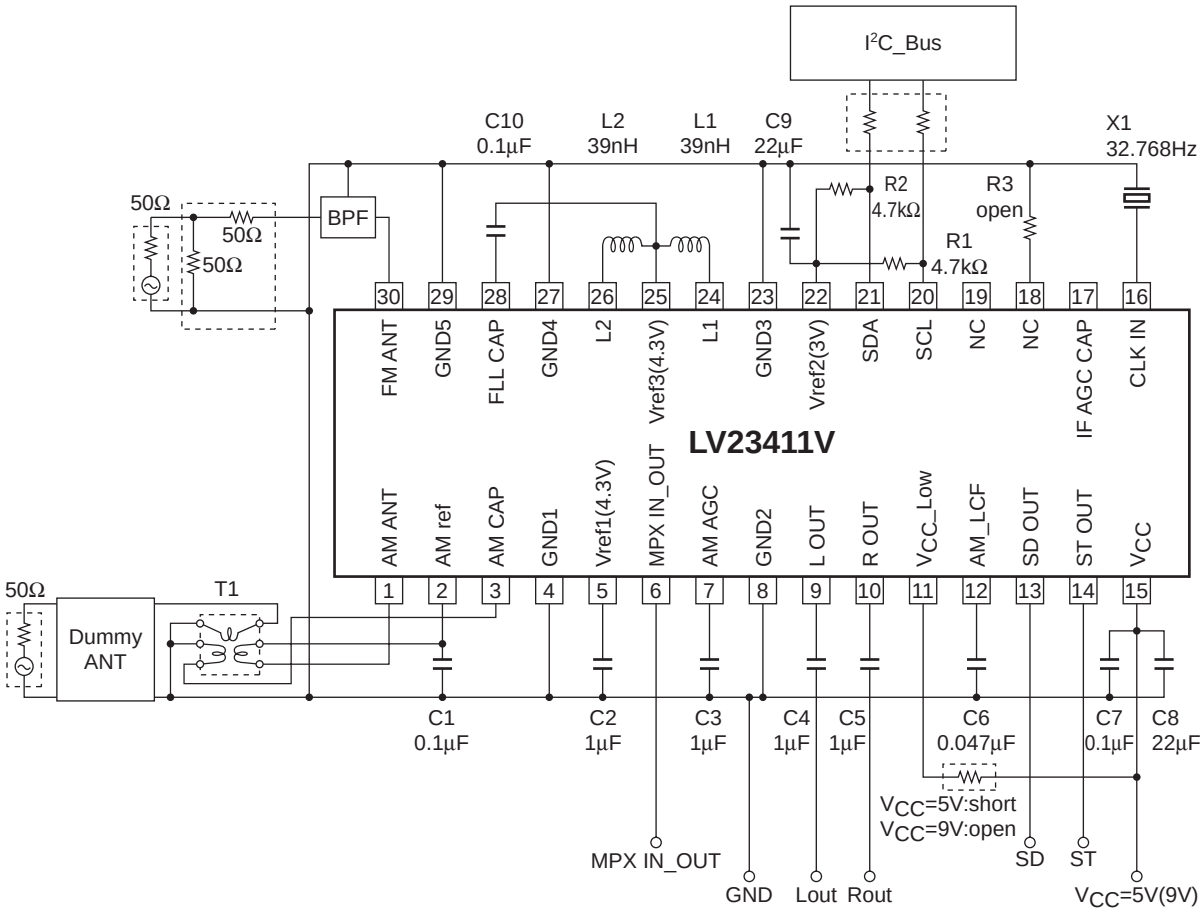
Bit 2 : MUTE : Audio Mute ON/OFF
0 = ON
1 = OFF

Bit 1 : AM_CAL : AM Calibration (Antenna tuning mode)
0 = AM Receiving mode (Normal)
1 = AM Calibration mode (AM antenna tuning mode)
Note : Set this bit to “1”, if ANT calibration frequency is measured.

Bit 0 : PW_RAD: Radio Power
0 = Power OFF (power save mode)
1 = Power ON

*1 : After the $V_{CC}$ voltage is impressed, PW_RAD is automatically set to "0" in 50ms.
*2 : When the $V_{CC}$ voltage is dropped once, content of registers other than PW_RAD becomes irregular.

## Test Circuit



## Application Circuit Example